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FAIRCHILD SEMICONDUCTOR®

April 2011

FUSB1500 — USB2.0 Full-Speed / Low-Speed Transceiver with Charger Detection

Features

- Complies with USB2.0 Specification
- Supports 12Mbps and 1.5Mbps USB2.0 Speeds
  - Single Ended (SE) Mode Signaling
  - Slew-Rate Controlled Differential Data Driver
  - Differential Input Receiver with Wide Common-Mode Range and High Input Sensitivity
  - Stable RCV Output during SE0 Condition
  - Two Single-Ended Receivers with Hysteresis
- Supports I/O Voltage: 1.65V to 3.6V

Applications

- Dual-Camera Applications for Cell Phones
- Dual-LCD Applications for Cell Phones, Digital Camera Displays, and Viewfinders

Description

The FUSB1500 is a USB2.0 FS/LS transceiver with resistive charger detection. It is compliant with the Universal Serial Bus Specification, Rev. 2.0 (USB2.0).

Ideal for portable electronic devices; such as mobile phones, digital still cameras, and personal digital assistants; it allows USB Application Specific ICs (ASICs) and Programmable Logic Devices (PLDs) with power supply voltages from 1.65V to 3.6V to interface with the physical layer of the Universal Serial Bus.

The FUSB1500 can be used as a USB device transceiver or a USB host transceiver. It can transmit and receive serial data at both full-speed (12Mbps) and low-speed (1.5Mbps) data rates.

The FUSB1500 supports the SE Mode controller interface.

IMPORTANT NOTE:

For additional performance information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FUSB1500MHX	-40 to +85°C	FUSB 1500	16-Pin, Molded Leadless Package (MLP), JEDEC MO217 Equivalent, 3mm Square	Tape and Reel

Block Diagram

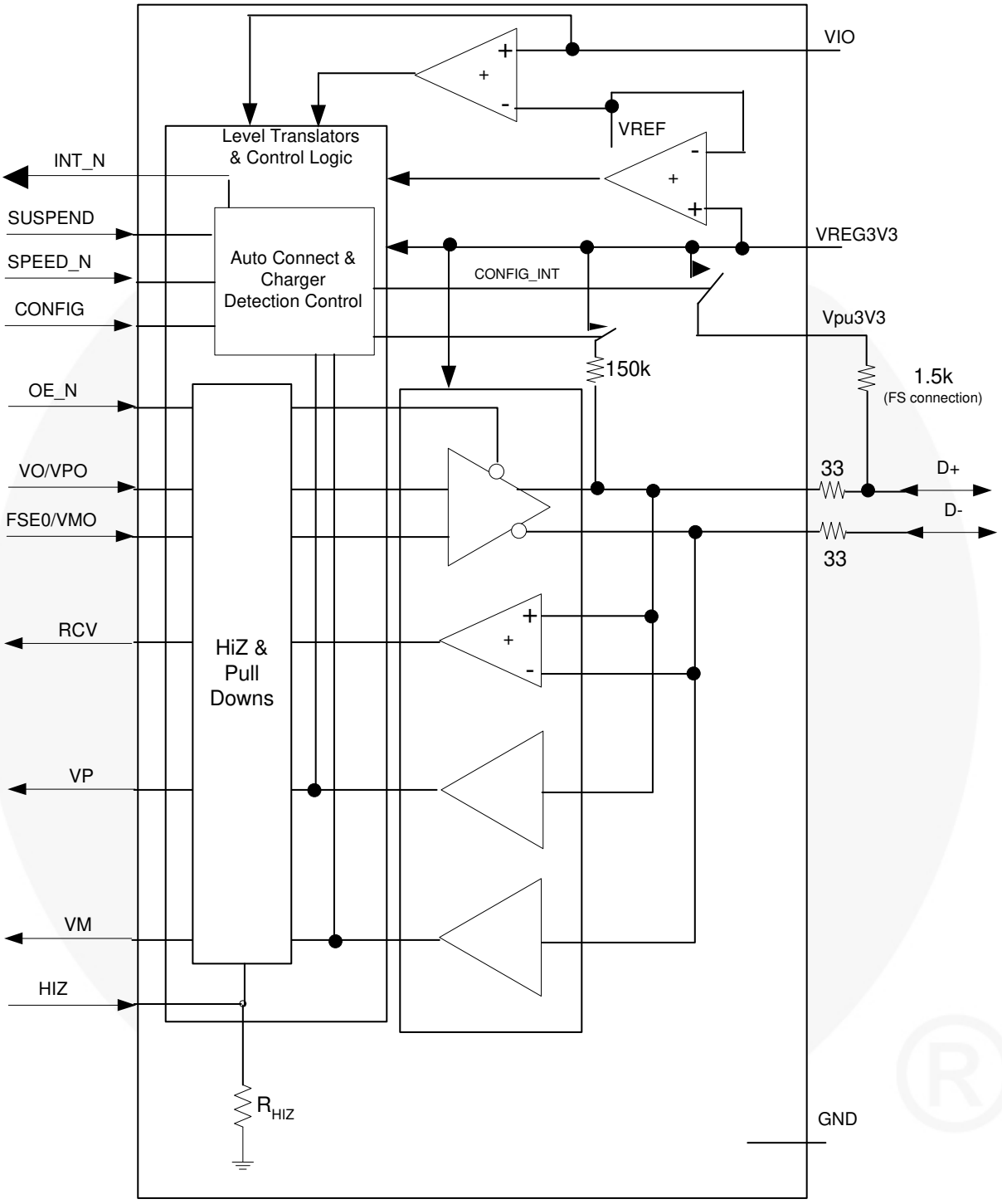


Figure 1. Functional Block Diagram

Pin Configuration

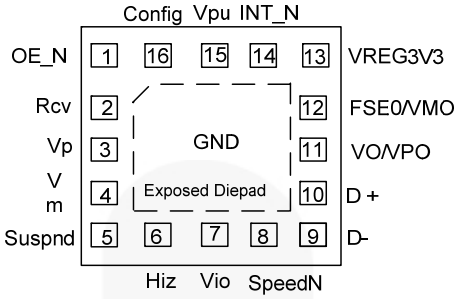


Figure 2. Pin Configuration (Top-Through View)

Pin Definitions

Pin #	Name	I/O	Description
1	OE_N	I	Output enable. Active LOW enables the transceiver to transmit data on the bus. When not active, the transceiver is in the receive mode (CMOS level is relative to V_{IO}).
2	RCV	O	Receive data output. Non-inverted CMOS level output for USB differential input (CMOS output level is relative to V_{IO}). Driven LOW when SUSPND mode is active; (SUSPND is only enabled per the specific extended control table – *see Table 4*); RCV output is stable and preserved during SE0 condition.
3	VP	O	Single-ended D+ receiver output VP (CMOS level relative to V_{IO}); used for external detection of SE0, error conditions, speed of connected device; driven HIGH when no supply connected to V_{REG3V3}.
4	VM	O	Single-ended D- receiver output VM (CMOS level relative to V_{IO}); used for external detection of SE0, error conditions, speed of connected device; driven HIGH when no supply is connected to V_{REG3V3}.
5	SUSPND	I	Suspend. Enables a low-power state (CMOS level is relative to V_{IO}). While the FUSB1500 is suspended, it drives the RCV pin to logic “0” state. (Suspend is only enabled per the specific extended control table – *see Table 4*).
6	HiZ	I	High-Z input (CMOS level is relative to V_{IO}). HIGH selects the high-Z mode, which puts all the outputs, including VPU, in high impedance. There is a 100kΩ weak pull-down on this pin.
7	VIO		Supply voltage for digital I/O pins (1.65V to 3.6V). When not connected, the D+ and D- pins are in three-state. This supply bus is independent of VPU and VREG3V3.
8	SPEED_N	I	Speed selection input (CMOS level relative to V_{IO}); adjusts the slew rate of differential outputs D+ and D- according to the extended control table *(see Table 4)*.
9	D-	AI/O	Data- bus connection.
10	D+	AI/O	Data+ bus connection; for FS peripheral mode, connect to VPU via 1.5kΩ.
11	VO/VPO	I	Driver data input (CMOS level is relative to V_{IO}); Schmitt-trigger input; VO is input pin for SE Mode.
12	FSE0/VMO	I	Driver data input (CMOS level is relative to V_{IO}); Schmitt-trigger input; FSE0 is input pin for SE Mode, *see Table 2 and Table 3.*
13	VREG3V3		Supply voltage input for 3.3V operation.
14	INT_N	O	This interrupt is active LOW. It is asserted when an SE0 is seen on the USB bus (SE0 detection circuit is only enabled per the specific extended control table). It is also referenced to V_{IO}.
15	VPU		Pull-up supply voltage (3.3V±300mV); connect an external 1.5kΩ resistor on D+ (FS data rate) or D- (LS data rate). Internal switch is controlled by the CONFIG, SPEED_N, and SUSPND input pins (*see Table 4*).
16	CONFIG	I	USB connect or disconnect, software-control input. SPEED_N and SUSPND also gate the pull-up resistor (*see Table 4*).
Exposed Die Pad	GND	GND	GND supply bonded to exposed die pad to be connected to the PCB GND.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{IO}	I/O Supply Voltage		-0.5	4.6	V
V_{PU}, V_{REG3V3}	Regulated Supply Voltage and Pull-up Supply		-0.5	4.6	V
I_{LU}	Latch-up Current	V_{IN} = -1.8 to +5.4V		150	mA
I_{IK}	DC Input Current	V_{IN} < 0		-50	mA
V_{IN}	DC Input Voltage[1]		-0.5	V_{IO} +0.5	V
I_{OK}	DC Output Diode Current	V_{OUT} > V_{REG3V3} or < 0		±50	mA
V_{OUT}	DC Output Voltage[1]		-0.5	V_{IO} +0.5	V
I_{OUT}	DC Output Source or Sink Current for D+, D- Pins	V_{OUT} = 0 to V_{REG3V3}		±50	mA
	DC Output Source or Sink Current for RCV, VM/VP	V_{OUT} = 0 to V_{REG3V3}		±15	
$I_{VREG3V3}$, I_{GND}	DC $V_{VREG3V3}$ or GND Current			±100	mA
ESD	Human Body Model, JEDEC: JESD22-A114	Pins D+, D-, I_{LI} < 3μA	-10500	+10500	V
		VREG3V3, VIO, and GND; I_{LI} < 3μA;	-12000	+12000	
		All Other Pins, I_{LI} < 1μA	-6500	+6500	
	Machine Model, JESD22-A115			200	
	Charged Device Model, JEDEC: JESD-C101			+1500	
	IEC 61000-4-2	Air Gap		+15000	
		Contact		+8000	
T_{STG}	Storage Temperature Range		-40	+125	°C
P_D	Power Dissipation	$I_{CC(VREG3V3)}$		48	mW
		I_{CCIO}		9	

Note:
1. Absolute maximum ratings for I/O must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{REG3V3}	DC Supply Voltage		3.0	3.6	V
V_{IO}	I/O DC Voltage		1.65	3.60	V
V_{IN}	DC Input Voltage Range		0	V_{IO}	V
$V_{AI/O}$	DC Input Range for AI/Os	Pins D+ and D-	0	3.6	V
T_A	Operating Ambient Temperature		-40	+85	°C

Electrical Characteristics — Supply Pins DC Characteristics

Unless otherwise noted, values are over the recommended range of supply voltage and operating free air temperature. V_{REG3V3} = 3.0V to 3.6V and V_{IO} = 1.65V to 3.6V.

Symbol	Parameter	Test Conditions	T_A=-40°C to 85°C			Units
			Min.	Typ.	Max.	
V_{REG3V3}	Regulated Supply Input[2,3]		3.0	3.3	3.6	V
$I_{VREG3V3}$	Operating Supply Current (V_{REG3V3})[4]	Transmitting and Receiving at 12Mbps; C_{LOAD} = 50pF(D+, D-)		4	8	mA
I_{CCIO}	I/O Operating Supply Current[4]	Transmitting and Receiving at 12Mbps		1	2	mA
I_{IDLE}	Supply Current During FS Idle and SE0 (V_{REG3V3})[5]	IDLE: $V_{D+} \geq 3.0V$, $V_{D-} \leq 0.3V$; SE0: $V_{D+} \leq 0.3V$, $V_{D-} \leq 0.3V$			500	µA
$I_{CCIO(STATIC)}$	I/O Static Supply Current	IDLE, SUSPND, or SE0			20	µA
I_{SUSPND}	Suspend (V_{REG3V3}) Supply Current[5]	SUSPND = H; OE_N = H or L; D+ = D- = Not Floating; VM = VP = Open			25	µA
$I_{DISABLE}$	Disable-Mode (V_{REG3V3}) Supply Current[5]	VIO Not Connected, D+ = D- = Not Floating			25	µA
$I_{SHARING}$	I/O Sharing-Mode Supply Current	VREG3V3 Not Connected			20	µA
$I_{D\pm (SHARING)}$	Sharing-Mode Load Current on D+/D- Pins	VREG3V3 Not Connected, CONFIG = LOW, $V_{D\pm}$ = 3.6V			10	µA
V_{REF}	V_{IO} Threshold-Detection Voltage	Supply Lost			0.5	V
		Supply Present	1.4			
V_{IO_hys}	V_{IO} Threshold-Detection Hysteresis Voltage[4]	V_{REG3V3} = 3.3V		450		mV

Notes:

2. I_{LOAD} includes the pull-up resistor current via the VPU pin.
3. The minimum voltage in Suspend Mode is 2.7V.
4. Not tested in production; value based on characterization.
5. Excludes any current from load and V_{PU} or V_{SW} current to the 1.5kΩ and 15kΩ pull-up / pull-down resistors (200µA typical).

Electrical Characteristics — Digital Pins DC Characteristics

Excludes D+ and D- pins. Unless otherwise noted, values are over the recommended range of supply voltage and operating free air temperature. V_{REG3V3} = 3.0V to 3.6V and V_{IO} = 1.65V to 3.6V.

Symbol	Parameter	Test Conditions	T_A=-40°C to 85°C		Units
			Min.	Max.	
Input Levels					
V_{IL}	LOW-Level Input Voltage			0.3	V
V_{IH}	HIGH-Level Input Voltage		0.6 • V_{IO}		V
Output Levels					
V_{OL}	LOW-Level Output Voltage	I_{OL} = 2.0mA		0.4	V
		I_{OL} = 100μA		0.15	
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 2.0mA	V_{IO} - 0.4		V
		I_{OH} = 100μA	V_{IO} - 0.15		
Leakage Current					
I_{LI}	Input Leakage Current, Excluding HIZ	V_{IO} = 1.65 to 3.60V	-1	+1	μA
Capacitance					
C_{IN}, $C_{I/O}$	Input Capacitance[6]	Pin to GND		10	pF
Resistance					
R_{HIZ}	Pull-Down Resistance on HIZ Input Pin		100		kΩ
R_{CHRGPU}	Pull-Up Resistance for CHRGR Function		105	171	kΩ

Note:

6. Not tested in production; value based on characterization.

Electrical Characteristics — Analog I/O Pins DC Characteristics

Unless otherwise noted, values are over the recommended range of supply voltage and operating free air temperature. V_{REG3V3} = 3.0V to 3.6V and V_{IO} = 1.65V to 3.6V.

Symbol	Parameter	Test Conditions	T_A=-40°C to 85°C		Units
			Min.	Max.	
Input Levels – Differential Receiver					
V_{DI}	Differential Input Sensitivity	$\lvert V_{IN(D+)} - V_{IN(D-)} \rvert$	0.2		V
V_{CM}	Differential Common Mode Voltage		0.8	2.5	V
Input Levels – Single-Ended Receiver					
V_{IL}	LOW-Level Input Voltage			0.8	V
V_{IH}	HIGH-Level Input Voltage		2.0		V
V_{HYS}	Hysteresis Voltage(7)		0.4	0.7	V
Output Levels					
V_{OL}	LOW-Level Output Voltage	R_L = 1.5kΩ to 3.6V		0.3	V
V_{OH}	HIGH-Level Output Voltage(8)	R_L = 15kΩ to GND	2.8	3.6	V
Leakage Current					
I_{OFF}	Input Leakage Current – Off State		-1	+1	µA
Capacitance					
$C_{I/O}$	I/O Capacitance(7)	Pin to GND		20	pF
Resistance					
Z_{DRV}	Driver Output Impedance(9)	Steady State	34	44	Ω
Z_{IN}	Driver Input Impedance		10		MΩ
R_{SW}	Switch Resistance	I_{SW} = 0 to 10mA		15	Ω
V_{TERM}	Termination Voltage(10,11)	R_{PU} - Upstream Port	3.0	3.6	V

Notes:

7. Not tested in production; value based on characterization.
8. V_{OH} minimum = V_{REG3V3} – 0.2V.
9. Includes external 33Ω ± 1% on both D+ and D- pins to comply with USB2.0.
10. This voltage is available at the VPU and VREG3V3 pins.
11. Minimum voltage is 2.7V in Suspend Mode.

Electrical Characteristics — AI/O Pins AC Characteristics, Full Speed

Unless otherwise noted, values are over the recommended range of supply voltage and operating free air temperature. V_{REG3V3} = 3.0V to 3.6V and V_{IO}= 1.65V to 3.6V.

Symbol	Parameter	Test Conditions	T_A=-40°C to 85°C			Units
			Min.	Typ.(13)	Max.	
Driver Characteristics, FS Mode						
t_{FR}	FS Output Rise Time(13,14)	10% to 90% $\lvert V_{OH} - V_{OL} \rvert$; C_L = 50 pF; *Figure 3*	4		20	ns
t_{FF}	FS Output Fall Time(13,14)	90% to 10% $\lvert V_{OH} - V_{OL} \rvert$; C_L = 50 pF; *Figure 3*	4		20	
t_{FRFM}	FS Rise/Fall Time Match(13,14)	t_R/t_F Excludes First Transition from Idle State	90.0		111.1	%
V_{CRS}	Output Signal Crossover Voltage(13,14)	Excludes First Transition from Idle State	1.3	V_{REG3V3}/2 ±200mV	2.0	V
Driver Characteristics, LS Mode						
t_{LR}	LS Output Rise Time(13,14)	10% to 90% $\lvert V_{OH} - V_{OL} \rvert$; C_L = 50 to 600pF; *Figure 3*	75		300	ns
t_{LF}	LS Output Fall Time(13,14)	90% to 10% $\lvert V_{OH} - V_{OL} \rvert$; C_L = 50 to 600pF; *Figure 3*	75		300	
t_{LRFM}	LS Rise/Fall Time Match(13,14)	t_R/t_F Excludes First Transition from Idle State	80		125	%
V_{CRS}	Output Signal Crossover Voltage(13,14)	Excludes First Transition from Idle State	1.3		2.0	V
Driver Timing, FS Mode						
t_{PLH}	Propagation Delay, FSE0/VO/VPO/ VMO to D+/D-	Input Edge Rates = 2.5ns; *Figure 4*			20	ns
t_{PHL}					20	ns
t_{PHZ}	Driver Disable Delay, OE_N to D+/D-	*Figure 6 , Figure 8*			18	ns
t_{PLZ}					18	ns
t_{PZH}	Driver Enable Delay, OE_N to D+/D-	*Figure 6 , Figure 8*			18	ns
t_{PZL}					18	ns
Driver Timing, LS Mode(12,13)						
Receiver Timing, FS and LS Mode						
t_{PLH}	Differential Receiver Propagation Delay, D+/D- to R_{CV}(15)	C_L = 15pF, *Figure 5, Figure 9*			21	ns
t_{PHL}					21	ns
t_{PLH}	Single-Ended Receiver Propagation Delay, D+/D- to VP, VM	C_L = 15pF, *Figure 5, Figure 9*			18	ns
t_{PHL}					18	ns
SE0 Detection Timing(13)						
t_{PWSE0}	SE0 Pulse Width Detection for INT_N(13)	Suspend, Config,Speed_N=011 VIO=VREG3V3= 3.6V		260		ns

Notes:

12. Edge rates of Low Speed (LS) mode dominate; consequently, there are no propagation delays specified for LS Mode.
13. Not production tested; guaranteed by characterization.
14. Typical conditions are at 25°C and 3.3V.
15. Excludes exiting Suspend or HiZ Mode.

Typical Performance Characteristics

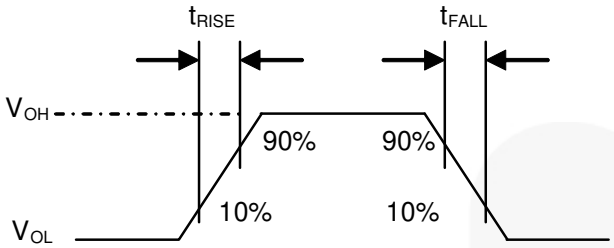


Figure 3. Rise and Fall Time

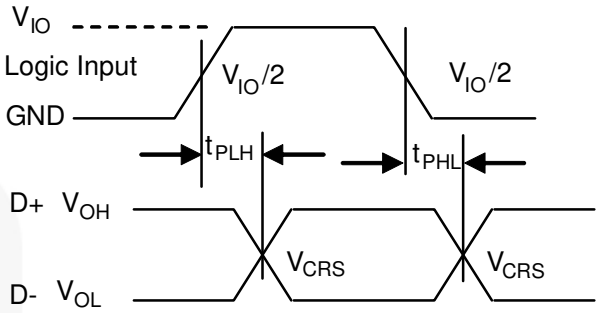


Figure 4. VO/FSE0/VPO/VMO to D+/D-

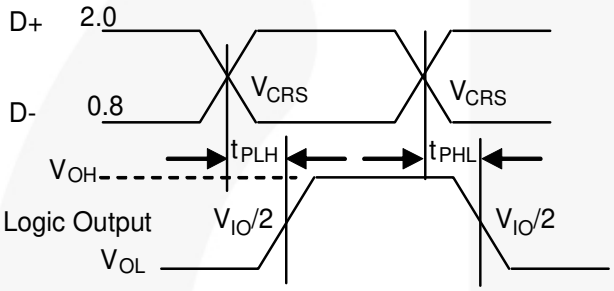


Figure 5. D+/D- to RCV, VP, and VM

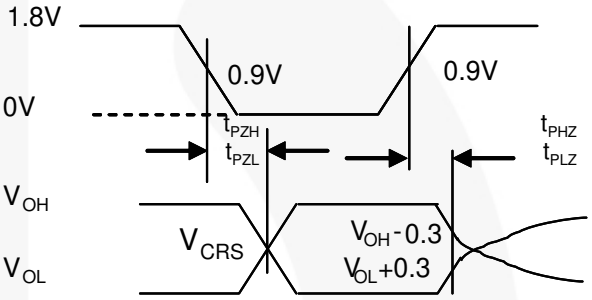
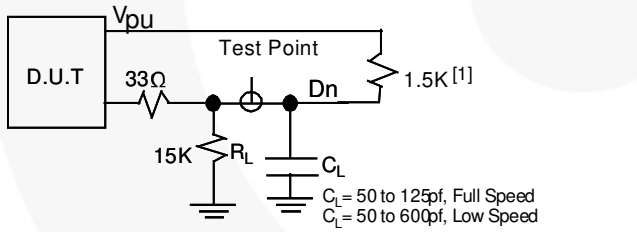


Figure 6. OE_N to D+/D-



[1] FS mode connect to D+; D+ and D- to be matched for R_L /C_L termination.

Figure 7. Load for D+/D-

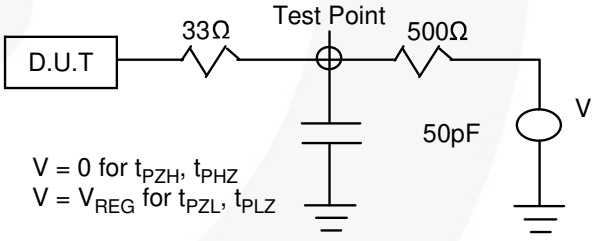


Figure 8. Load for Enable and Disable Time

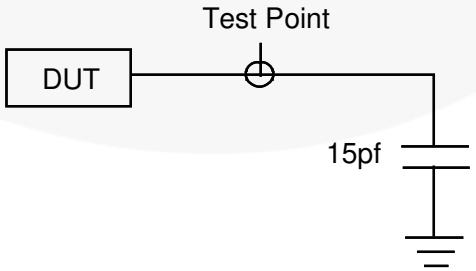


Figure 9. Load for VM, VP, and RCV

Functional Description

The FUSB1500 transceiver is designed to convert CMOS data into USB differential bus signal levels and to convert USB differential bus signals to CMOS data. The FUSB1500 supports the SE Mode interface from the controller and has an extended Control Mode that enables a simplified dedicated charger functionality via a weak pull-up resistance (nominally 125kΩ). This mode is described in Table 4.

To minimize EMI and noise, the outputs are edge-rate controlled with the rise and fall times defined for full-speed (12Mbps) and low-speed (1.5Mbps) data rates. The rise and fall times are balanced between the differential pins to minimize skew.

The FUSB1500 is defined as a self-powered device, or bus-powered where the regulation down to 3.3V is external to the FUSB1500, so it accepts the regulated 3.3V as its supply input. The V_{IO} rail supports I/Os of 1.65V to 3.6V.

If V_{IO} is lost, the pins go into the high-Z state. If V_{IO} is present, but the V_{REG3V3} power supply is lost, the high-Z detection circuit still functions.

USB Mode

Table 1 describes the specific pin functionality when USB Traffic Mode is selected. This is also referred to as normal mode. Table 2 and Table 3 describe the specific truth tables for driver and receiver operating functions.

Table 1. Function Table for USB Mode

OE_N	Hi-Z	D+, D-	RCV	VP/VM	Function
LOW	LOW	Driving & Receiving	Active	Active	Normal Driving (Differential Receiver Active)
HIGH	LOW	Receiving(16)	Active	Active	Receiving
LOW	LOW	Driving	Inactive(17)	Active(18)	Driving during Suspend (Differential Receiver Inactive)

Notes:
16. Signal levels on the D+ and D- pins are determined by external connections and Table 4 (Extended Control Configurations).
17. When in Suspend Mode *(see Table 4 for suspended configurations)*, the differential receiver is inactive and the RCV output is forced LOW. Out-of-suspend signaling (K) is detected via the single-ended receiver outputs VP and VM.
18. The states of VP and VM are functions of signal levels on D+/D- in normal mode.

Table 2. Driver Function (OE_N = L, HiZ= L or Floating) USB Transmit Mode

FSE0/VMO	VO/VPO	FUSB1500
		Data (D+, D-)
LOW	LOW	Differential Logic 0 (01)
LOW	HIGH	Differential Logic 1 (10)
HIGH	LOW	SE0(19) (00)
HIGH	HIGH	SE0(19) (00)

Note:
19. SE0 – Single-Ended Zero.

Table 3. Receiver Function (OE_N = H, HiZ= L or Floating) USB Receive Mode

D+, D-	RCV	VP(20)	VM(20)
Differential Logic 1	HIGH	HIGH	LOW
Differential Logic 0	LOW	LOW	HIGH
SE0	RCV(21)	LOW	LOW
X-(Sharing Mode)(22)	LOW	HIGH	HIGH

Note:
20. VP = VM = HIGH indicates Sharing Mode.
21. Denotes the signal level on output RCV prior to the SE0 event. This level is stable during the SE0 event period.
22. Sharing mode is not a function of D+/D- but is entered when V_{IO} is present and V_{REG3V3} is disconnected.

Functional Description (Continued)

Extended Control Mode

This block of control has a multi-function role; it is used to signal a SE0 detect to the host via INT_N and uses a weak resistor pull-up method for charger detection.

Note that the signaling of SE0 via INT_N is only enabled for the state “011” and all SE0 events can still be decoded from the VP, VM, and RCV outputs.

When the three inputs (SUSPND, CONFIG, and SPEED_N) are not “011,” INT_N is not active; the SE0 detector (RCV = 0) is not active and its latch is set to HIGH. When the “011” is seen on the inputs, the FUSB1500/1501 is waiting for an SE0 event. When the SE0 event (deglitched) is detected, INT_N goes active (HL transition). The host detects this INT_N signal and configures the inputs to the pattern “110” or “010” to keep the 1.5kΩ pull-up enabled. The INT_N signal is then de-asserted and the SE0 detector reset.

If a code other than “010” or “110” is written, the mode configuration is a function as described in Table 4 and the SE0 detector and INT_N are de-asserted to reset states.

When entering the state “111,” which enables the weak pull up resistor for charger detection, the D+/D- drivers are automatically configured to USB receive mode (equivalent to OE_N HIGH).

Figure 10 shows the extended control logic and Table 4 the truth table for the extended control.

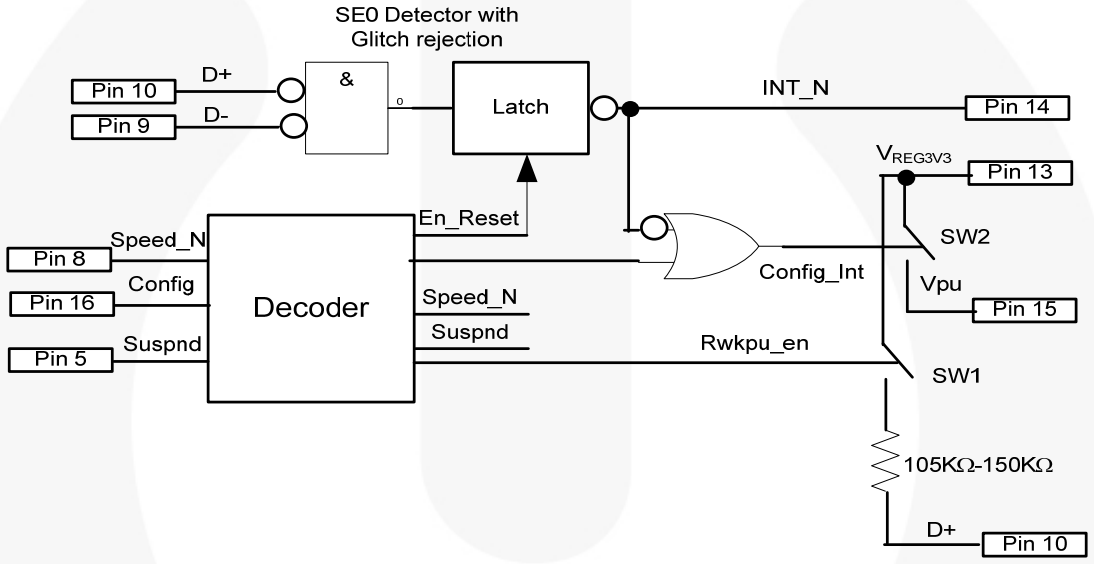


Figure 10. Extended Control Function

Table 4. Extended Control

Hi-Z	SUSPND	CONFIG	SPEED_N	Function		
0	0	0	0	No 1.5kΩ Pull-up	FS	USB Mode, Default State
0	0	1	0	1.5kΩ Pull-up	FS	USB Mode
0	0	0	1	No 1.5kΩ Pull-up	LS	USB Mode
0	0	1	1	Pull-up On After Detecting SE0	FS	Suspend, Conditional Pull-up
0	1	0	0	No 1.5kΩ Pull-up	FS	Suspend
0	1	1	0	1.5kΩ Pull-up	FS	Suspend
0	1	0	1	No 1.5kΩ Pull-up	LS	Suspend
0	1	1	1	No 1.5kΩ Pull-up, 125kΩ Pull-up Connected		USB Rx Mode & RWPU On
1	X	X	X	VP, VM, D+, D-, RCV High Impedance, SW1 and SW2 Open		Hi-Z Mode

Functional Description (Continued)

Power Supply Configurations and Options

The three modes of power-supply operation are:

- *Normal Mode* – The VIO and VREG3V3 pins are connected. V_{IO} is an independent voltage source (1.65 to 3.6V) that is a function of the external circuit configuration.
- *Disable Mode* – VIO is not connected; VREG3V3 is connected. In this mode, the D+, D- pins are three-state and the device enters low-power (suspended) state upon detection of V_{IO} lost.
- *Hi-Z Mode* – When the Hi-Z pin is pulled HIGH, with VREG3V3 powered, the RCV/VP/VM interface can be used to access the Baseband for production test programming. VP/VM/RCV are in high impedance states.
- *Sharing Mode* – V_{IO} is the only supply connected. In this mode, the D+ and D- pins are three-state and the FUSB1500 allows external signals up to 3.6V to share the D+ and D- bus lines. Internally, the circuitry limits leakage from the D+ and D- pins (maximum 10μA) and V_{IO} such that device is in low-power (suspended) state. The VP and VM pins are driven HIGH and RCV is forced LOW as an indication of this mode. Can be used for production test programming via D+/D-. to UART or Baseband processor. HiZ is to be Low or Floating to ensure VP/VM/RCV is signaled to processor.

A summary of the supply configurations is described in Table 5.

Table 5. Power Supply Mode Configuration Options

Pin	Hi-Z	Sharing	Disable	Normal
VREG3V3	3.3V Externally Supplied	Not Connected	Connected	3.3V Externally Supplied
VIO	1.65 - 3.6V Source	1.65-3.60V Source	Not Connected	1.65V- 3.60V Source
VPU	Three-State (Off)	Three-State (Off)	Three-State (Off)	Function of Mode Set-up
D+, D-	Three-State	Three-State	Three-State	Function of Mode Set-up
VP / VM	Three-State	HIGH	Invalid[23]	Function of Mode Set-up
RCV	Three-State	LOW	Invalid[23]	Function of Mode Set-up
VPO, VMO, SPEED_N,OE_N, SUSPND, CONFIG	Inputs	Inputs	Three-State	Function of Mode Set-up
HiZ	HIGH	LOW or Floating	Three-State	LOW or Floating
INT_N	HIGH	HIGH	Three-State	Function of Mode Set-up

Note:
23. Three-state or driven LOW.

Single Ended Zero Detection Timing

The SE0 detection logic is activated when entering the state “011” (SUSPND, CONFIG, and SPEED_N) and the logic waits to detect an SE0 event. Since the FUSB1500 can also be used as an LS host device, it is important to ensure that the t_{LST} time for the USB2.0 specification is met. t_{LST} is the minimum time to not interpret LS differential signaling as an SE0 and is 210ns in duration. Similarly for FS differential signaling, there is a time period, t_{FST} time, of 14ns.

Seeing an SE0 for greater than t_{LST} results in the INT_N pin toggling LOW. The FUSB1500 is designed for 260ns (typical).

Exiting HiZ or Suspend Mode Timing

As the RCV path is required to maintain the previous state through an SE0 event, there is the possibility when exiting HiZ or Suspend Mode to have the previous result stored. The transition through the SE0 decode logic is such that software should ignore RCV for at least 100ns when exiting HiZ mode to ensure the correct D+/D- state is available on the RCV output.

Hi-Z and Sharing Mode for Production Test

When in production test, to gain access to the processor or UART, the D+/D- pins can be used (Sharing Mode) or the RCV/VP/VM interface of the host side of the FUSB1500 (Hi-Z). If sharing the D+/D- pins then VREG3V3 is unpowered and the processor is signaled this mode via the VP/VM outputs being pulled High and the RCV pin is pulled Low.

If the RCV/VP/VM interface is to be used by production test then Hi-Z is pulled High, with VREG3V3 remaining powered.

Figure 11 indicates the production test scenarios.

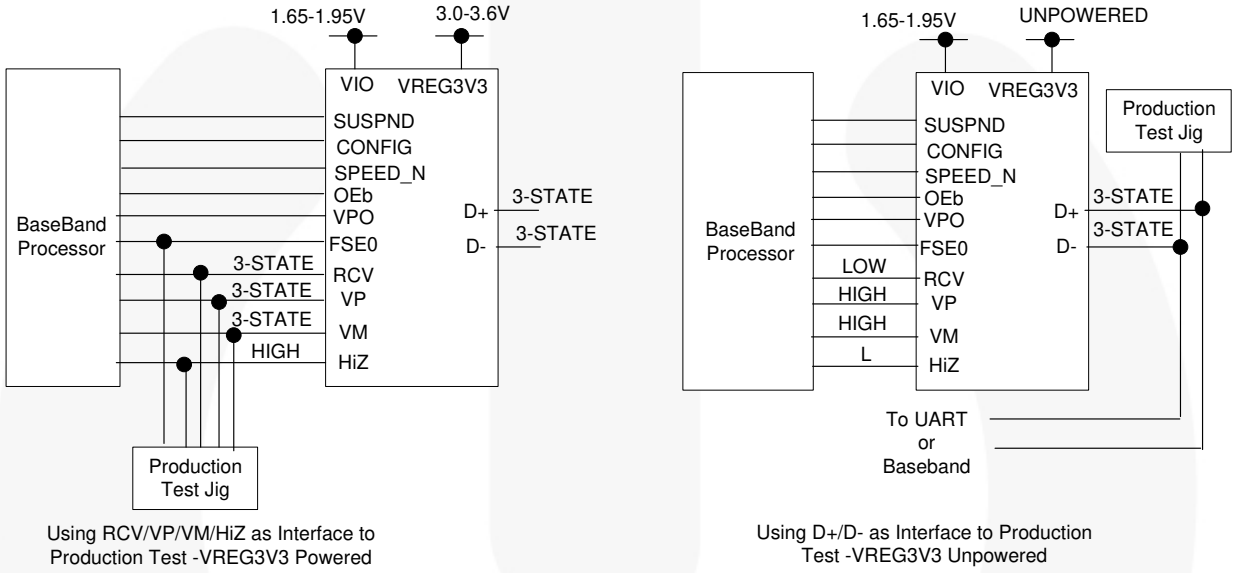
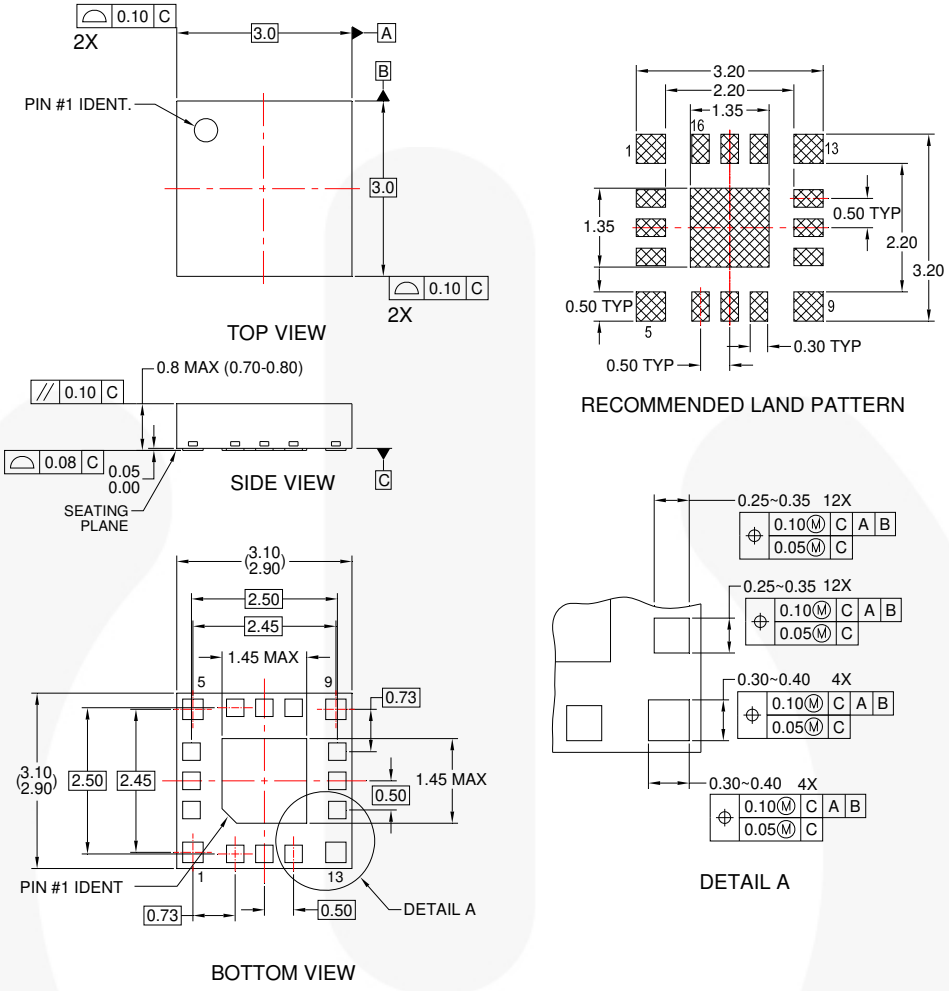


Figure 11. Production Test Using Hi-Z or Sharing Mode

Physical Dimensions



NOTES:

A. SIMILAR TO JEDEC REGISTRATION MO-217,

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

D. LANDPATTERN RECOMMENDATION IS PER
FSC INTERNAL DESIGN

E. DRAWING FILENAME: MLP16HBrev4

Figure 12. 16-Pin, Molded Leadless Package (MLP), JEDEC MO217 Equivalent, 3mm Square

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