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# FUSB2805

## USB2.0 High-Speed OTG Transceiver with ULPI Interface

### Features

- Complies with USB 2.0, OTG Rev 1.3 Supplement, and ULPI Rev 1.1 Specifications
- Supports 480 Mbps, 12 Mbps, and 1.5 Mbps USB2.0 Speeds
  - Integrated Termination Resistors Meet USB2.0 Resistor ECN
  - Integrated Serializer and Deserializer
  - Insertion and Removal of Stuffed Bits as Appropriate
  - USB Clock and Data Recovery to  $\pm 150$ ppm
- Supports USB OTG Rev 1.3 Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- 15 kV ESD, IEC 61000 Board Level, Air Gap

### Applications

- Set-Top Box Video Camera, MP3 Player
- Cell Phone, Digital Still Camera, PDA
- DVD Recorder, Scanner, Printer

### Description

The FUSB2805 is a UTMI+ Low-Pin Interface (ULPI) USB2.0 OTG transceiver. It is compliant with the Universal Serial Bus Specification Rev 2.0 (USB2.0), the ULPI Specification Rev. 1.1, and the On-The-Go (OTG) supplement to USB2.0, Rev. 1.3.

The FUSB2805 is optimized to connect the USB2.0 host, peripheral, or OTG-controller to the USB connector via the ULPI link. Data can be transmitted and received at high speed (480 Mbps), full speed (12 Mbps), and low speed (1.5 Mbps) through a 12-bit (SDR) interface.

### Related Resources

*UTMI+ Low Pin Interface Specification (ULPI), Revision 1.1, October 20, 2004.* <http://www.ulpi.org>

*UTMI+ Specification, Revision 1.0, February 22, 2004.* <http://www.ulpi.org>

*For additional performance information, please contact [analogswitch@fairchildsemi.com](mailto:analogswitch@fairchildsemi.com).*

### Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FUSB2805MLX	FUSB2805	-40 to +85°C	32-Terminal, Molded Leadless Package (MLP), Quad, JEDEC MO-220

### Block Diagram

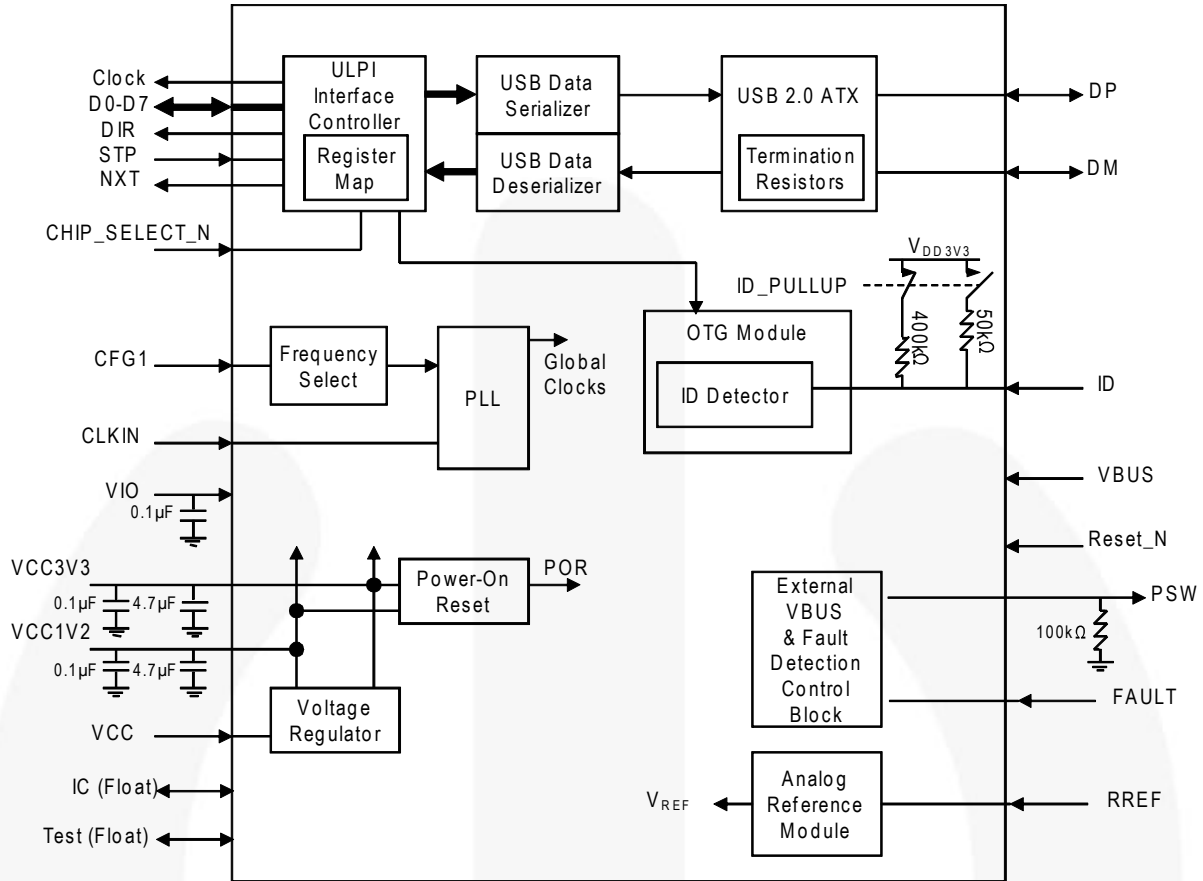


Figure 1. Functional Block Diagram

### Pin Configuration

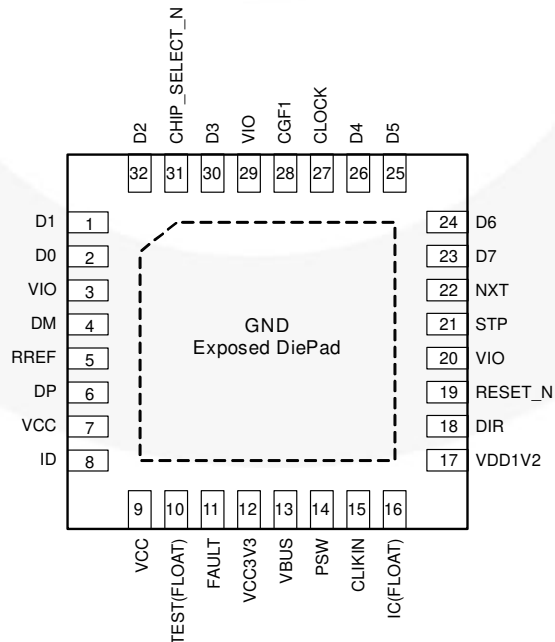


Figure 2. Pin Assignments (Through View)

## Pin Definitions

Symbol	Type <sup>(1)</sup>	Description
Chip Select_N	I	Active LOW. HIGH – ULPI pin three-stated; LOW – ULPI operates normally. TTL compatible; CMOS input with hysteresis.
R <sub>REF</sub>	AI/O	Resistor reference. Connect through 12 kΩ ±1% to GND.
DM	AI/O	USB D- pin. USB mode: data minus (D-) pin of the USB cable.
DP	AI/O	USB D+ pin. USB mode: data plus (D+) pin of the USB cable.
FAULT	I	FAULT is used to signal a V <sub>BUS</sub> over-current/over-voltage condition from an external SMPS or power management IC. The link must enable this function via the ExternalVbusFault register bit and the polarity must be set via the ExternalVbusActiveLow register bit.
ID	I	Identification (ID) pin of the micro-USB cable. TTL; if not used, connect to 3V3.
VCC	P	Input supply voltage or battery source.
PSW	O	Controls an external, active HIGH, V <sub>BUS</sub> power switch/charge pump and/or an SMPS charger IC. An external 100 kΩ pull-down resistor is required. Open source, slew-rate-controlled output; this pin is referenced to V <sub>CC3V3</sub> .
V <sub>BUS</sub>	AI/O	Should be connected to the VBUS pin of the USB cable. Leave open circuit if not used. An internal 90 kΩ ±11% pull-down resistor is present on this pin.
V <sub>CC3V3</sub>	P	3.3 V regulator output requiring capacitors. Internally powers OTG, analog core, and ATX.
CLKIN	I	Clock input; frequency depends on the CFG1 pin. This is a digital input buffer, not analog for a crystal.
I.C.	I/O	Internally connected; float pin.
TEST	I/O	Internally connected; float pin.
CFG1	I	Configures the clock frequency; 0: input is 19.2 MHz. 1: input is 26 MHz.
V <sub>DD1V2</sub>	P	1.2 V regulator output requiring capacitors. Internally powers the digital core and analog core.
V <sub>IO</sub>	P	Input I/O supply rail; 0.1 μF capacitor connected to power input.
Reset_N	I	Connect to V <sub>IO</sub> when not used. Resets the transceiver; active LOW.
GND	P	Connect to ground.
DIR	O	ULPI direction output signal.
STP	I	ULPI stop input signal; CMOS input.
NXT	O	ULPI next output signal.
D7	I/O	ULPI data pin 7; three-state output.
D6	I/O	ULPI data pin 6; three-state output.
D5	I/O	ULPI data pin 5; three-state output.
D4	I/O	ULPI data pin 4; three-state output.
D3	I/O	ULPI data pin 3; three-state output.
D2	I/O	ULPI data pin 2; three-state output.
D1	I/O	ULPI data pin 1; three-state output.
D0	I/O	ULPI data pin 0; three-state output.
CLOCK	O	60 MHz clock output when digital 19.2 MHz (or 26 MHz) clock is applied; Push-pull output.

### Notes:

- I=input; O=output; I/O=digital input/output; OD=open-drain output; AI/O=analog input/output; P=power or ground.
- Per USB2.0, below a supply of 2.97 V, USB full-speed and low-speed transactions are not guaranteed; although some devices may continue to function with the FUSB2805 at the lower supply rail.

## Functional Description

### ULPI Interface Controller

The FUSB2805 provides a 12-pin interface (SDR) compliant with the UTMI+ Low-Pin Interface (ULPI) specification, revision 1.1. This interface must be connected to the USB link controller.

The ULPI controller provides the following functions:

- ULPI-compliant interface and register set
- Full control of USB peripheral, host, and On-The-Go functionality
- Prioritizes USB receive data, USB transmit data, interrupts, and register operations
- Parses USB transmit and receive data
- Controls the  $V_{BUS}$  external source
- $V_{BUS}$  monitoring, charging, and discharging
- Low-power mode
- 6- and 3-pin serial modes
- Generates RX CMDs (status updates)
- Maskable interrupts
- Control over the ULPI bus state

### USB Serializer and Deserializer

The USB data serializer prepares data for transmitting onto the USB bus. To transmit data, the USB link controller sends a transmit command and data on the ULPI bus. The serializer performs parallel-to-serial conversion, bit stuffing, and Non Return to Zero, Invert (NRZI) encoding. For packets with a PID, the serializer adds a SYNC pattern to the start of the packet and an EOP pattern to the end of the packet. When the serializer is busy and cannot accept more data, the ULPI interface controller de-asserts NXT.

The USB data deserializer decodes data received from the USB bus. When data is received, the deserializer strips the SYNC and EOP patterns, if applicable, then performs serial-to-parallel conversion, NRZI decoding, and bit unstuffing on the data payload. The ULPI interface controller sends the data to the USB link controller by asserting DIR, then asserting NXT whenever a byte is ready. The deserializer also detects various receive errors, including bit-stuff errors, elasticity buffer under-run or over-run, and byte-alignment errors.

### USB 2.0 ATX

The USB 2.0 ATX block is an analog front-end containing the circuitry needed for transmitting, receiving, and terminating the USB bus in high speed (HS), full speed (FS), and low speed (LS); for USB peripheral, host, and OTG implementations; per the USB2.0 specification and its relevant supplements. The following circuitry is included:

- Differential drivers for transmitting data at HS, FS, and LS
- Differential receiver and single-ended receivers for receiving data at HS, FS, and LS
- Squelch circuit to detect HS bus activity
- HS disconnect detector
- 45  $\Omega$  HS bus terminations on DP and DM for peripheral and host mode
- 1.5 k $\Omega$  pull-up resistor on DP for FS for peripheral mode only (DM resistor pull up for LS peripheral is not supported since FUSB2805 is HS capable.)
- 15 k $\Omega$  bus terminations on DP and DM for host mode only

### PLL and Clock Generation

The FUSB2805 has a built-in Phase Locked Loop (PLL) for clock generation.

The PLL takes the square wave clock (19.2 MHz or 26 MHz) from the CLKIN and multiplies or divides it into various frequencies for internal use.

From the clock source, the PLL produces the following frequencies:

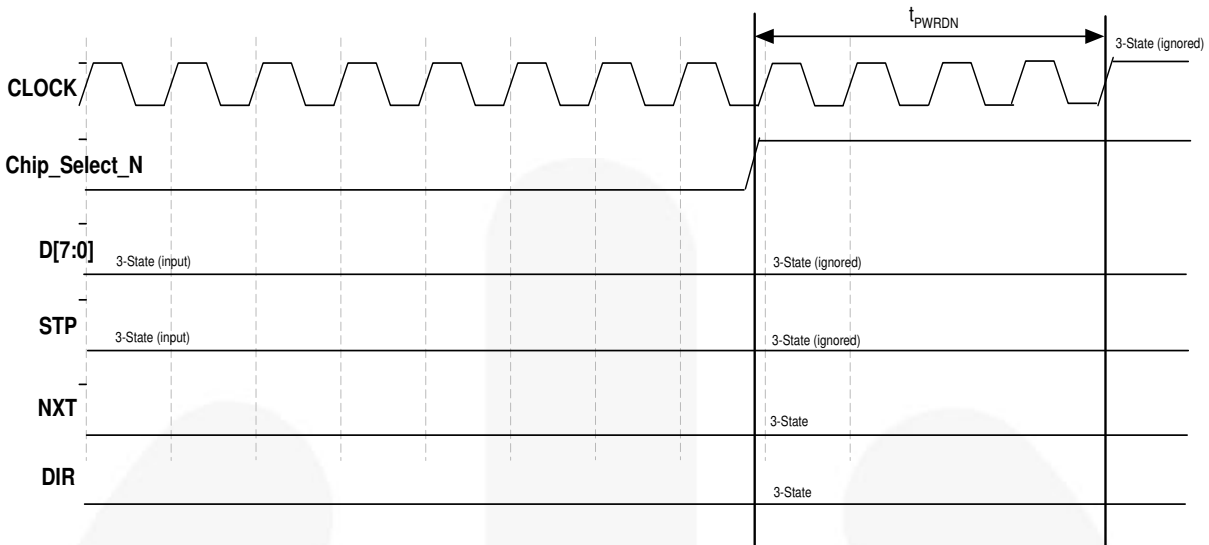
- 60 MHz clock for the ULPI interface controller
- 1.5 MHz for low-speed USB data
- 12 MHz for full-speed USB data
- 480 MHz for high-speed USB data

### Interface Protection

To prevent incorrect activity when the ULPI interface is not correctly driven by the link, such as when the link controller powers up slower than the FUSB2805, there is a weak pull-up resistor on the STP pin.

If the STP is unexpectedly HIGH at any time, the FUSB2805 protects the ULPI interface by enabling weak pull-down resistors on D[7:0].

This interface protection scheme can be disabled by setting the INTF\_PROT\_DIS bit to 1b (INTF\_CNTRL[7]).



**Figure 3. ULPI Behavior with Chip\_Select\_N as a Power-Down Control Signal**

### Power Down Using Chip\_Select

When CHIP SELECT\_N is de-asserted (HIGH), the FUSB2805 three-states the ULPI interface pins and powers down the internal circuitry. If CHIP SELECT\_N is not used as a power-down control signal, it is tied to a LOW. Figure 3 shows the ULPI interface behavior when CHIP SELECT\_N is asserted and subsequently de-asserted.

After the  $t_{PWRDN}$  duration, the CLOCK output enters three-state and is ignored by the link.

### Power-On Reset (POR)

The power supply for the internal regulators is  $V_{CC}$ . This supply is fed into the 3.3 V and 1.2 V regulators. The output of the 3.3 V regulator is  $V_{CC3V3}$ . The 1.2 V regulator generates  $V_{DD1V2}$ .

During the power-up stage, the POR is held in a stable state to ensure that the digital logic does not operate the I/O or any analog circuit in such a way that may be damaging to the rest of the system.

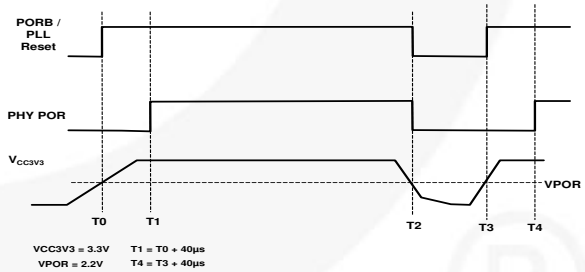
The output of the POR block, PORB (internal signal), should be 1'b0 during the power supply ramping period. Once the power supplies have completely ramped, PORB should be de-asserted. This signal is driven into the 19.2 / 26 MHz to 12 MHz PLL. The POR signal

(active HIGH reset) in the USB OTG PHY block must remain asserted for no less than 40  $\mu$ s.

PORB de-assertion is determined via a comparator on  $V_{CC3V3}$  with a POR trigger threshold,  $V_{POR}$ , of 2.0 V.

Figure 4 illustrates how PORB should be pulsed based on the voltage level of  $V_{CC3V3}$ . This diagram also shows what the POR should do to PORB when  $V_{CC3V3}$  drops below  $V_{POR}$  for any length of time.

When CLOCK starts toggling after power up, the USB link controller must issue a reset command over the ULPI bus to ensure correct operation.



**Figure 4. Power-On Reset Sequence**

## OTG Module

The OTG module contains several sub-blocks that provide the functionality required by the USB On-The-Go Rev. 1.3 supplement. Specifically, it provides the following circuits:

- ID detector to sense the ID pin of the micro-USB cable. The ID pin dictates which device is initially configured as the host and which is configured as the peripheral.
- $V_{BUS}$  comparators to determine the  $V_{BUS}$  voltage level. This is required for Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).
- Resistors to temporarily charge and discharge  $V_{BUS}$ . This is required for SRP.

### ID Detector

Detects which end of the mini-USB (or micro-USB) cable is plugged in. The ID detector must first be enabled by setting the ID\_PULLUP register bit to 1b. If the FUSB2805 senses a value on ID different from the previously reported value, an RX CMD status update is sent to the USB link controller or an interrupt is asserted.

If the micro-B end of the cable is plugged in, the FUSB2805 reports that ID\_GND is logic 1 and the USB link controller changes to peripheral mode.

If the micro-A end of the cable is plugged in, the FUSB2805 reports that ID\_GND is logic 0 and the USB link controller changes to host mode.

The ID pin has a weak pull-up resistor (400k $\Omega$ ) to avoid floating conditions. This resistor is connected when ID\_PULLUP register bit is 0. If the application does not use the ID pin, tie this pin to  $V_{CC3V3}$ .

### $V_{BUS}$ Comparators

The FUSB2805 provides three comparators for detecting the  $V_{BUS}$  voltage level, as listed in Table 9 and Table 12. The comparators are as follows:

#### $V_{BUS}$ -Valid Comparator

This comparator is used by an A-device (or host) to determine whether or not the voltage on  $V_{BUS}$  is at a valid level for operation. The minimum threshold for the  $V_{BUS}$  valid comparator is 4.4 V. Any voltage on  $V_{BUS}$  below this threshold is considered a fault. During power-up, the comparator output is ignored.

#### Session-Valid Comparator

The session-valid comparator is a TTL-level input that determines when  $V_{BUS}$  is high enough for a session to start. Both the A-device and the B-device use this comparator to detect when a session is being started. The A-device also uses this comparator to determine when a session is completed. The session valid threshold is between 0.8 V to 2.0 V.

#### Session-End Comparator

The session-end comparator determines when  $V_{BUS}$  is below the B-device session-end threshold of 0.2 V to 0.8 V. The B-device uses this threshold to determine when a session has ended.

#### SRP Charge and Discharge Resistors

The FUSB2805 provides on-chip resistors for short-term charging and discharging of  $V_{BUS}$ . These are used by the B-device to request a session, prompting the A-device to restore  $V_{BUS}$  power. First, the B-device verifies that  $V_{BUS}$  is fully discharged from the previous session by setting the DISCHARGE\_VBUS register bit to 1b and waiting for SESS\_END to be 1b. Then the B-device charges  $V_{BUS}$  by setting the CHARGE\_VBUS register bit to 1b. The A-device detects that  $V_{BUS}$  is charged above the session-valid threshold and starts a session by turning on  $V_{BUS}$  power.

#### Analog Reference Module

The analog reference module provides stable internal voltage and current references for biasing internal analog circuitry. This module requires an accurate external reference resistor. A value of 12 k $\Omega$   $\pm$ 1% resistor is required between the R\_REF pin and GND.



## Detailed Description of Pins

### D0 to D7

D0 to D7 are bi-directional ULPI data bus pins. The USB link controller must drive D0-D7 LOW when the ULPI bus is idle (DIR is LOW). When the link has data to transmit to the FUSB2805, it drives a non-zero value.

The data bus can be re-configured to carry different data types. There are four modes of the data bus:

- Synchronous mode: default is SDR mode<sup>(3)</sup>, with the 8-bit data bytes being synchronous to the rising edge of CLOCK.
- Low-power mode: carries asynchronous line state and  $V_{BUS}$  information.
- 3-pin serial mode: carries asynchronous 3-pin FS/LS serial signaling.
- 6-pin serial mode: carries asynchronous 6-pin FS/LS serial signaling.

Data pins can also be three-stated by driving `chip_select_N` HIGH.

#### Note:

3. DDR is not supported by the FUSB2805.

### $V_{IO}$

$V_{IO}$  is the input power pin that sets the I/O voltage level.  $V_{IO}$  powers the on-chip pads of the following pins:

- CLOCK
- DIR
- STP
- NXT
- D0-D7
- RESET\_N
- CFG1

### $R_{REF}$

Resistor reference analog I/O pin. A  $12\text{ k}\Omega \pm 1\%$  resistor is required.

### DP and DM

When in USB mode, the DP pin functions as USB data plus line; the DM pin functions as USB data minus line.

The DP and DM pins should be connected to the D+ and D- pins of the USB receptacle.

### FAULT

This input pin is used by an external SMPS or power management IC to signal an over-current or over-voltage fault condition. This is applicable in OTG host where PSW is used to control driving  $V_{BUS}$  or signaling for higher charging currents to an OTG SMPS management IC, as shown in Figure 5.

### ID

For OTG implementation, the ID (identification) pin is connected to the ID pin of the mini-USB (or micro-USB) receptacle. As defined in the OTG specification, the ID pin dictates the initial role of the link controller. If ID is detected as HIGH, the link controller must assume the role of peripheral. If ID is detected as LOW, the link controller must assume the host role. Roles can be swapped later using Host Negotiation Protocol (HNP).

The FUSB2805 provides an internal pull-up resistor to sense the value of the ID pin. The pull-up resistor, with a value of  $50\text{ k}\Omega$ , must first be enabled by setting the `ID_PULLUP` register bit to 1b. If the value on ID has changed, the FUSB2805 sends an RX CMD or interrupt to the link controller by time  $t_{ID}$ . If the link controller does not receive any RX CMD or interrupt by  $t_{ID}$ , then the ID value has not changed.

To avoid a floating ID pin, a  $400\text{ k}\Omega$  resistor pull-up is switched in when `ID_PULLUP` register bit is set to 0b.

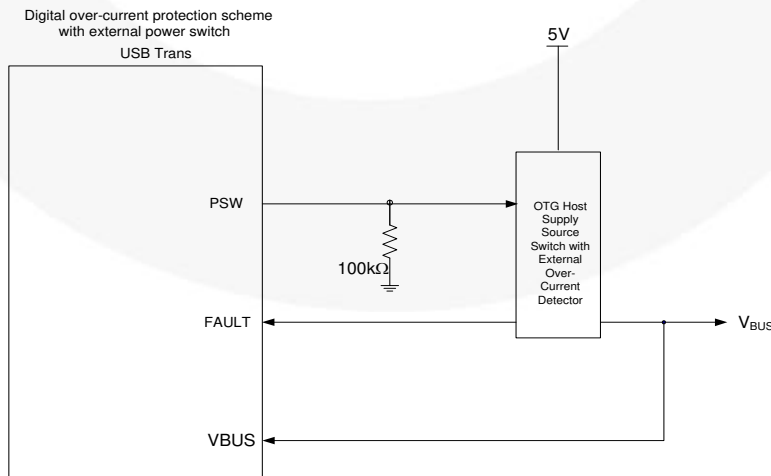


Figure 5. Digital Over-Current Detection Scheme

**V<sub>CC</sub>**

V<sub>CC</sub> is the main input supply voltage for FUSB2805. The FUSB2805 operates correctly when V<sub>CC</sub> is between 2.7 V and 4.5 V. The maximum transients that should be seen on V<sub>CC</sub> are 5.5V for a maximum of 5ms. A 100nF decoupling capacitor is preferred.

**PSW**

This is an active-HIGH, open-source, power-switch analog output. This pin can be connected to an external V<sub>BUS</sub> switch or an external charge pump enable circuit to control the external V<sub>BUS</sub> power source. If the link controller is in host mode, this can be set via the DRV\_VBUS and DRV\_VBUS\_EXT bits in the OTG control register to logic 1. The FUSB2805 drives PSW to HIGH to enable the external V<sub>BUS</sub> supply. If the link controller detects an over-current condition (V<sub>BUS\_valid</sub>=0), it should disable the external V<sub>BUS</sub> supply by setting DRV\_VBUS\_EXT to 0b. An external 100 kΩ pull-down resistor is used.

In addition, the polarity of the signal that controls PSW can be changed via the INTF\_CTRL register.

**V<sub>BUS</sub>**

This power I/O pin acts as input to the V<sub>BUS</sub> comparators and over-current detector.

When the DRIVE\_VBUS bit of the OTG control register is set to 1b, an external V<sub>BUS</sub> source tries to drive V<sub>BUS</sub> to a voltage of 4.4 V to 5.25 V with an output current capability of at least 8 mA.

**V<sub>CC3V3</sub> and V<sub>DD1V2</sub>**

Regulator output voltages. These supplies are used to internally power digital and analog circuits.

**CLKIN**

Clock input pin; CLKIN is the digital clock input. The allowed frequencies on CLKIN are 19.2 MHz and 26 MHz. The frequency tolerance required by the clock is 50 ppm. The link controller requires a 60 MHz clock from the FUSB2805. This is generated from the PLL, which uses the CLKIN as the input clock.

- 19.2 MHz – CFG1 set to LOW
- 26 MHz – CFG1 set to HIGH

**CHIP\_SELECT\_N**

Active LOW chip-select pin. When asserted HIGH; D[0-7], CLOCK, DIR, and NXT pins are three-stated and ignored and all internal circuits are powered down, including the regulator. When LOW, the FUSB2805 wakes up and the ULPI pins operate normally.

**IR**

Direction output pin. This pin is synchronous to the rising edge of CLOCK and controls the direction of the data bus. By default, the FUSB2805 holds DIR LOW, causing the data bus to be an input. When DIR is LOW, the FUSB2805 listens for data from the link controller. The FUSB2805 pulls DIR HIGH only when it has data to send to the link, which is for one of two reasons:

1. To send USB receive data, RX CMD status updates, and register-read data to the link controller.
2. To block the link controller from driving the data bus during power up, reset, and low-power mode (suspend).

The DIR pin can also be three-stated when Chip\_Select\_N is de-asserted HIGH.

**STP**

Stop input pin. This signal is synchronous to the rising edge of CLOCK. The link must assert STP to signal the end of a transmit packet or a register-write operation. When DIR is asserted, the link controller can optionally assert STP to abort the FUSB2805, causing it to de-assert DIR in the next clock cycle.

**NXT**

Next data output pin. This signal is synchronous to the rising edge of CLOCK. The FUSB2805 holds NXT LOW by default. When DIR is LOW and the link is sending data, NXT is asserted to tell the link to provide the next data byte. When DIR is HIGH and the FUSB2805 is sending data to the link, NXT is asserted to tell the link another valid byte is on the bus. NXT is not used for register read data or the RX CMD status update.

The NXT pin can also be three-stated when Chip\_Select\_N is de-asserted HIGH.

**CLOCK**

This is the 60MHz interface clock for synchronizing the ULPI bus. It is configured as an output. Being a 12-pin interface implementation, all the ULPI signals are synchronous to the rising edge of CLOCK. The FUSB2805 accepts a digital clock input and outputs the 60MHz to the link.

**GND**

The global ground signal acts as a ground to all circuits in the FUSB2805.

**Reset\_N**

Reset\_N is an active LOW reset signal with V<sub>IO</sub> voltage. Tie to V<sub>IO</sub> 1.8 V if not used. Typically tied to the power-on reset signal of the product.

## Modes of Operation

### ULPI Modes

The ULPI bus can be programmed to operate in four different modes and a power-down mode. Each mode re-configures the signals on the data bus. Setting more than one mode leads to undefined behavior.

### Synchronous Mode

This is the default mode. On power-up and when CLOCK is stable, the FUSB2805 enters synchronous mode.

In synchronous mode, the link controller must synchronize all ULPI signals to CLOCK, meeting the setup and hold times defined in the Dynamic Characteristics tables.

This mode is used by the link controller to perform the following tasks:

- Detect high-speed handshake (chirp)
- Transmit and receive USB packets
- Read and write to registers
- Receive USB status updates (RX CMDs) from FUSB2805

*Please refer to section 3.8 of the ULP Rev. 1.1 specification for further details.*

### Low-Power Mode

When the USB is idle, the link controller can place the FUSB2805 into low-power mode (also known as “suspend” mode). To enter low-power mode, the link controller clears the SUSPENDM bit in the function control (FUNC\_CTRL) register to 0b.

During low-power mode, the FUSB2805 provides line state and interrupt information on the data bus for the link controller to monitor basic USB states and draws less than 200  $\mu$ A from the  $V_{CC}$  supply.

In addition, during low-power mode, the clock on CLKIN may be stopped; but it must be restarted before asserting STP to exit low-power mode.

Once in low-power mode, the FUSB2805 must remain in low-power mode for a minimum of 120 clock cycles (or 2  $\mu$ s). After the 2  $\mu$ s delay, low-power mode may be exited by asserting the STP signal. The FUSB2805 then issues an RXCMD to the link if a change was detected in any interrupt source and the change still exists. An RXCMD may not be sent if the interrupt condition is removed before exiting.

In low-power mode, the data bus assignments are changed to those described in Table 1.

**Table 1. Signal Mapping on ULPI Bus During Low-Power Mode**

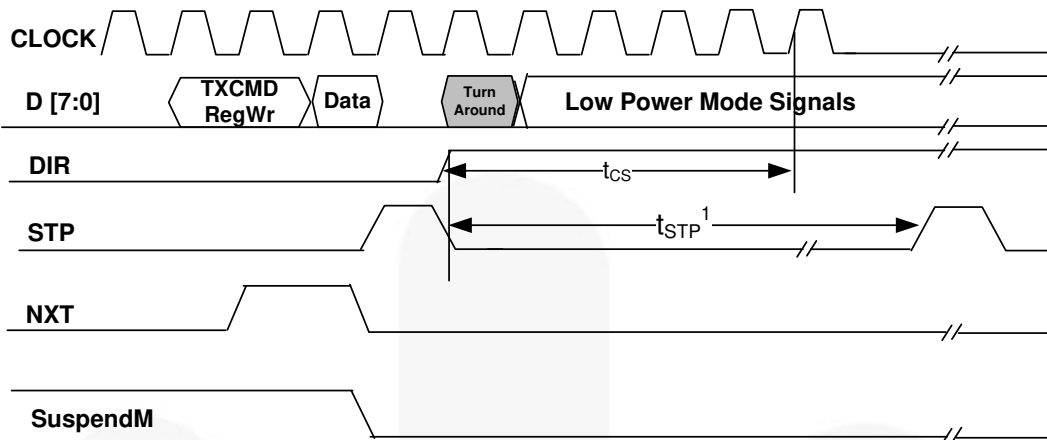
Signal	Maps To	Direction	Description
LINSTATE0	D0	Out	Combinatorial LINSTATE0 directly driven by the analog receiver
LINSTATE1	D1	Out	Combinatorial LINSTATE1 directly driven by the analog receiver
RESERVED	D2	Out	Reserved; the FUSB2805 drives this pin LOW
INT	D3	Out	Active-HIGH interrupt signal; asserted and latched whenever any unmasked interrupt occurs
RESERVED	D[7:4]	Out	Reserved; the FUSB2805 drives these pins LOW

### Entering Low-Power Mode

The link sets SuspendM=0b (in Function Control Register) to place the FUSB2805 into low-power mode. The CLOCK may be stopped a minimum of five (5) cycles after the FUSB2805 accepts the register write data as described in Figure 6. When entering low-power mode, the FUSB2805 asserts DIR

and holds NXT LOW. There is one cycle of data bus turnaround provided after the assertion of DIR, during which the value of D[7:0] is not valid. Upon completion of the turnaround cycle the FUSB2805 begins driving the signals as described in Table 1.

**ULPI Signals**



Note: The second STP pulse indicates the exit of low-power (suspend) mode

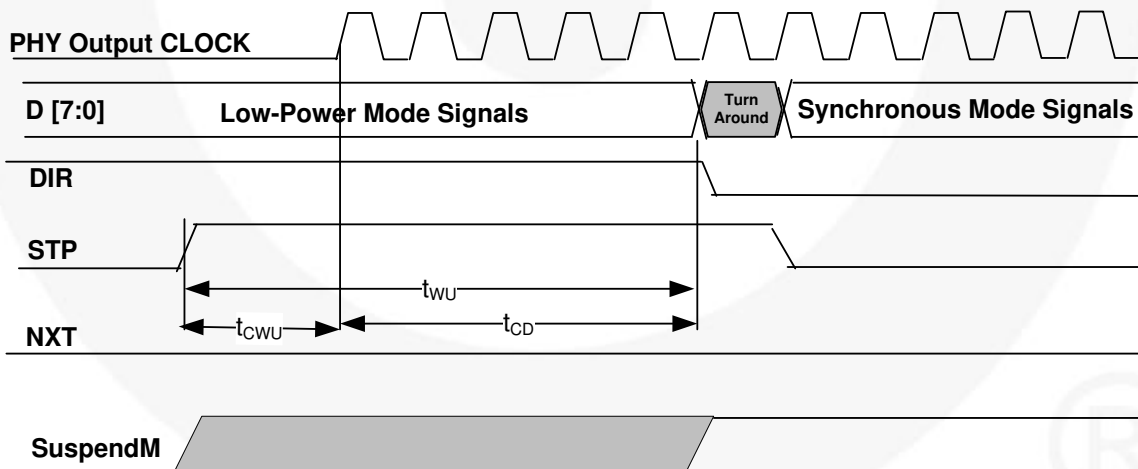
**Figure 6. Entering Low-Power Mode**

**Exiting Low-Power Mode**

If the FUSB2805 has been in suspend at least 2  $\mu$ s, the link may signal the FUSB2805 to exit low-power mode by asynchronously asserting STP. The FUSB2805 immediately starts to wake up its internal circuitry. Upon meeting the ULPI timing requirements the FUSB2805 then de-asserts DIR, ensuring a minimum of 5 cycles of CLOCK have been driven before de-asserting DIR and

setting SuspendM=1b (in Function Control Register). The link de-asserts STP in the cycle following the de-assertion of DIR. There is one cycle of data bus turnaround provided after the assertion of DIR, during which the value of D[7:0] is not valid. Upon completion of the turnaround cycle the FUSB2805 begins driving the signals as described in Table 1.

**ULPI Signals**



**Figure 7. Exiting Low-Power Mode when FUSB2805 Provides Output CLOCK**

**6-Pin Full-Speed / Low-Speed Serial Mode**

This mode of operation is provided for links that contain legacy FS/LS functionality and enables a cost-effective upgrade path to HS functionality.

To enter 6-pin serial mode, the link controller sets the 6PIN\_FLSL\_SERIAL bit in the interface control register to logic 1. To exit 6-pin serial mode, the link controller asserts STP.

An INT signal is also provided to inform the link of USB events. If the link requires CLOCK to be running during 6-pin serial mode, the CLK\_SUSPENDM register bit must be set to logic 1b before entering 6-pin serial mode.

The FUSB2805 requires CLKIN to be kept running when in 6-pin mode. In 6-pin serial mode, the data bus assignments are changed to those described in Table 2. Examples of the signaling of data packets are shown in Figure 22.

**Table 2. Signal Mapping on ULPI Bus During 6-Pin Serial Mode**

Signal	Maps To	Direction	Description
TX_ENABLE	D0	In	Active-HIGH transmit enable
TX_DATA	D1	In	Transmit the differential data on DP and DM
TX_SE0	D2	In	Transmit single-ended zero (SE0) on DP and DM
INT	D3	Out	Active-HIGH interrupt signal; asserted and latched whenever any unmasked interrupt occurs
RX_DP	D4	Out	Single-ended receive data from DP
RX_DM	D5	Out	Single-ended receive data from DM
RX_RCV	D6	Out	Differential receive data from DP and DM
RESERVED	D7	Out	Reserved; the FUSB2805 drives this pin LOW

### 3-Pin FS/LS Serial Mode

This mode is provided for links that contain legacy FS/LS functionality and enables a cost-effective upgrade path to HS functionality.

To enter 3-pin serial mode, the link controller sets the 3PIN\_FSL\_SERIAL bit in the interface control register to logic 1. To exit this mode, the link controller asserts STP.

An INT signal is also provided to inform the link of USB events. If the link requires CLOCK to be running during 3-pin serial mode, the CLK\_SUSPENDM register bit must be set to logic 1b before entering 3-pin serial mode.

The FUSB2805 requires CLKIN to be kept running when in 3-pin mode. In 3-pin serial mode, the data bus assignments are changed to those described in Table 3. Examples of the signaling of data packets are shown in Figure 21.

**Table 3. Signal Mapping on ULPI Bus During 3-Pin Serial Mode**

Signal	Maps To	Direction	Description
TX_ENABLE	D0	In	Active-HIGH transmit enable
DAT	D1	I/O	Transmit differential data on DP and DM when TX_ENABLE is HIGH Receive differential data from DP and DM when TX_ENABLE is LOW
SE0	D2	I/O	Transmit single-ended zero on DP and DM when TX_ENABLE is HIGH Receive single-ended zero on DP and DM when TX_ENABLE is LOW
INT	D3	Out	Active-HIGH interrupt signal; asserted and latched whenever any unmasked interrupt occurs
RESERVED	D[7:4]	Out	Reserved; the FUSB2805 drives this pin LOW

### Power Supply Modes

The FUSB2805 supports two basic modes of supply operation and include the following:

- Normal Mode
- Power-Down Mode

#### Normal Mode

This mode is entered when V<sub>CC</sub> and V<sub>IO</sub> are powered and Chip\_Select\_N is asserted.

#### Power-Down Mode

When chip select is inactive, FUSB2805 enters power-down mode, during which the following apply:

- Chip\_Select\_N is HIGH or V<sub>IO</sub> is not present.
- All internal circuits are powered down; total V<sub>CC</sub> current <36 μA.
- D[0-7], CLOCK, NXT, and DIR are three-stated and ignored; STP is ignored.
- Voltage regulators powering the OTG PHY are turned off.
- Pull-down resistors on the ULPI interface are enabled to prevent a floating bus (V<sub>IO</sub> present).
- The FUSB2805 is forced into a low-power state and ignores any ULPI commands, including wake-up events.
- If V<sub>IO</sub> is not present, those signals referenced to V<sub>IO</sub> are also not powered.

## USB State Transitions

A high-speed USB host or On-The-Go (OTG) device handles more than one electrical state, as defined in the USB and OTG specifications. The FUSB2805 accommodates the various states through the register

bit settings of XcvrSelect, TermSelect, OpMode[1:0], DpPulldown, and DmPulldown. Table 4 summarizes the operating states.

**Table 4. Operating States and Corresponding Resistor Settings**

Signaling Mode	Register Settings					Internal Resistor Settings				
	XcvrSelect[1:0]	TermSelect	OpMode[1:0]	DpPulldown	DmPulldown	rpu_dp_en	rpu_dm_en	rpd_dp_en	rpd_dm_en	hsterm_en
<b>General Settings</b>										
Three-State Drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or $V_{BUS} < V_{th}$ (SESS_END)	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
<b>Host Settings</b>										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host High Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test_J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
<b>Peripheral Settings</b>										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral High Speed	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral Full Speed	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral Test_J/Test_K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG Device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG Device, Peripheral High Speed	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG Device, Peripheral Full Speed	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG Device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG Device Peripheral, HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG Device Peripheral, Test_J/Test_K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b

## Protocol Description

### ULPI References

The FUSB2805 provides a 12-pin (SDR) ULPI interface for communication with the link controller. It is strongly recommended that users of the FUSB2805 read the ULPI and UTMI+ specifications as listed below:

*UTMI+ Low Pin Interface Specification (ULPI), Revision 1.1, October 20, 2004.* <http://www.ulpi.org>

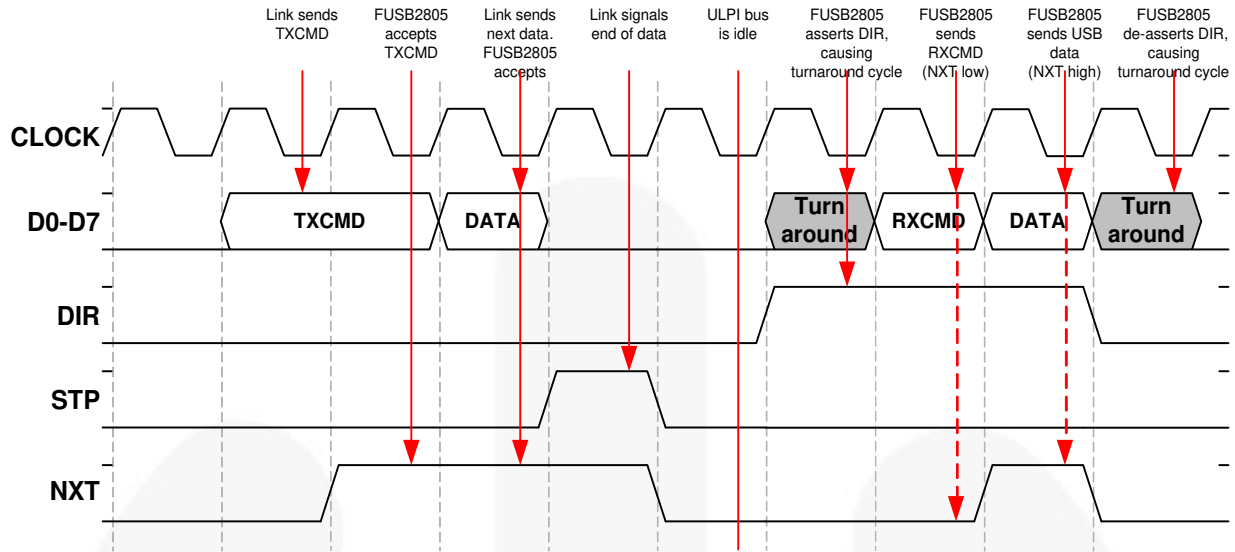
*UTMI+ Specification, Revision 1.0, February 22, 2004.* <http://www.ulpi.org>

### ULPI Bus

A description of the ULPI pin signals are given in Table 5. During synchronous mode, all signals are synchronous to CLOCK. Using the ULPI bus, the link controller can perform register reads and writes and transmit data on the USB bus. The FUSB2805 uses the ULPI bus to send status information, decoded USB data, and register contents to the link controller. During low-power and serial modes, all signals are asynchronous to CLOCK, even if the clock is running. An example of ULPI bus usage is shown in Figure 8.

**Table 5. ULPI Signal Description**

Signal Name	Direction on FUSB2805	Signal Description
CLOCK	OUT	60 MHz interface clock. If a clock is attached on CLKIN, the FUSB2805 drives a 60 MHz output clock. During low-power and serial modes, the clock can be turned off to save power.
D0-D7	I/O	8-bit data bus. In synchronous (SDR) mode, the link drives D0-D7 LOW by default. The link initiates transfers by sending a non-zero data pattern called a TXCMD (transmit command). In synchronous mode, the direction of D0-D7 is controlled by DIR. Contents of the D0-D7 lines must be ignored for exactly one clock cycle whenever DIR changes value; called a "turnaround" cycle. The data lines have fixed directions and different meanings in low-power, 6-pin, and 3-pin serial modes.
DIR	OUT	Controls the direction of the D0-D7 data bus. In synchronous (SDR) mode, the FUSB2805 drives DIR LOW by default, making the data bus an input so the FUSB2805 can listen for TXCMDs from the link controller. The FUSB2805 drives DIR HIGH only when it has data for the link. When DIR and NXT are both HIGH, the byte on the data bus contains decoded USB data. When DIR is HIGH and NXT is LOW, the byte contains status information called an RXCMD (receive command). The only exception is when the FUSB2805 returns register-read data, where NXT is also LOW, replacing the usual RXCMD byte. Every change in DIR causes a turnaround cycle on the data bus, during which D0-D7 are not valid and must be ignored by the link. DIR is always asserted during low-power, 6-pin, 3-pin, and serial modes.
STP	IN	Stop. In synchronous (SDR) mode, the link drives STP HIGH for one cycle after the last byte of data sent to the FUSB2805. The link can optionally assert STP to force DIR to be de-asserted. In low-power and serial modes, the link holds STP HIGH to wake up the FUSB2805, causing the ULPI bus to return to synchronous mode.
NXT	OUT	Next. In synchronous (SDR) mode, the FUSB2805 drives NXT HIGH to throttle data. If DIR is LOW, the FUSB2805 asserts NXT to tell the link controller to place the next data byte on D0-D7 in the following clock cycle. If DIR is HIGH, the FUSB2805 asserts NXT to tell the link controller a valid USB data byte is on D0-D7 in the current cycle. The FUSB2805 always drives an RXCMD when DIR is HIGH and NXT is LOW, unless register-read data is to be returned to the link controller in the current cycle. NXT is not used in low-power or serial modes.



**Figure 8. ULPI Generic Data Transmit Followed by Data Receive**

On power-up, the FUSB2805 performs an internal power-on reset and asserts DIR to indicate to the link that the ULPI bus cannot be used. When the internal PLL is stable, the FUSB2805 de-asserts DIR. The power-up time depends on the  $V_{CC}$  supply rise time and the PLL startup time ( $t_{startPLL}$ ).

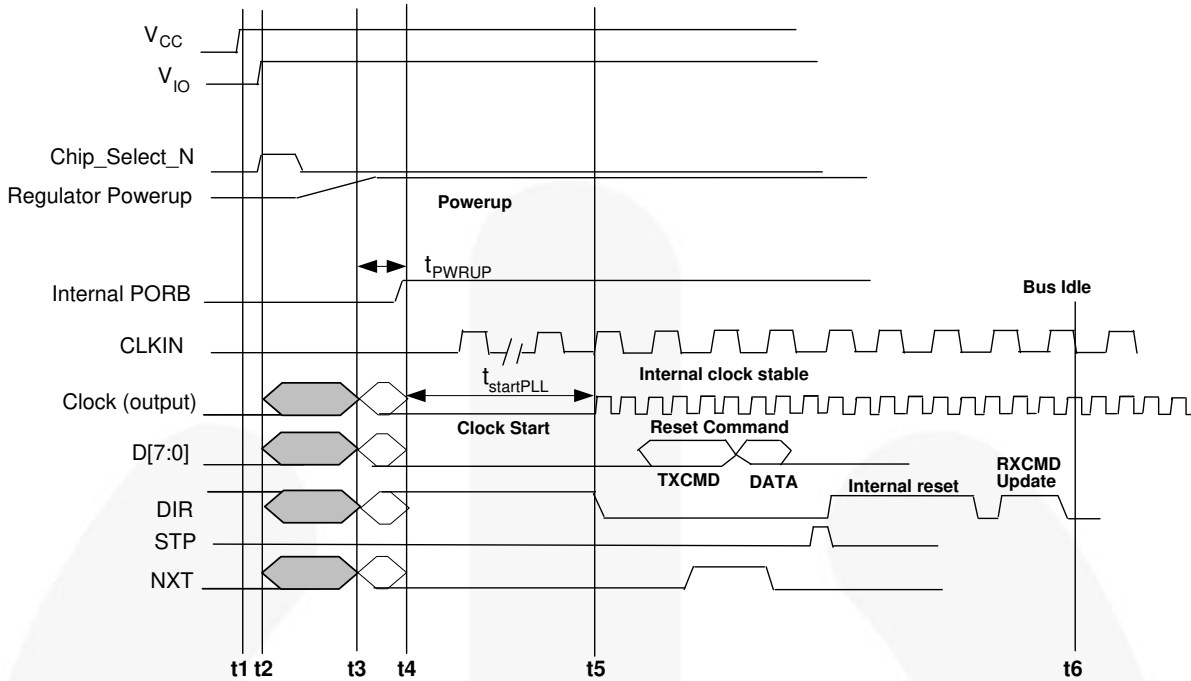
Whenever DIR is asserted, the FUSB2805 drives the NXT pin LOW and must drive the data bus (D0-D7) with RXCMD values. When DIR is de-asserted, the link must drive the data bus (D0-D7) to the default LOW. Before beginning USB packets, the FUSB2805 is reset by the link setting the RESET bit in the function control register. After the RESET bit is set, the FUSB2805 asserts DIR until the internal reset completes. The FUSB2805 automatically de-asserts DIR and clears the RESET bit when the reset has completed. After every reset, an RX CMD is sent to the link to update USB status information. After this sequence, the ULPI bus is ready for use and the link can start USB operations.

If Chip\_Select\_N is de-asserted, the FUSB2805 is retained in power-down mode, where all ULPI interface pins are three-state, internal regulators are shut down, and power consumption is reduced even further than in low-power mode.

If low-power mode is entered due to no  $V_{IO}$ , the recommended power-up sequence for the link is:

1. Connect  $V_{CC}$  and  $V_{IO}$  supplies.
2. Chip\_Select\_N goes HIGH to LOW to enable the FUSB2805.
3. Link waits for at least  $t_{PWRUP}$ , ignoring all ULPI pins' status.
4. The link may start to detect DIR status level; if the DIR is detected LOW, the link may send a reset command.
5. The ULPI interface is ready for use.





**Figure 9. Power-up, Reset, and Bus Idle Sequence for ULPI Ready**

**Notes:**

4. With the CLKIN stable, the FUSB2805 drives a 60 MHz clock out from the CLOCK pin when DIR de-asserts. This is shown as “CLOCK (output)” above.
5. t1: V<sub>CC</sub> is applied to the FUSB2805.
6. t3: Chip\_Select\_N transitions to active state (LOW). FUSB2805 internal regulator turns on and the ULPI pins become active (may be driven HIGH or LOW), but should be ignored during the power-up time t<sub>PWRUP</sub>.
7. t4: After the POR pulse (Power-On Reset), the ULPI pins are driven to a defined level. DIR is driven HIGH, then the other ULPI pins are driven LOW.
8. t5: The PLL stabilizes after the PLL startup time, t<sub>startPLL</sub>. The CLOCK pin begins to output 60 MHz, the DIR pin transitions LOW, and the link must drive STP and D[7:0] to LOW (idle). The link then initiates a reset command to initialize the FUSB2805.
9. t6: The power-up sequence is completed and the ULPI bus interface is ready for use.

**V<sub>BUS</sub> Power and Over-Current Detection**

**Driving 5 V on V<sub>BUS</sub> – External Only**

No internal charge pump is supported by the FUSB2805. The PSW pin supports an external V<sub>BUS</sub> supply and is an active HIGH (open source) signal used to control external power management integrated circuits, such as OTG support SMPS devices.

**Over-Current Detection**

Only external over-current detection is supported by the FUSB2805. An over-current detection circuit is required for host applications that supply more than 100 mA on V<sub>BUS</sub> between voltages of 4.75 V to 5.25 V.

A digital signal from this external circuit must be connected to the FAULT pin, which directly controls the PSW pin (as shown in Figure 5). The polarity of the signal input to this pin, which controls PSW, is selectable.

## USB Packet Transmit and Receive

When transmitting and receiving USB packets, there are limits set on the link and PHY processing time to ensure that USB inter-packet delays are also met.

These times are determined by the USB event and the packet format (i.e. transmit with PID or NOPID, transmit error, receive error, etc.).

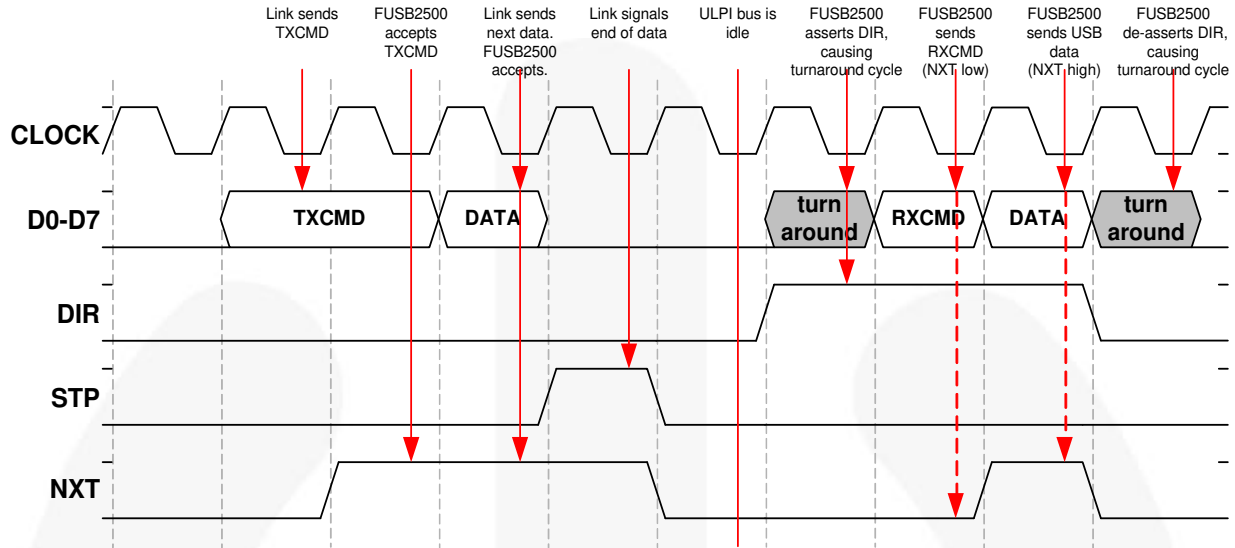


Figure 10. Example ULPI Packet Transmit and Receive

**Note:**

10. Please refer to ULPI specifications section 3.8.2 for further detail on USB packet operations and functionality.

### USB Packet Timing

The USB2.0 specification defines the inter-packet timing and the UTMI/UTMI+ specifications define synchronization and processing delays. The ULPI Rev. 1.1 specification defines the inter-packet delays to ensure compatibility with USB2.0 and supplemental specifications.

### Pipeline Delays

Table 6 describes the delays (in clock cycles) with which to comply using ULPI. The USB bus events are measured relative to D+ and D-. The ULPI timings are relative to the clock edge on which the transition is detected (i.e. the clock edge on which STP is detected).

**Table 6. Pipeline Delays**

Parameter Name	HS PHY Delay	FS PHY Delay	LS PHY Delay	Definition
RXCMD Delay(J/K)	4	4	4	Number of clocks after a change in the internal USB bus state is detected to an RXCMD byte being sent over the ULPI bus. Applies to all changes except SE0.
RXCMD Delay(SE0)	4	4 to 6	16 to 18	Number of clocks between the USB bus state indicating SE0 to an RXCMD byte being sent over the ULPI bus. Delay is increased due to filtering.
TX Start Delay	1 to 2	6 to 10	74 to 75	Number of clocks between the FUSB2805 detecting a TXCMD on the ULPI bus to transmitting the first K of the SYNC pattern on the USB bus.
TX End Delay (packets)	2 to 5	NA	NA	Number of clocks between the FUSB2805 detecting STP on the ULPI bus to completing EOP transmission on the USB bus. HS EOP is completed when all eight consecutive ones have finished transmitting on the USB bus. FS/LS packets finish many clock cycles after STP is asserted. The link must look for RXCMD bytes indicating SE0-to-J transition to determine when the transmission is completed on the USB bus.
TX End Delay (SOF)	6 to 9	NA	NA	HS SOF packets have a long EOP. The link must wait at least nine clocks or for an RXCMD, indicating squelch (LINESTATE=00b), before transmitting the next packet.
RX Start Delay	3 to 8	NA	NA	Number of clocks after first K of SYNC pattern is seen on the USB bus to the simultaneous assertion of DIR and NXT or an RXCMD indicating RxActive. Used for HS packets only. For FS/LS packets, the link must look for RXCMD bytes indicating J-to-K transition.
RX End Delay	3 to 8	17 to 18	122 to 123	Number of clocks after EOP occurs on the USB bus to the FUSB2805 de-asserting DIR or indicating RxActive LOW in an RXCMD byte. HS EOP is completed when all eight consecutive ones have finished transmitting on the USB bus. FS/LS EOP occurs when SE0 starts on the USB bus. For FS/LS, the link uses LINESTATE and not RxEnd delay to time USB packets.

**Note:**

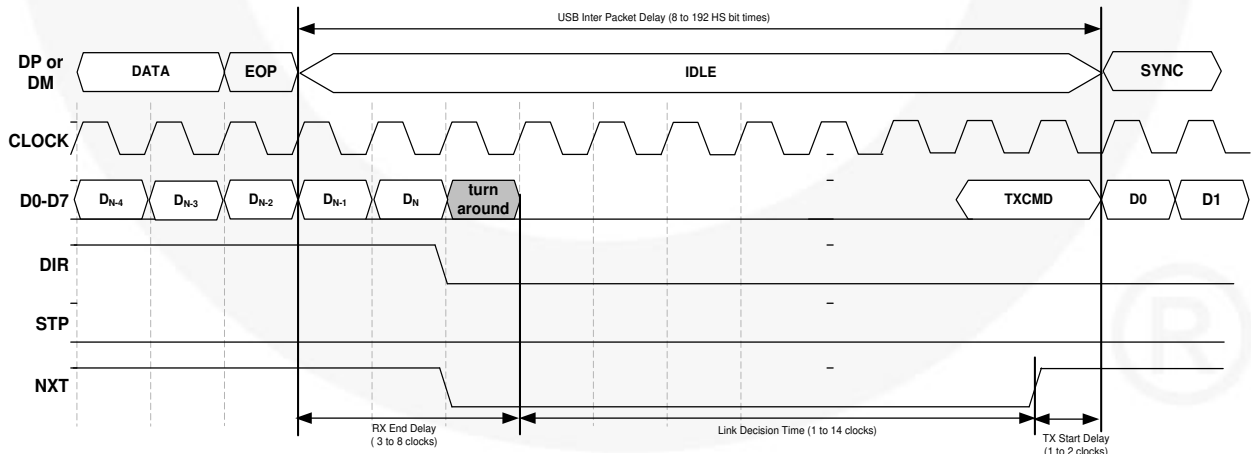
11. Please refer to ULPI Rev 1.1 specifications, section 3.8.2.6.2 for details on PHY pipeline delays.

**Link Decision Times**

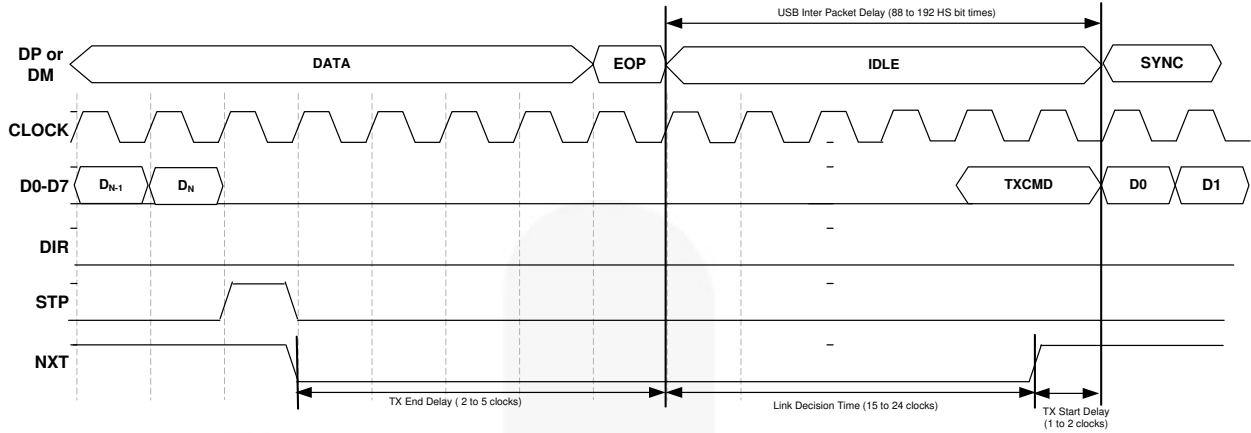
The amount of clock cycles allocated to the link to respond to a received packet and correctly receive back-to-back packets is given in Table 7.

**Table 7. Link Decision Times**

Parameter Name	HS PHY Delay	FS PHY Delay	LS PHY Delay	Definition
Transmit-Transmit (Host Only)	15 to 24	7 to 18	77 to 247	Number of clocks a host link must wait before driving the TXCMD for the second packet. In HS, the link starts counting from the assertion of STP for the first packet. In FS, the link starts counting from the RXCMD indicating LINESTATE has transitioned from SE0-to-J for the first packet. The timings given ensure inter-packet delays of 2.0 to 6.5 bit times.
Receive-Transmit (Host or Peripheral)	1 to 14	7 to 18	16 to 18	Number of clocks the link must wait before driving the TXCMD for the transmit packet. In HS, the link starts counting from the end of the receive packet (de-assertion of DIR or an RXCMD indicating RxActive is LOW). In FS/LS, the link starts counting from the RXCMD indicating LINESTATE has transitioned from SE0-to-J for the receive packet. The timings given ensure inter-packet delays of 2.0 to 6.5 bit times.
Receive-Receive (Peripheral Only)	1	1	1	Minimum number of clocks between consecutive receive packets. The link must be capable of receiving both packets.
Transmit-Receive (Host or Peripheral)	92	80	718	Host or peripheral transmits a packet, then times out after this number of clock cycles if a response is not received. Any subsequent transmission can occur after this time.



**Figure 11. HS Receive to Transmit Packet Timing, Example 1**

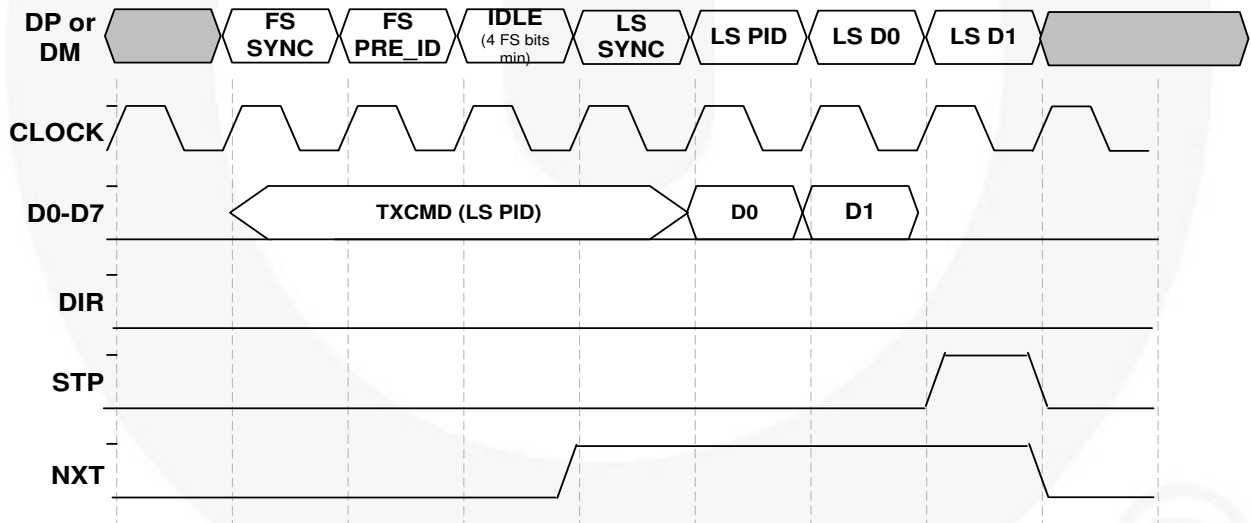


**Figure 12. HS Transmit to Transmit Packet Timing, Example 2**

**Preamble**

Preamble packets are headers to low-speed packets that must travel over a FS bus between a host and a hub. To enter preamble mode, the link sets XCVRSELECT[1:0]=11b in the FUNC\_CTRL register and, when in this mode (Preamble), the FUSB2805 operates just as in FS mode and sends all the data with the FS rise and fall time characteristics. Whenever the link transmits a USB packet in preamble mode, the FUSB2805 automatically sends a preamble header at

the FS bit rate before sending the packet at low-speed bit rate. The FUSB2805 ensures a minimum gap of four FS bit times between the last bit of the FS PRE\_PID and the first bit of the LS SYNC. The FUSB2805 drives a J-state for at least one FS bit time after sending the PRE-PID, after which the resistor can hold the J-state on the bus. In preamble mode, the FUSB2805 can also receive LS packets from the FS bus. Figure 13 shows an example preamble packet.



**Figure 13. Preamble Sequence**

## RXCMD and TXCMD

ULPI modifies the original UTMI data stream such that it can fit more data types. Redundancy in the PID byte during transmit is overloaded with ULPI transmit commands (TXCMD). Unused data bytes in the receive stream are overloaded with receive commands (RXCMD). ULPI defines a transmit command byte that is sent by the link and a receive command byte that is sent by the FUSB2805.

## Transmit Command (TXCMD)

The link initiates transfers to the FUSB2805 by sending the transmit command (TXCMD) byte, as described in Table 8. TXCMD is comprised of a 2-bit command code and a 6-bit payload.

**Table 8. Transmit Commands (TXCMD) from Link to FUSB2805**

Command Type Descriptor	Command Code [7:6]	Command Payload [5:0]	Description
IDLE	00b	00 0000b (NOOP)	No operation. 00h is the idle state of the ULPI bus. The link drives NOOP by default.
		XX XXXXb	Reserved command space. Values other than those above create undefined behavior.
TRANSMIT	01b	00 0000b (NOPID)	Transmit USB data that does not have a PID (packet ID), such as chirp, and resume signaling. The FUSB2805 starts transmitting on the USB beginning with the next data byte.
		00 XXXXb (PID)	Transmit USB packet. D[3:0] indicates USB packet identifier PID[3:0].
		XX XXXXb (RSVD)	Reserved command space. Values other than those above create undefined behavior.
REGISTER WRITE	10b	10 1111b (EXTW)	Extended register write command (optional). The 8-bit address must be in the next clock cycle after the command is accepted.
		XX XXXXb (REGW)	Register write command with 6-bit immediate address.
REGISTER READ	11b	10 1111b (EXTR)	Extended register read command (optional). The 8-bit address must be provided in the next clock cycle after the command is accepted.
		XX XXXXb (REGR)	Register read command with 6-bit immediate address.

### Receive Command (RXCMD)

The FUSB2805, after asserting DIR, uses the receive command (RXCMD) byte to update the link on line state, USB receive, disconnect, and OTG information via the ULPI data bus.

The FUSB2805 automatically sends an RXCMD whenever there is a change in any of the RXCMD data fields. The link must be able to accept an RXCMD at any time; including single or multiple (back-to-back) RXCMDs and, at any time during USB receive packets, when NXT is LOW.

**Table 9. RXCMD Data Byte Format**

DATA[7:0]	Status Name	Description																									
[1:0]	LINESTATE	<p><b>Line State Signals:</b>  D[0]: LINESTATE0  D[1]: LINESTATE1  LINESTATE[1:0] reflects the current status of DP and DM and is a function of various register settings and whether the device is a host or peripheral. The detailed encoding, and descriptions thereof, is shown in Table 10 and Table 11.</p>																									
[3:2]	V <sub>BUS</sub> State	<p><b>Encoded V<sub>BUS</sub> Voltage State:</b> This encoding is used for over-current detection, session start, and session request (SRP). The Sess_End and Sess_VLD indicators are signals from the internal FUSB2805 V<sub>BUS</sub> comparators. These encoded V<sub>BUS</sub> states are:</p>																									
		<table border="1"> <thead> <tr> <th>Value</th> <th>V<sub>BUS</sub> Voltage</th> <th>Sess_End</th> <th>Sess_VLD</th> <th>A_V<sub>BUS</sub>_VLD</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td><math>V_{BUS} &lt; V_{B\_Sess\_End}</math></td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>01b</td> <td><math>V_{B\_Sess\_End} \leq V_{BUS} &lt; V_{A\_Sess\_Vld}</math></td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>10b</td> <td><math>V_{A\_Sess\_Vld} \leq V_{BUS} &lt; V_{A\_VBUS\_Vld}</math></td> <td>X</td> <td>1</td> <td>0</td> </tr> <tr> <td>11b</td> <td><math>V_{BUS} \geq V_{A\_VBUS\_Vld}</math></td> <td>X</td> <td>X</td> <td>1</td> </tr> </tbody> </table>	Value	V <sub>BUS</sub> Voltage	Sess_End	Sess_VLD	A_V <sub>BUS</sub> _VLD	00b	$V_{BUS} < V_{B\_Sess\_End}$	1	0	0	01b	$V_{B\_Sess\_End} \leq V_{BUS} < V_{A\_Sess\_Vld}$	0	0	0	10b	$V_{A\_Sess\_Vld} \leq V_{BUS} < V_{A\_VBUS\_Vld}$	X	1	0	11b	$V_{BUS} \geq V_{A\_VBUS\_Vld}$	X	X	1
		Value	V <sub>BUS</sub> Voltage	Sess_End	Sess_VLD	A_V <sub>BUS</sub> _VLD																					
		00b	$V_{BUS} < V_{B\_Sess\_End}$	1	0	0																					
		01b	$V_{B\_Sess\_End} \leq V_{BUS} < V_{A\_Sess\_Vld}$	0	0	0																					
10b	$V_{A\_Sess\_Vld} \leq V_{BUS} < V_{A\_VBUS\_Vld}$	X	1	0																							
11b	$V_{BUS} \geq V_{A\_VBUS\_Vld}$	X	X	1																							
[5:4]	RxEvent	<p><b>RxEvt Encoding:</b> This encoding field of RXCMD is used to inform the link of information packets received on the USB bus. These events are:</p>																									
		<table border="1"> <thead> <tr> <th>Value</th> <th>RxError</th> <th>RxActive</th> <th>HostDisconnect</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>01b</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>10b</td> <td>X</td> <td>X</td> <td>1</td> </tr> <tr> <td>11b</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Value	RxError	RxActive	HostDisconnect	00b	0	0	0	01b	0	1	0	10b	X	X	1	11b	1	1	0					
		Value	RxError	RxActive	HostDisconnect																						
		00b	0	0	0																						
		01b	0	1	0																						
10b	X	X	1																								
11b	1	1	0																								
[6]	ID	This bit reflects the state of the ID pin. It is valid 50ms after ID_PULLUP is set to 1b.																									
[7]	ALT_INT	Default is not to use this alternate interrupt bit. The link, optionally, can enable the BVALID_RISE and/or BVALID_FALL bits in the PWR_CNTRL register. Corresponding changes in BVALID cause an RXCMD to be sent to the link with this ALT_INT bit asserted.																									

## Line State Encoding

As mentioned in Table 9, the LINESTATE[1:0] sent to the link is a function of whether the port is upstream (peripheral) or downstream (host) facing. Dual-role OTG devices must select the correct LINESTATE encoding,

depending upon its mode. Note that the configuration as a LS peripheral (upstream facing port), with DM pull-up, is not supported by the FUSB2805.

**Table 10. LINESTATE[1:0] Encoding for Upstream (Peripheral) Facing Ports; DP\_PULLDOWN=0b**

Mode	Value	Full Speed	High Speed	Chirp
XCVRSELECT[0:1]		01, 11	00	00
TERMSELECT		1	0	1
LINESTATE[1:0]	00b	SE0	Squelch	Squelch
	01b	FS-J	! Squelch	(! Squelch) AND (HS_Differential_Receiver_Output)
	10b	FS-K	Invalid	(! Squelch) AND (! HS_Differential_Receiver_Output)
	11	SE1	Invalid	Invalid

**Notes:**

- 12. (! Squelch) indicates inactive squelch.
- 13. (! HS\_Differential\_Receiver\_Output) indicates inactive HS\_Differential\_Receiver\_Output.

**Table 11. LINESTATE[1:0] Encoding for Downstream (Host) Facing Ports; DP\_PULLDOWN and DM\_PULLDOWN=1b**

Mode	Value	Low Speed	Full Speed	High Speed	Chirp
XCVRSELECT[0:1]		10	01, 11	00	00
TERMSELECT		1	1	0	0
OPMODE[1:0]		X	X	00, 01 or 11	10
LINESTATE[1:0]	00b	SE0	SE0	Squelch	Squelch
	01b	LS-K	FS-J	! Squelch	(! Squelch) AND (HS_Differential_Receiver_Output)
	10b	LS-J	FS-K	Invalid	(! Squelch) AND (! HS_Differential_Receiver_Output)
	11	SE1	SE1	Invalid	invalid

**Notes:**

- 14. (! Squelch) indicates inactive squelch.
- 15. (! HS\_Differential\_Receiver\_Output) indicates inactive HS\_Differential\_Receiver\_Output.



## V<sub>BUS</sub> Voltage State Encoding

As mentioned in Table 9, changes in the V<sub>BUS</sub> state encoding initiate an RXCMD to the link. For the link to receive V<sub>BUS</sub> state updates, the link must first enable the corresponding interrupts in the USB\_INTR\_EN\_R and USB\_INTR\_EN\_F registers. Link uses the indicator signals to take action based on typical configurations (host, peripheral, OTG device). Table 12 shows the V<sub>BUS</sub> indicators in RXCMD based on the configuration.

**Table 12. V<sub>BUS</sub> Indicator Signals in RXCMD**

Configuration	A_VBUS_VLD	SESS_VLD	SESS_END
Standard Host	Yes	No	No
Standard Peripheral	No	Yes	No
OTG A-Device	Yes	Yes	No
OTG B-Device	No	Yes	Yes

For the standard USB host controller application, the following applies:

- The system must be able to provide 500 mA for  $4.75\text{ V} \leq V_{BUS} \leq 5.25\text{ V}$ .
- An external circuit is to be used to detect over-current conditions. If the external over-current detector provides a digital fault signal, the signal must be connected to the FAULT input pin and the link must do the following:
  1. Set the IND\_COMPL bit in the INTF\_CTRL register to 0b or 1b, depending on the polarity of the external fault signal.
  2. Set the USE\_EXT\_VBUS\_IND bit in the OTG\_CTRL register to 1b.
  3. If it is not necessary to qualify the fault indicator with the internal A\_VBUS\_VLD comparator, set the IND\_PASSTHRU bit in the INTF\_CTRL register to 1b.

For the standard USB peripheral controller applications, the standard peripherals detect when V<sub>BUS</sub> is at a sufficient level for operation. SESS\_VLD must be enabled to detect the start and end of a USB peripheral operation. Detection of the A\_VBUS\_VLD and SESS\_END thresholds is not needed for standard peripherals.

For a device configured as an OTG B-device, SESS\_VLD must be used to detect when V<sub>BUS</sub> is at a sufficient level for operation. SESS\_END must be used to detect when V<sub>BUS</sub> has dropped to a LOW level, allowing the B-device to safely initiate V<sub>BUS</sub> pulsing SRP.

A device configured as an OTG A-device must provide a minimum of 8 mA onto V<sub>BUS</sub>. This 8 mA (minimum) is

provided external to the FUSB2805. If the external charge pump source provides more than 100 mA, the over-current circuit must be used and the host controller application criteria apply. The OTG A-device also uses SESS\_VLD to detect when an OTG B-device is initiating V<sub>BUS</sub> pulsing SRP. The control of this external charge pump is accomplished via the PSW pin.

## RxEvent Encoding

As mentioned in Table 9, this encoding provides information to the link related to the packets received on the USB bus. The primary encodings are RxActive, RxError, and HostDisconnect.

### RxActive

When the FUSB2805 detects a SYNC pattern on the USB bus, it signals an RxActive event to the link. This RxActive event can be communicated in two methods:

- FUSB2805 simultaneously asserts DIR and NXT; or
- FUSB2805 sends an RXCMD to the link with the RxActive field in the RxEvent bits set to 1b.

The link must be capable of detecting both methods and the RxActive frames the receive packet from the first byte to the last byte. It also must assume that RxActive is set to 0b when indicated in an RXCMD or when DIR is de-asserted, whichever occurs first.

The RxActive is also used by the link to time the high-speed packets and ensure that the bus turn-around times are met.

### RxError

When the FUSB2805 detects an error while receiving a USB packet, it de-asserts NXT and sends an RXCMD with the RxError field set to 1b. The received packet is no longer valid and must be dropped by the link.

### HostDisconnect

This encoding is only valid when the FUSB2805 is configured as a host (DP\_PULLDOWN=DM\_PULLDOWN=1b) and indicates to the host controller when a peripheral is connected (0b) or disconnected (1b). The host controller must enable HostDisconnect by setting the HOST\_DISCON\_R and HOST\_DISC\_F bits in the USB\_INTR\_EN\_R and USB\_INTR\_EN\_F registers, respectively. Changes in HostDisconnect cause the FUSB2805 to send an RXCMD to the link with the updated value.

In peripheral mode, HostDisconnect must be ignored and must not mask events on RxActive or RxError.

*Refer to ULPI specifications, section 3.8.1 for details on RXCMD and TXCMD operations and functionality.*

## Register Read and Write Operations

The link can read or write register bytes, and set or clear register bits as needed, using the TXCMD byte. The FUSB2805 supports immediate and extended addressing register operations, with the extended register addressing being optional for the link. If the FUSB2805 asserts DIR during an operation, the register operation is aborted. When a register operation is aborted, the link must retry until successful.

### Immediate Register Read and Write

Immediate address registers are accessed by first sending the TXCMD byte as either a RegRead or RegWrite command with the required register address.

For RegRead, the link sends its read command request and waits for NXT to assert. In the cycle after NXT asserts, the FUSB2805 asserts DIR to gain control of the bus. In the cycle after DIR asserts, the FUSB2805 must return the register read data. The FUSB2805 does not assert NXT when DIR is asserted during the register read operation, including during the period that the register read data is being returned, to ensure that a USB receive event always overrides the register read during any cycle (*see section 3.8.3.2 of ULPI Rev. 1.1 specification*). If the FUSB2805 aborts the RegRead by asserting DIR early, the link must retry the RegRead when the bus is idle.

For RegWrite, the link sends its write command request and waits for NXT to assert. In the cycle after NXT asserts, the link sends the register write data and waits for NXT to assert again. When NXT asserts the second time, the link asserts STP in the following cycle to complete the operation. The FUSB2805 must detect STP assertion before it accepts another transmit command. If the FUSB2805 aborts the RegWrite by asserting DIR the link must retry the RegWrite when the link is idle.

*For back-to-back read/write and USB receive signaling, refer to ULPI specifications, section 3.8.3.3 for details and timing waveforms.*

### Extended Register Read and Write

Extended addressing read (EXTR) and write (EXTW) means that the address is available in the next clock cycle. Accessing immediate address 2Fh indicates an access to the extended register set.

For an EXTR (extended register read), the link sends a register-read command with the address set to 2Fh and waits for NXT to assert. In the cycle after NXT asserts, the link sends the extended register address and waits for NXT to assert again. When NXT asserts the second time, the FUSB2805 asserts DIR to gain control of the bus. In the cycle after DIR asserts, the FUSB2805 must return the register read data. The FUSB2805 does not

assert NXT when DIR is asserted during the register read operation, including during the period that the register read data is being returned, to ensure that a USB receive event always overrides the register read during any cycle (*see section 3.8.3.5 of ULPI Rev. 1.1 specification*). If the FUSB2805 aborts the RegRead by asserting DIR early, the link must retry the RegRead when the bus is idle.

For an EXTW (extended register write), the link sends a register write command with the address set to 2Fh and waits for NXT to assert. In the cycle after NXT asserts, the link sends the extended register address and waits for NXT to assert again. When NXT asserts the second time, the link sends the register write data and waits for NXT to assert again. When NXT asserts the third time, the link asserts STP in the following cycle to complete the operation. If the FUSB2805 aborts the RegWrite by asserting DIR, the link must retry the RegWrite when the bus is idle.

*For back-to-back extended read and USB receive signaling, refer to ULPI specifications section 3.8.3.5 for details and timing waveforms.*

*Please refer to ULPI specification, section 3.8.3 for details on register read and write operations and functionality.*

## Aborting ULPI Transfers

There are two ways to abort ULPI transfers:

- Link aborted by the FUSB2805
- FUSB2805 aborted by the link.

### Link Aborted by the FUSB2805

When the link is transferring data, the FUSB2805 can abort the link by asserting DIR.

### FUSB2805 Aborted by the Link

When FUSB2805 has DIR asserted (in synchronous mode), the link can abort by asserting STP. There are very specific criteria to meet in the timing diagram to guarantee the link transaction, which is related to the cycle in which STP is asserted by the link to request aborting the FUSB2805 (*see section 3.3.4.2 of the ULPI Rev. 1.1 specification for timing details*). While this feature can be used at any time, it is provided to terminate a “babbling” port by disabling the FUSB2805. The FUSB2805 cannot guarantee the validity of USB data during the current packet and the next packet if the link asserts STP during a USB receive packet.

*Please refer to ULPI specification, section 3.8.4 for details on aborting ULPI transfers.*