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# FUSB301A

## Autonomous USB Type-C Controller with Configurable I<sup>2</sup>C Address

### Features

- Fully Autonomous Type-C Controller Supports Type-C Versions 1.1 and 1.0
- V<sub>DD</sub> Operating Range, 3.0 V- 5.5 V
- Low Disable Power: I<sub>CC</sub> = 2.0  $\mu$ A (Max.)
- Low Standby Power: I<sub>CC</sub> = 7.0  $\mu$ A (Max.)
- DRP Mode with Optional Accessory Support
- Configurable I<sup>2</sup>C Address
- Capable of Supporting Try.SNK and Try.SRC
- Dead Battery Support (SINK Support when No Power Applied)
- 2 kV HBM ESD Protection
- Small Packaging, 12 Lead TMLP (1.6 mm x 1.6 mm x 0.375 mm)

### Description

The FUSB301A is a fully autonomous Type-C controller optimized for <15 W applications. The FUSB301A offers CC logic detection for Source Mode, Sink Mode, DRP, accessory detection support, and dead battery support. The FUSB301A features configurable I<sup>2</sup>C address to support multiple ports per system. The FUSB301A features an extremely low power disable mode as well as low power during normal operation. It is available in an ultra thin, 12-Lead TMLP package.

### Applications

- Smartphones
- Tablets
- Notebooks
- Ultra Portable Applications

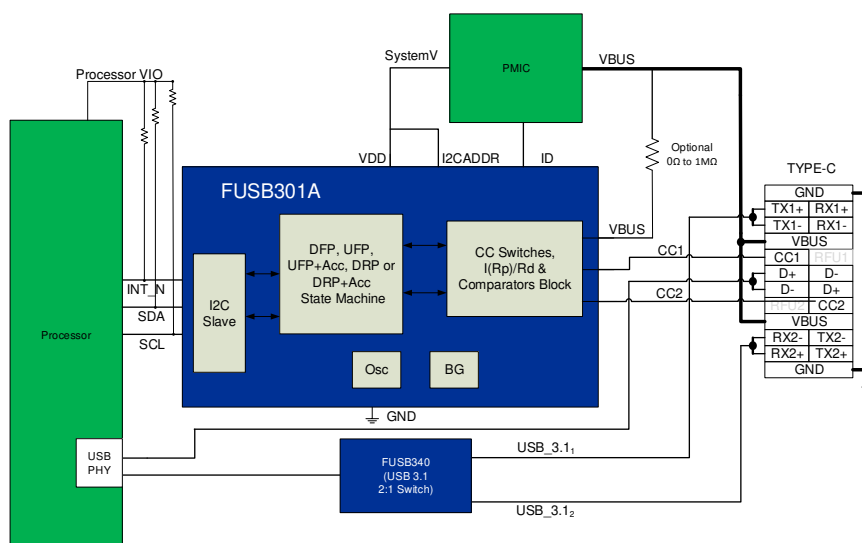


Figure 1. Typical Application

### Ordering Information

| Part Number | Top Mark | Operating Temperature Range | Package  | Packing Method |
|-------------|----------|-----------------------------|--|----------------|
| FUSB301A    | NX       | -40 to 85°C                 | 12-Lead Ultra-thin Molded Leadless Package (TMLP) 1.6 mm x 1.6 mm x 0.375 mm | Tape and Reel  |

## Block Diagram

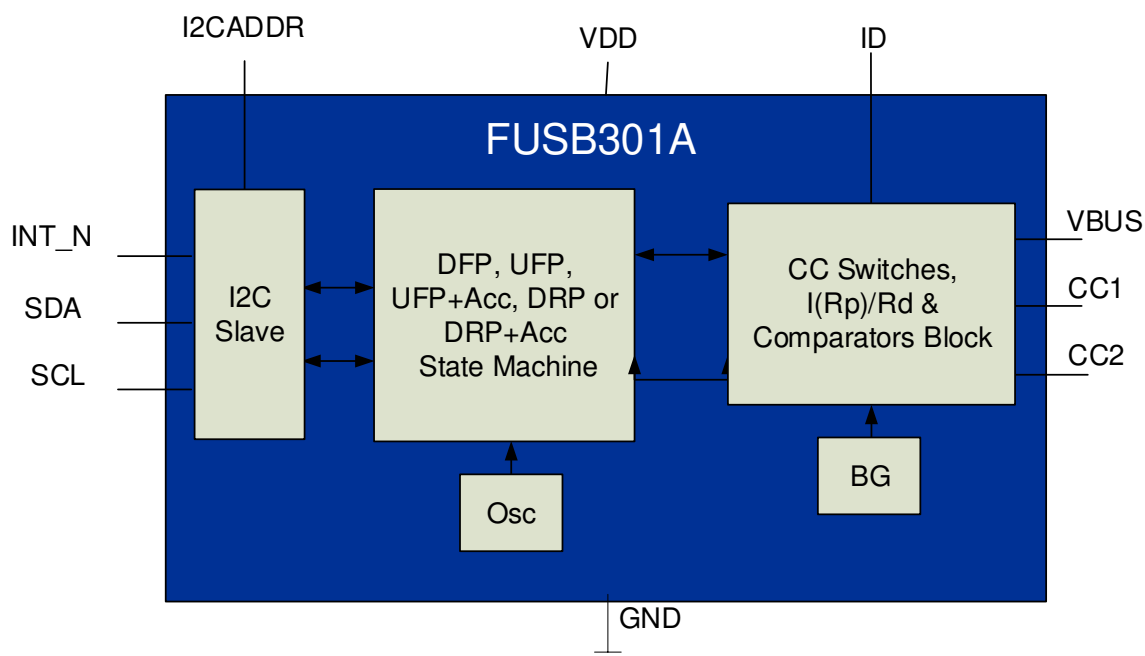


Figure 2. Block Diagram

## Pin Configuration

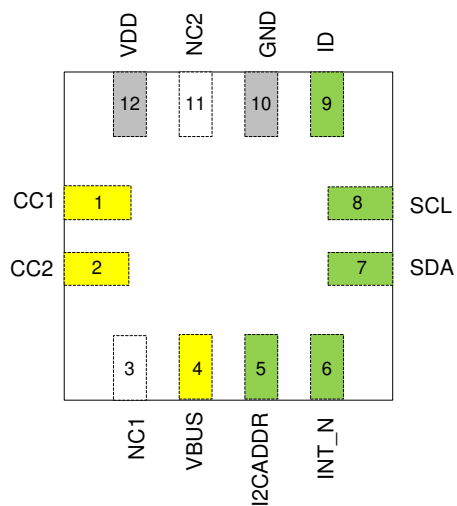


Figure 3. Pin Assignment (Top Through View)



## Pin Descriptions

| Pin #                                 | Name     | Type              | Description   |
|---------------------------------------|----------|-------------------|---|
| <b>USB Type-C Connector Interface</b> |          |                   |   |
| 1, 2                                  | CC1, CC2 | I/O               | Type-C Configuration Channel  |
| 4                                     | VBUS     | Input             | VBUS input pin for attach and detach detection  |
| 10                                    | GND      | Ground            | Ground  |
| <b>Power Interface</b>                |          |                   |   |
| 12                                    | VDD      | Power             | Input Supply Voltage  |
| <b>Signal Interface</b>               |          |                   |   |
| 8                                     | SCL      | Input             | I <sup>2</sup> C serial clock signal to be connected to the I <sup>2</sup> C master.  |
| 7                                     | SDA      | Open-Drain I/O    | I <sup>2</sup> C serial data signal to be connected to the I <sup>2</sup> C master  |
| 6                                     | INT_N    | Open-Drain Output | Active LOW open drain interrupt output used to prompt the processor to read the I <sup>2</sup> C register bits                  |
| 9                                     | ID       | Open-Drain Output | Used to Identify if connected device is Source or Sink. The ID Pin can be used to interface with USB2.0 Input on the processor. |
| 5                                     | I2CADDR  | Input             | Used to change bit 3 of the I2C address so that multiple addresses can be used in a system where two device addresses conflict  |
| 3                                     | NC1      | NC                | No Connect – Tie to Ground or Float   |
| 11                                    | NC2      | NC                | No Connect – Tie to Ground or Float   |

### Dead Battery

If power is not applied to FUSB301A and it is attached to a Source device, then the Source would pull up the CC line connected through the cable. The FUSB301A in response would turn on the pull-down that will bring the CC voltage to a range that the Source can detect an attach and turn on VBUS.

### Power Up, Initialization and Reset, Interrupt Operation

When power is first applied, the FUSB301A will power up in Sink mode with all interrupts masked. The local processor must configure the FUSB301A to the desired mode and clear the global interrupt mask bit, INT\_MASK. The INT\_N pin is an active low, open drain output. This pin indicates to the host processor that an interrupt has occurred in the FUSB301A which needs

attention. The INT\_N pin is in a high impedance state by default after power-up or device reset, and the global interrupt mask (INT\_MASK in Control register) is set. After INT\_MASK bit is cleared by the local processor, the INT\_N pin stays high impedance in preparation of future interrupts. When an interruptible event occurs, INT\_N is driven LOW and is in a high impedance state again when the processor clears the interrupt by reading the interrupt registers. Subsequent to the initial power up or reset; if the processor writes a “1” to global interrupt mask bit when the system is already powered up, the INT\_N pin stays in a high impedance state and ignores all interrupts until the global interrupt mask bit is cleared. If an event happens that would ordinarily cause an interrupt when the global interrupt mask bit is set, the INT\_N pin goes LOW when the global interrupt mask is cleared.

**Table 1. ID Pin Truth Table**

| TYPE Register (h12, bit 4) | Description       | ID             |
|----------------------------|-------------------|----------------|
| SINK = b0                  | SINK Not Detected | Hi-Z (default) |
| SINK = b1                  | SINK Detected     | Low            |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol                | Parameter   |                                    |         | Min. | Max. | Unit |
|-----------------------|---|------------------------------------|---------|------|------|------|
| V <sub>DD</sub>       | Supply Voltage from V <sub>DD</sub>                       |                                    |         | -0.5 | 6.0  | V    |
| V <sub>BUS</sub>      | VBUS supply voltage                                       |                                    |         | -0.5 | 28   | V    |
| V <sub>CC_HDDRP</sub> | CC pins when configured as Host, Device or Dual Role Port |                                    |         | -0.5 | 6.0  | V    |
| T <sub>STORAGE</sub>  | Storage Temperature Range                                 |                                    |         | -65  | +150 | C    |
| T <sub>J</sub>        | Maximum Junction Temperature                              |                                    |         |      | +150 | C    |
| T <sub>L</sub>        | Lead Temperature (Soldering, 10 seconds)                  |                                    |         |      | +260 | C    |
| ESD                   | IEC 61000-4-2 System ESD                                  | Connector Pins (VBUS, CC1 & CC2)   | Air Gap | 15   |      | kV   |
|                       |   |                                    | Contact | 8    |      |      |
|                       | Human Body Model, JEDEC JESD22-A114                       | Connector Pins (VBUS, CC1 and CC2) |         | 4    |      | kV   |
|                       |   | Others                             |         | 2    |      |      |
|                       | Charged Device Model, JEDEC LESD22-C101                   | All Pins                           |         | 1    |      |      |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol           | Parameter             | Min.               | Typ. | Max. | Unit |
|------------------|-----------------------|--------------------|------|------|------|
| V <sub>BUS</sub> | VBUS Supply Voltage   | 3.7                | 5.0  | 21   | V    |
| V <sub>DD</sub>  | Supply Voltage        | 2.8 <sup>(1)</sup> | 3.3  | 5.5  | V    |
| T <sub>A</sub>   | Operating Temperature | -40                |      | +85  | C    |

### Note:

1. This is for functional operation only and isn't the lowest limit for all subsequent electrical specifications below. All electrical parameters have a minimum of 3 V operation.

## DC and Transient Characteristics

Unless otherwise specified: Recommended T<sub>A</sub> and T<sub>J</sub> temperature ranges. All typical values are at T<sub>A</sub>=25°C and V<sub>DD</sub>=3.3 V unless otherwise specified.

| Symbol                     | Parameter  | T <sub>A</sub> = -40 to +85°C<br>T <sub>J</sub> =-40 to +125°C |      |      | Unit |
|----------------------------|--|--|------|------|------|
|                            |  | Min.   | Typ. | Max  |      |
| Type C Specific Parameters |  |  |      |      |      |
| I <sub>80_CCX</sub>        | Source 80 μA CC Current (Default) HOST_CUR1=0, HOST_CUR0=1               | 64   | 80   | 96   | μA   |
| I <sub>180_CCX</sub>       | SOURCE 180 μA CC Current (1.5 A) HOST_CUR1=1, HOST_CUR0=0                | 166  | 180  | 194  | μA   |
| I <sub>330_CCX</sub>       | SOURCE 330 μA CC Current (3 A) HOST_CUR1=1, HOST_CUR0=1                  | 304  | 330  | 356  | μA   |
| V <sub>SNKDB</sub>         | SINK Pull-Down Voltage in Dead Battery Under all Pull-up SOURCE Loads    |  |      | 2.18 | V    |
| R <sub>DEVICE</sub>        | Device Pull-Down Resistance when VDD is within Operating Range           | 4.6  | 5.1  | 5.6  | kΩ   |
| zOPEN                      | CC Resistance for Disabled State   | 126  |      |      | kΩ   |
| vRa-SRCdef                 | Ra Detection Threshold for CC Pin for Source for Default Current on VBUS | 0.15   | 0.20 | 0.25 | V    |
| vRa-SRC1.5A                | Ra Detection Threshold for CC Pin for Source for 1.5 A Current on VBUS   | 0.35   | 0.40 | 0.45 | V    |
| vRa-SRC3A                  | Ra Detection Threshold for CC Pin for Source for 3 A Current on VBUS     | 0.75   | 0.80 | 0.85 | V    |
| vRd-SRCdef                 | Rd Detection Threshold for Source for Default Current (HOST_CUR1/0=01)   | 1.50   | 1.60 | 1.65 | V    |
| vRd-SRC1.5A                | Rd Detection Threshold for Source for 1.5 A Current (HOST_CUR1/0=10)     | 1.50   | 1.60 | 1.65 | V    |
| vRd-SRC3A                  | Rd Detection Threshold for Source for 3 A Current (HOST_CUR1/0=11)       | 2.45   | 2.60 | 2.75 | V    |
| vRa-SNK                    | Ra Detection Threshold for CC Pin for Sink                               | 0.15   | 0.20 | 0.25 | V    |
| vRd-def                    | Rd Default Current Detection Threshold for Sink                          | 0.61   | 0.66 | 0.70 | V    |
| vRd-1.5A                   | Rd 1.5 A Current Detection Threshold for Sink                            | 1.16   | 1.23 | 1.31 | V    |
| vRd-3.0A                   | Rd 3 A Current Detection Threshold for Sink                              | 2.04   | 2.11 | 2.18 | V    |
| vVBUSthr                   | VBUS Threshold at which I_VBUSOK Interrupt is Triggered                  |  |      | 3.7  | V    |

## Current Consumption

| Symbol               | Parameter                                   | V <sub>DD</sub> (V) | Conditions                            | T <sub>A</sub> = -40 to +85°C<br>T <sub>J</sub> = -40 to +125°C |      |      | Unit |
|----------------------|---|---------------------|---------------------------------------|---|------|------|------|
|                      |   |                     |                                       | Min.  | Typ. | Max. |      |
| I <sub>disable</sub> | Disabled Current                            | 3.0 to 5.5          | Disabled State                        |   | 0.35 | 2.0  | μA   |
| I <sub>stby</sub>    | Unattached.Sink                             | 3.0 to 5.5          | Nothing attached                      |   | 3.5  | 7.0  | μA   |
|                      | Unattached Sink + Acc, Source + Acc, or DRP |                     | Nothing attached, Internally Toggling |   | 5    | 20   | μA   |
| I <sub>attach</sub>  | Attach Current (Less Host Current)          | 3.0 to 5.5          | Attached as a Sink                    |   | 5    | 15   | μA   |
|                      |   |                     | Attached as a Source                  |   | 10   | 15   |      |

## Timing Parameters

| Symbol                     | Parameter   |              | T <sub>A</sub> = -40 to +85°C<br>T <sub>J</sub> = -40 to +125°C |       |       | Unit |
|----------------------------|---|--------------|---|-------|-------|------|
|                            |   |              | Min.  | Typ.  | Max.  |      |
| t <sub>CCDebounce</sub>    | Debounce Time for CC (Source or Accessory)  |              | 100   | 150   | 200   | ms   |
|                            | Debounce Time for CC (Sink)   |              | 63  | 75    | 87    | ms   |
| t <sub>PDDebounce</sub>    | Debounce Time for CC Detach Detection   |              | 10  | 15    | 20    | ms   |
| t <sub>AccDetect</sub>     | Debounce Time to Detect AudioAccessory, or DebugAccessory is Attached                               |              | 50  | 100   | 200   | ms   |
| t <sub>ErrorRecovery</sub> | Time staying in the ErrorRecovery State if sent there via the ERROR_REC bit or by a change of Modes |              | 25  | 50    | 100   | ms   |
| t <sub>VBUSondeb</sub>     | Debounce Time of VBUS Detection when acting as a Sink to Signal VBUS is present                     |              | 0.167   | 0.200 | 0.375 | ms   |
| t <sub>VBUSoffdeb</sub>    | Debounce Time of VBUS Detection when acting as a Sink to Signal VBUS has been removed               |              | 10  | 15    | 20    | ms   |
| t <sub>DRPToggle1</sub>    | For DRP Operation, Time Spent in Unattached.Sink before going to Unattached.Source State            | DRPTOGGLE=00 | 35  |       | 70    | ms   |
|                            |   | DRPTOGGLE=01 | 30  |       | 60    | ms   |
|                            |   | DRPTOGGLE=10 | 25  |       | 50    | ms   |
|                            |   | DRPTOGGLE=11 | 20  |       | 40    | ms   |
| t <sub>DRPToggle2</sub>    | For DRP Operation, Time Spent in Unattached.Source before going to Unattached.Sink State            | DRPTOGGLE=00 | 15  |       | 30    | ms   |
|                            |   | DRPTOGGLE=01 | 20  |       | 40    | ms   |
|                            |   | DRPTOGGLE=10 | 25  |       | 50    | ms   |
|                            |   | DRPTOGGLE=11 | 30  |       | 60    | ms   |



## IO Specifications

| Symbol   | Parameter  | V <sub>DD</sub> (V) | Conditions                     | T <sub>A</sub> = -40 to +85°C<br>T <sub>J</sub> = -40 to +125°C |      |                    | Unit |
|--|--|---------------------|--------------------------------|---|------|--------------------|------|
|  |  |                     |                                | Min.  | Typ. | Max.               |      |
| Host Interface Pins (ID)                             |  |                     |                                |   |      |                    |      |
| V <sub>OLID</sub>                                    | Output Low Voltage   | 3.0 to 5.5          | I <sub>OL</sub> =4 mA          |   |      | 0.4                | V    |
| Host Interface Pins (I2CADDR)                        |  |                     |                                |   |      |                    |      |
| V <sub>ILADDR</sub>                                  | Low-Level Input Voltage                                    | 3.0 to 5.5          |                                |   |      | 0.3V <sub>DD</sub> | V    |
| V <sub>IHADDR</sub>                                  | High-Level Input Voltage                                   | 3.0 to 5.5          |                                | 0.7V <sub>DD</sub>  |      |                    | V    |
| Host Interface Pins (INT_N)                          |  |                     |                                |   |      |                    |      |
| V <sub>OLINTN</sub>                                  | Output Low Voltage   | 3.0 to 5.5          | I <sub>OL</sub> =4 mA          |   |      | 0.4                | V    |
| I <sup>2</sup> C Interface Pins – Fast Mode SDA, SCL |  |                     |                                |   |      |                    |      |
| V <sub>ILI2C</sub>                                   | Low-Level Input Voltage                                    | 3.0 to 5.5          |                                |   |      | 0.4                | V    |
| V <sub>IHI2C</sub>                                   | High-Level Input Voltage                                   | 3.0 to 5.5          |                                | 1.2   |      |                    | V    |
| V <sub>HYS</sub>                                     | Hysteresis of Schmitt Trigger Inputs                       | 3.0 to 5.5          |                                | 0.2   |      |                    | V    |
| I <sub>I2C</sub>                                     | Input Current of SDA and SCL Pins,                         | 3.0 to 5.5          | Input Voltage<br>0.26 V to 2 V | -10   |      | 10                 | μA   |
| I <sub>CCTI2C</sub>                                  | VDD Current when SDA or SCL is HIGH                        | 3.0 to 5.5          | Input Voltage<br>1.8 V         |   |      | 10                 | μA   |
| V <sub>OLSDA</sub>                                   | Low-Level Output Voltage at 3 mA Sink Current (Open-Drain) | 3.0 to 5.5          |                                | 0   |      | 0.3                | V    |
| C <sub>I</sub>                                       | Capacitance for Each I/O Pin <sup>(2)</sup>                | 3.0 to 5.5          |                                |   |      | 10                 | pF   |

**Note:**

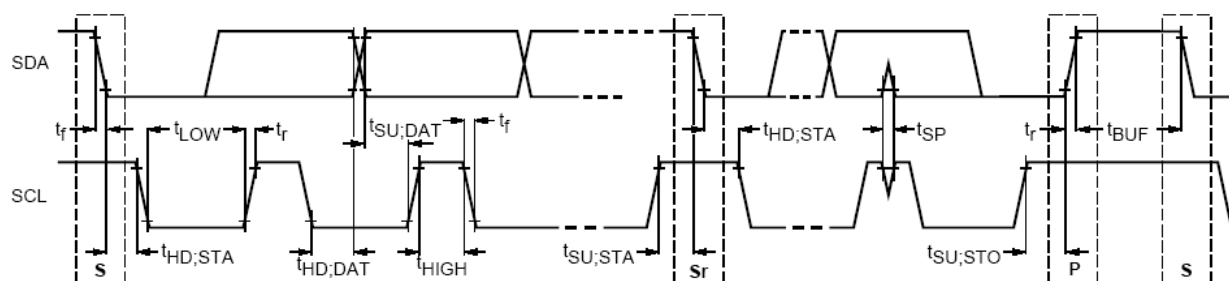
2. Guaranteed by characterization. Not production tested.

**Fast Mode I<sup>2</sup>C Specifications<sup>(3)</sup> (see Figure 4)**

| Symbol              | Parameter   | Fast Mode                   |      |      |
|---------------------|---|-----------------------------|------|------|
|                     |   | Min.                        | Max. | Unit |
| f <sub>SCL</sub>    | I2C_SCL Clock Frequency   | 0                           | 400  | kHz  |
| t <sub>HD;STA</sub> | Hold Time (Repeated) START Condition                              | 0.6                         |      | μs   |
| t <sub>LOW</sub>    | LOW Period of I2C_SCL Clock                                       | 1.3                         |      | μs   |
| t <sub>HIGH</sub>   | HIGH Period of I2C_SCL Clock                                      | 0.6                         |      | μs   |
| t <sub>SU;STA</sub> | Set-up Time for Repeated START Condition                          | 0.6                         |      | μs   |
| t <sub>HD;DAT</sub> | Data Hold Time  | 0                           | 0.9  | μs   |
| t <sub>SU;DAT</sub> | Data Set-up Time <sup>(4)</sup>                                   | 100                         |      | ns   |
| t <sub>r</sub>      | Rise Time of I2C_SDA and I2C_SCL Signals <sup>(5)</sup>           | 20*(V <sub>DD</sub> /5.5 V) | 250  | ns   |
| t <sub>f</sub>      | Fall Time of I2C_SDA and I2C_SCL Signals <sup>(5)</sup>           | 20*(V <sub>DD</sub> /5.5 V) | 250  | ns   |
| t <sub>SU;STO</sub> | Set-up Time for STOP Condition                                    | 0.6                         |      | μs   |
| t <sub>BUF</sub>    | BUS-Free Time between STOP and START Conditions                   | 1.3                         |      | μs   |
| t <sub>SP</sub>     | Pulse Width of Spikes that Must Be Suppressed by the Input Filter | 0                           | 50   | ns   |

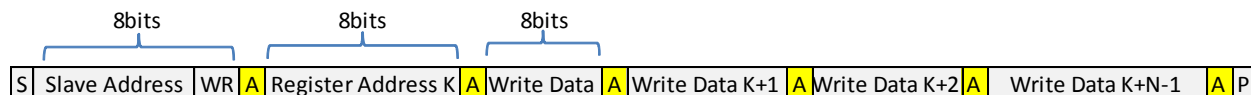
**Notes:**

- Guaranteed by characterization. Not production tested
- A fast-mode I<sup>2</sup>C-bus device can be used in a standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SU;DAT</sub> ≥ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C\_SCL signal. If such a device does stretch the LOW period of the I2C\_SCL signal, it must output the next data bit to the I2C\_SDA line t<sub>r\_max</sub> + t<sub>SU;DAT</sub> = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the I2C\_SCL line is released.
- C<sub>b</sub> equals the total capacitance of one bus line in pF. If mixed with high-speed devices, faster fall times are allowed according to the I<sup>2</sup>C specification.

**Figure 4. Definition of Timing for Full-Speed Mode Devices on the I<sup>2</sup>C Bus**

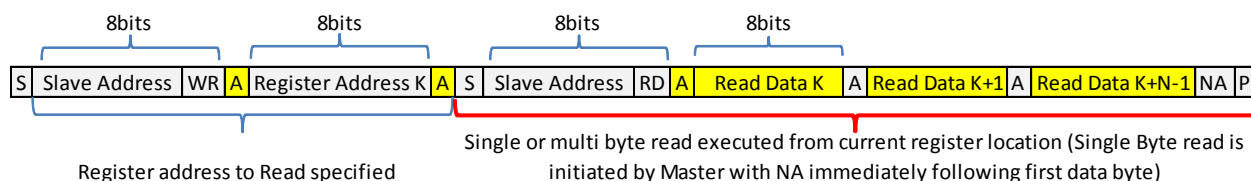
## I<sup>2</sup>C Interface

The FUSB301A includes a full I<sup>2</sup>C slave controller. The I<sup>2</sup>C slave fully complies with the I<sup>2</sup>C specification version 6 requirements. This block is designed for fast mode. Examples of an I<sup>2</sup>C write and read sequence are shown Figure 5 and Figure 6 respectively.





**Note:** Single Byte read is initiated by Master with P immediately following first data byte

**Figure 5. I<sup>2</sup>C Write Example**



**Note:** If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

|   |                      |          |                       |           |                            |           |                |
|---|----------------------|----------|-----------------------|-----------|----------------------------|-----------|----------------|
|  | From Master to Slave | <b>S</b> | Start Condition       | <b>NA</b> | NOT Acknowledge (SDA High) | <b>RD</b> | Read =1        |
|  | From Slave to Master | <b>A</b> | Acknowledge (SDA Low) | <b>WR</b> | Write=0                    | <b>P</b>  | Stop Condition |

**Figure 6. I<sup>2</sup>C Read Example**

## I<sup>2</sup>C Address

The I2CADDR bit high or low is indicated in bit3 of the slave address shown in Table 2.

**Table 2. FUSB301A I<sup>2</sup>C Slave Address**

| Name          | Size (Bits) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3   | Bit 2 | Bit 1 | Bit 0 |
|---------------|-------------|-------|-------|-------|-------|---------|-------|-------|-------|
| Slave Address | 8           | 0     | 1     | 0     | 0     | I2CADDR | 0     | 1     | R/W   |

## Register Definitions

**Table 3. Register Map**

| Address   | Register Name | Type | Rst Val | Bit7            | Bit6 | Bit5    | Bit4    | Bit3             | Bit2      | Bit1       | Bit0      |
|-----------|---------------|------|---------|-----------------|------|---------|---------|------------------|-----------|------------|-----------|
| 0x01      | Device ID     | RO   | 12      | Version ID[3:0] |      |         |         | Revision ID[3:0] |           |            |           |
| 0x02      | Modes         | R/W  | 04      |                 |      | DRP+ACC | DRP     | Sink+ACC         | Sink      | Source+ACC | Source    |
| 0x03      | Control       | R/W  | 03      | DRPTOGGLE       |      |         |         |                  | HOST_CUR1 | HOST_CUR0  | INT_MASK  |
| 0x04      | Manual        | W/C  | 00      |                 |      |         |         | UNATT_SNK        | UNATT_SRC | DISABLED   | ERROR_REC |
| 0x05      | Reset         | W/C  | 00      |                 |      |         |         |                  |           |            | SW_RES    |
| 0x06-0x0F | Reserved      | X    | xx      | Do Not Use      |      |         |         |                  |           |            |           |
| 0x10      | Mask          | R/W  | 00      |                 |      |         |         | M_ACC_CH         | M_BC_LVL  | M_DETACH   | M_ATTACH  |
| 0x11      | Status        | RO   | 00      |                 |      | ORIENT1 | ORIENT0 | VBUSOK           | BC_LVL1   | BC_LVL0    | ATTACH    |
| 0x12      | Type          | RO   | 00      |                 |      |         | Sink    | Source           |           | DEBUGACC   | AUDIOACC  |
| 0x13      | Interrupt     | R/C  | 00      |                 |      |         |         | I_ACC_CH         | I_BC_LVL  | I_DETACH   | I_ATTACH  |
| 0x14-0x1F | Reserved      | X    | xx      | Do Not Use      |      |         |         |                  |           |            |           |

### Notes:

6. Do not use registers that are blank
7. Values read from undefined register bits are invalid. Do not write to undefined registers.

**Table 4. Device ID**

Address: 01h

Reset Value: 0x0001\_0010

Type: Read Only

| Bit # | Name        | Size (Bits) | Description  |
|-------|-------------|-------------|--|
| 7:4   | Version ID  | 4           | Device version ID by Trim or etc.<br>A_[Version ID]: 0010 ( <b>FUSB301ATMX</b> ) |
| 3:0   | Revision ID | 4           | Revision History of each version<br>[Revision ID]_revC: 0010                     |

**Table 5. Modes**

Address: 02h

Reset Value: 0x0000\_0100

Type: Read/Write

| Bit # | Name       | Size (Bits) | Description   |
|-------|------------|-------------|---|
| 7:6   | Reserved   | 2           | Do Not Use  |
| 5     | DRP+ACC    | 1           | 1: Configure device as a Dual Role Port (DRP) with accessory support    |
| 4     | DRP        | 1           | 1: Configure device as a Dual Role Port (DRP) without accessory support |
| 3     | Sink+ACC   | 1           | 1: Configure device as a Sink with accessory support                    |
| 2     | Sink       | 1           | <b>1: Configure device as a Sink without accessory support</b>          |
| 1     | Source+ACC | 1           | 1: Configure device as a Source with accessory support                  |
| 0     | Source     | 1           | 1: Configure device as a Source without accessory support               |

**Table 6. Control**

Address: 03h

Reset Value: 0xXX00\_X011

Type: Read/Write

| Bit # | Name          | Size (Bits) | Description  |
|-------|---------------|-------------|--|
| 7:6   | Reserved      | 2           | Do Not Use   |
| 5:4   | DRPTOGGLE     | 1           | Selects different timing for Dual Role Port Toggle between Unattached.Sink State and Unattached.SOURCE State.<br><b>00: 35 ms min. in Unattached.Sink and 15 ms min. in Unattached.SOURCE</b><br>01: 30 ms min. in Unattached.Sink and 20 ms min. in Unattached.SOURCE<br>10: 25 ms min. in Unattached.Sink and 25 ms min. in Unattached.SOURCE<br>11: 20 ms min. in Unattached.sink and 30 ms min. in Unattached.SOURCE |
| 3     | Reserved      | 1           | Do Not Use   |
| 2:1   | HOST_CUR[1:0] | 2           | 1: Controls the pull-up current when device enabled as a Source<br>00: No Current<br><b>01: 80 <math>\mu</math>A – Default USB Power</b><br>10: 180 $\mu$ A – Medium Current Mode: 1.5 A<br>11: 330 $\mu$ A – High Current Mode: 3 A   |
| 0     | INT_MASK      | 1           | <b>1: Global interrupt mask to mask all interrupts</b>   |

**Table 7. Manual<sup>(8)</sup>**

Address: 04h

Reset Value: 0xFFFF\_0000

Type: Write/Clear

| Bit # | Name                    | Size (Bits) | Description  |
|-------|-------------------------|-------------|--|
| 7:4   | Reserved                | 4           | Do Not Use   |
| 3     | UNATT_SINK              | 1           | 1: Put device in Unattached.Sink State as defined in the Type C spec   |
| 2     | UNATT_SOURCE            | 1           | 1: Put device in Unattached.Source state as defined in the Type C spec |
| 1     | DISABLED <sup>(9)</sup> | 1           | 1: Put device in Disabled state as defined in the Type C spec          |
| 0     | ERROR_REC               | 1           | 1: Put device in ErrorRecovery state as defined in the Type C spec     |

**Notes:**

8. If more than one bit is set to “b1” simultaneously then an order of priority will be used. 1st priority is DISABLED, 2nd is ERROR\_REC, 3rd is UNATT\_SOURCE, last is UNATT\_SINK. The highest priority bit will take precedence and all other bits will be cleared automatically.
9. The DISABLED bit must be manually cleared.

**Table 8. Reset**

Address: 05h

Reset Value: 0xFFFF\_XXX0

Type: Write/Clear

| Bit # | Name     | Size (Bits) | Description                           |
|-------|----------|-------------|---------------------------------------|
| 7:6   | Reserved | 7           | Do Not Use                            |
| 0     | SW_RES   | 1           | 1: Reset the system and I2C Register. |

**Table 9. Mask**

Address: 10h

Reset Value: 0xFFFF\_0000

Type: Read/Write

| Bit # | Name     | Size (Bits) | Description   |
|-------|----------|-------------|---|
| 7:4   | Reserved | 4           | Do Not Use  |
| 3     | M_ACC_CH | 1           | 1: Mask a change from Accessory Present to Attached Accessory |
| 2     | M_BC_LVL | 1           | 1: Mask a change in I_BC_LVL interrupt bit                    |
| 1     | M_DETACH | 1           | 1: Mask the I_DETACH interrupt bit                            |
| 0     | M_ATTACH | 1           | 1: Mask a change in the I_ATTACH interrupt bit                |



**Table 10. Status**

Address: 11h

Reset Value: 0xXX00\_0000

Type: Read

| Bit # | Name        | Size (Bits) | Description  |
|-------|-------------|-------------|--|
| 7:6   | Reserved    | 2           | Do Not Use   |
| 5:4   | ORIENT[1:0] | 2           | Status to indicate which CCx pins has the CC cable connection<br>11: A fault has occurred during the detection<br>10: Cable CC is connected through the CC2 pin<br>01: Cable CC is connected through the CC1 pin<br><b>00: No or unresolved connection detected</b>                |
| 3     | VBUSOK      | 1           | 1: Status to indicate VBUS is in the valid range   |
| 2:1   | BC_LVL[1:0] | 2           | Thresholds that allow detection of current advertisement on CC line<br><b>00: Ra or unattached Sink</b><br>01: Rd threshold for Sink default current advertisement<br>10: Rd threshold for Sink 1.5 A current advertisement<br>11: Rd threshold for Sink 3 A current advertisement |
| 0     | ATTACH      | 1           | 1: Attached to a device or accessory of a type shown in the Type register  |

**Table 11. Type**

Address: 12h

Reset Value: 0xXXX0\_0X00

Type: Read

| Bit # | Name     | Size (Bits) | Description                                      |
|-------|----------|-------------|--|
| 7:5   | Reserved | 3           | Do Not Use                                       |
| 4     | Sink     | 1           | 1: Indicates a Sink has been detected            |
| 3     | Source   | 1           | 1: Indicates a Source has been detected          |
| 2     | Reserved | 1           | Do Not Use                                       |
| 1     | DEBUGACC | 1           | 1: Indicates a Debug Accessory has been detected |
| 0     | AUDIOACC | 1           | 1: Indicates a Audio Accessory has been detected |

**Table 12. Interrupt0**

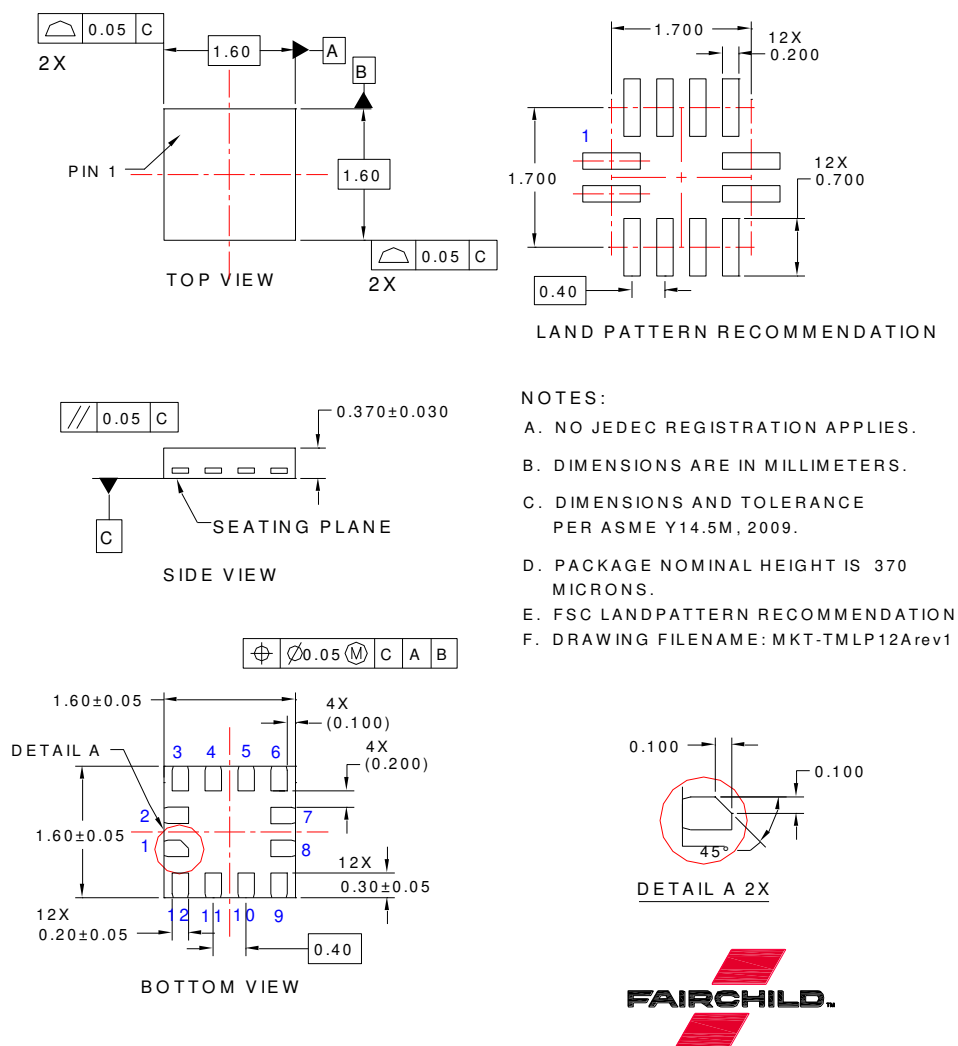
Address: 13h

Reset Value: 0xFFFF\_X000

Type: Write/Clear

| Bit # | Name     | Size (Bits) | Description  |
|-------|----------|-------------|--|
| 7:4   | Reserved | 5           | Do Not Use   |
| 3     | I_ACC_CH | 1           | 1: Interrupt flagged when a change from Accessory Present to Audio Accessory or Debug Accessory occurs   |
| 2     | I_BC_LVL | 1           | 1: Interrupt flagged when a change in BC_LVL advertised current level has occurred                       |
| 1     | I_DETACH | 1           | 1: Interrupt flagged when a device or accessory has been detached  |
| 0     | I_ATTACH | 1           | 1: Interrupt flagged when a device or accessory of type indicated in the Type register has been attached |

## Physical Dimensions



**Figure 7. 12 Lead, TMLP, Quad, Ultra-Thin MLP, 1.6 mm x 1.6 mm x 0.375 mm**

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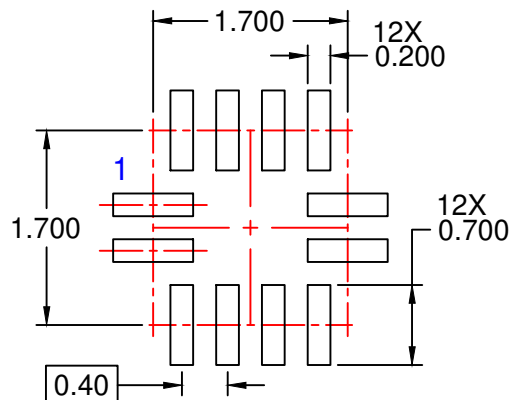
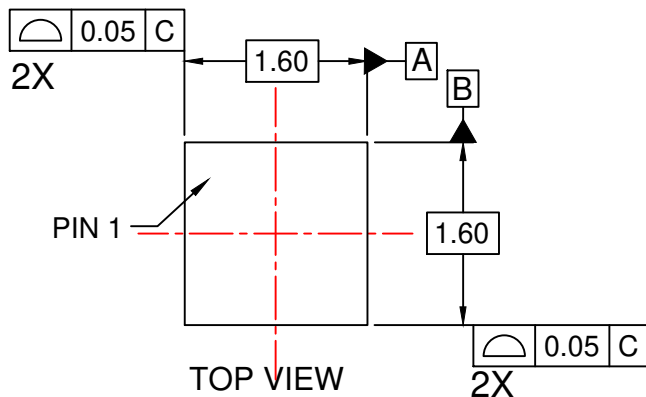
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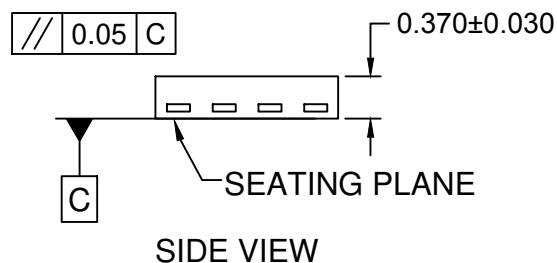
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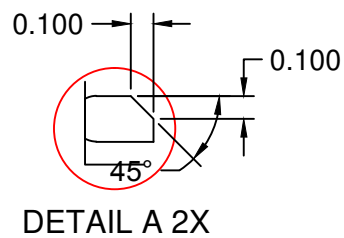
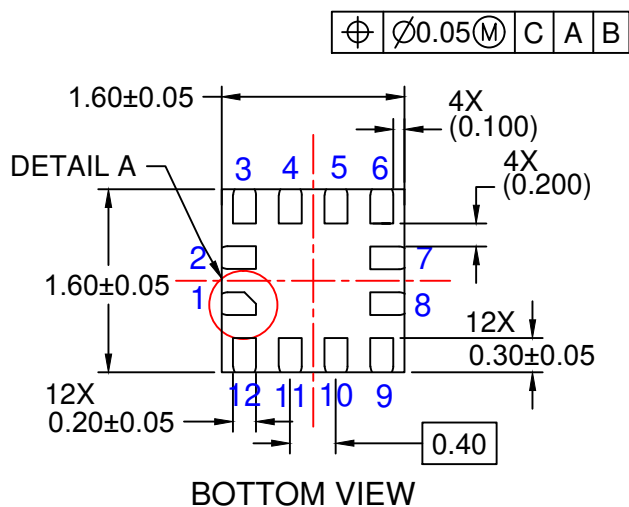



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