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FUSB307B

USB Type-C Port Controller with USB-PD

Description

The FUSB307B targets system designers looking to implement up to four USB Type−C port controllers (TCPC) with USB−PD capabilities.

This solution provides integrated Type−C Rev 1.3 detection circuitry enabling manual attach/detach detection. Time critical Power Delivery functionality is handled autonomously, offloading the µProcessor or Type−C Port Manager (TCPM).

The FUSB307B complies with the USB−PD Interface Specification Rev 1.0 as a TCPC for a standardized interface with TCPM.

Features

- USB−PD Interface Specification Rev 1.0 Ver. 1.2 Compatible
- USB Type−C Rev 1.3 Compatible
- USB−PD Rev3.0 Ver. 1.1 Compatible
- Fast Role Swap
- Sink Transmit
- Extended Data Messages (Chunked)
- Dual−Role Functionality
  - Manual Type−C Detection
  - Automatic DRP Toggling
- USB−PD Interface Specification Support
  - Automatic GoodCRC Packet Response
  - Automatic Retries of Sending Packet
  - All SOP* Types Supported
- VBUS Source and Sink Control
- Integrated 3 W Capable VCONN to CCx Switch
- 10−bit VBUS ADC
- Programmable GPIOs
- 4 Selectable I^2C Addresses

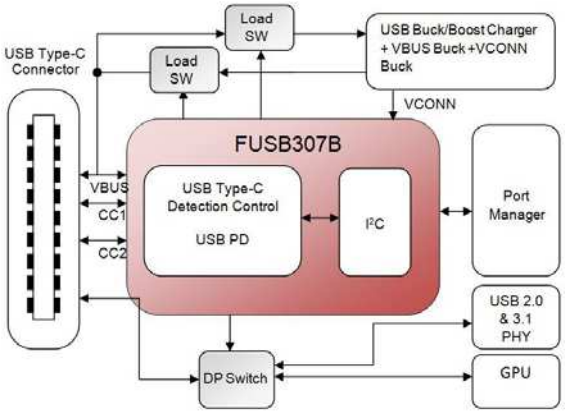

Figure 1. FUSB307B Block Diagram

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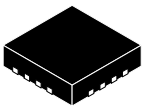
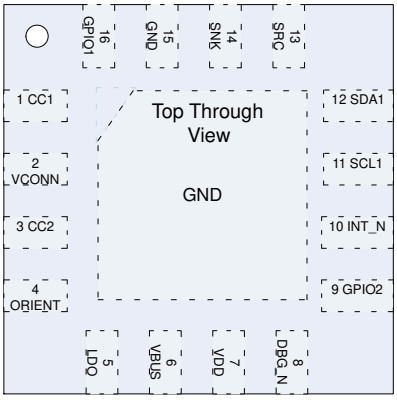


SCALE 3:1
WQFN16 3 x 3, 0.5P
CASE 510BS

PIN ASSIGNMENT



QFN16

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

Features (continued)

- Dead Battery Operation
  - Powered from VBUS
  - LDO Output Provides Power to TCPM
- Packaging:
  - FUSB307B− 16 Pin QFN

Applications

- Smartphones and Tablets
- Digital Cameras
- Desktops and Laptops
- Rechargeable Docks/Speakers
- Wall Adapters
- Automotive

Table of Contents

Table 1. ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method†
FUSB307BMPX	–40 to 85°C	16–Lead Molded Leadless Package (QFN) JEDEC, ML220, 3 mm Square	Tape and Reel
FUSB307BVMPX	Automotive –40 to 105°C		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Typical Application

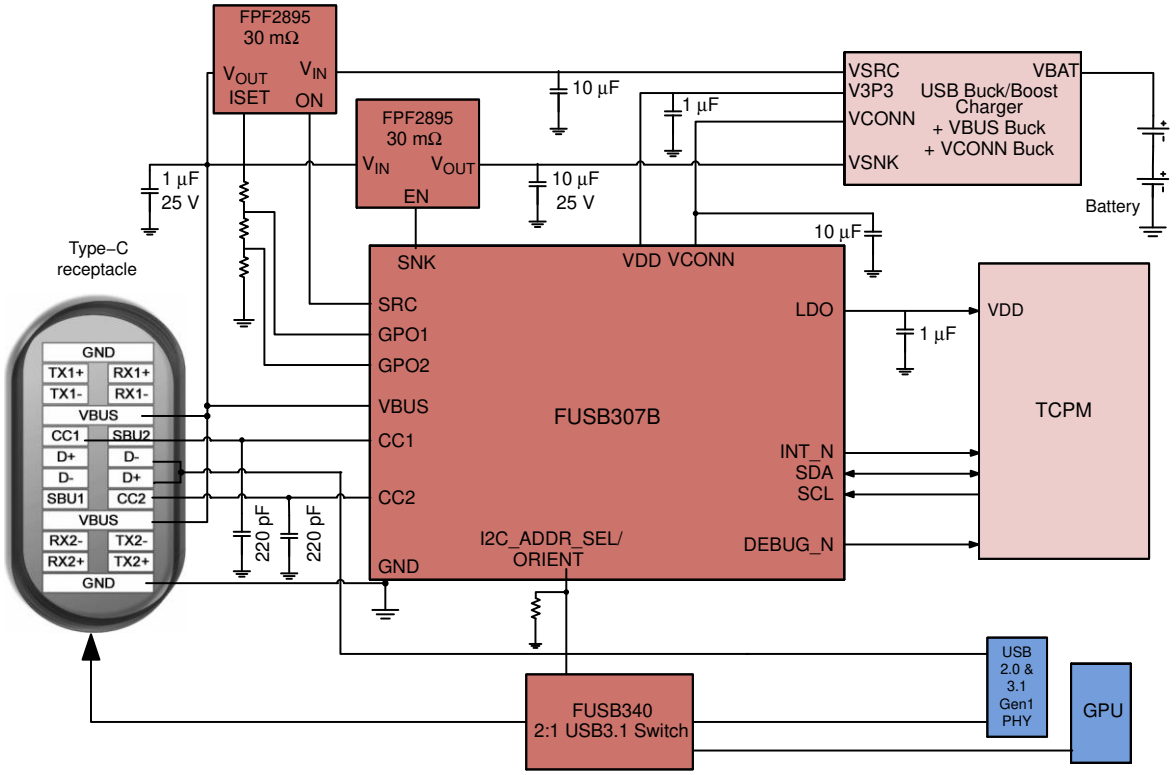


Figure 2. FUSB307B Typical Mobile Computing Application

Block Diagram

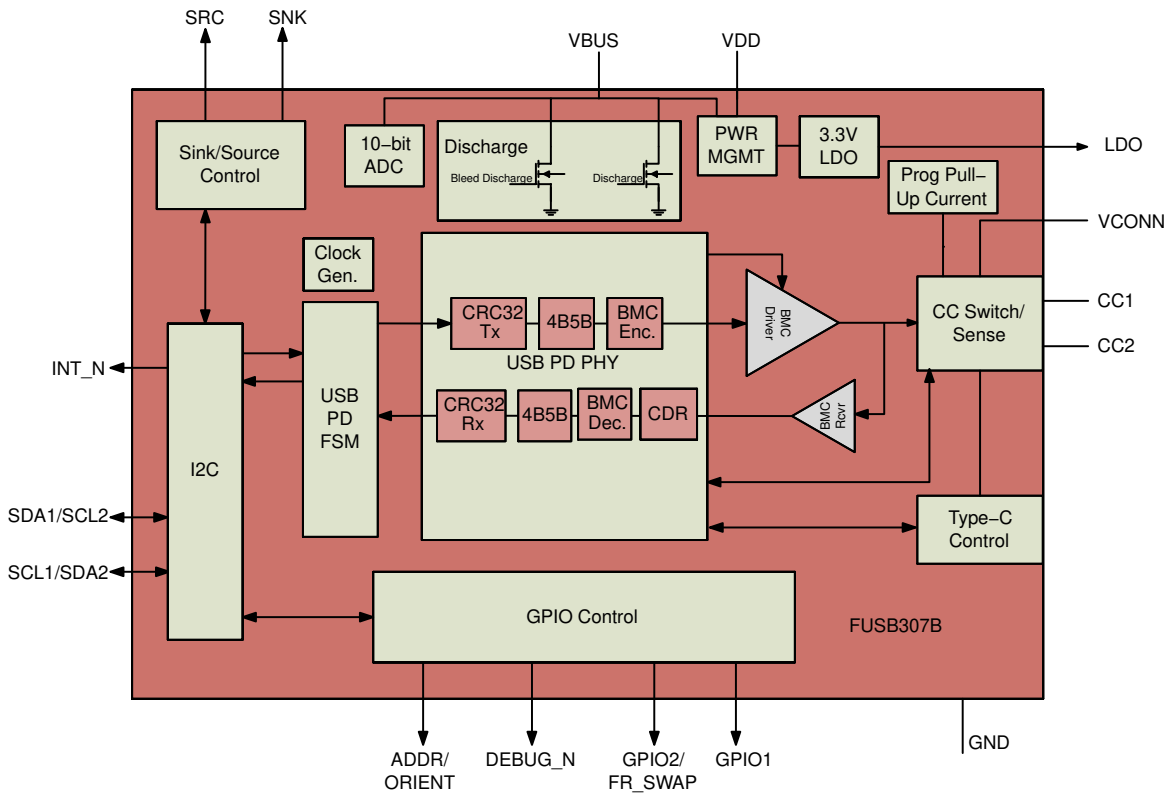


Figure 3. FUSB307B Block Diagram

Pin Configurations

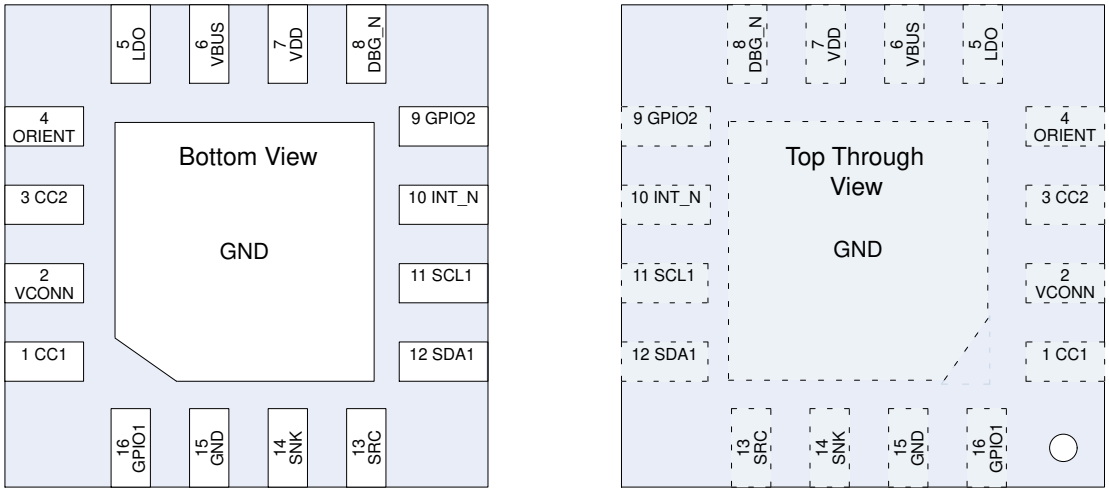


Figure 4. Pin Assignment QFN (FUSB307B)

Pin Descriptions

Table 2. PIN DESCRIPTION

Name	Type	Description
USB TYPE−C CONNECTOR INTERFACE		
CC1	I/O	Type−C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation of the insertion is. Functionality after attach depends on mode of operation detected. Operating as a host: − Sets the allowable charging current for VBUS to be sensed by the attached device − Used to communicate with devices using USB BMC Power Delivery − Used to detect when a detach has occurred Operating as a device: − Indicates what the allowable sink current is from the attached host − Used to communicate with devices using USB BMC Power Delivery
CC2	I/O	
GND	Ground	Ground
VBUS	Power	VBUS supply pin for attach and detach detection when operating as an upstream facing port (Device)
POWER INTERFACE		
VDD	Power	Input supply voltage
LDO	LDO Output	3.3 V LDO Output
VCONN	Power Switch	Regulated input to be switched to correct CC pin as VCONN to power USB3.1 fully featured cables, powered accessories or dongles bridging Type C to other video or audio connectors
SIGNAL INTERFACE		
SCL1/SDA2 (Note 1)	Open−Drain I/O	I^2C serial clock/data signal to be connected to the I^2C master
SDA1/SCL2 (Note 1)	Open−Drain I/O	I^2C serial clock/data signal to be connected to the I^2C master
INT_N	Open−Drain Output	Active LOW open drain interrupt output used to prompt the processor to read the I^2C register bits
ORIENT/I2C_ ADDR (Note 1)	3−State CMOS Output	Selects I^2C Address on Power up and then becomes a General Purpose CMOS Output
DBG_N	Open−Drain I/O	Debug Accessory Detection Open−Drain Output
GPIO2	3−State CMOS I/O	General Purpose I/O 2
GPIO1	3−State CMOS I/O	General Purpose I/O 1
VBUS SOURCE AND SINK INTERFACE		
SNK	CMOS Output	Controls external VBUS Sink Load Switch on/off (Active High)
SRC	CMOS Output	Controls external VBUS Source Load Switch on/off (Active High)

1. A different I2C address is used depending on which SDA and SCL are used and the state of ORIENT/I2C_ADDR at power up.

Power Up, Initialization and Reset

When power is first applied to VDD or VBUS, the FUSB307B goes through its POR sequence to load up all the default values in the register map, read all the fuses so that the trimmed values are available when VDD or VBUS is in its valid range. A software reset can be executed by writing SW_RES to 1 in RESET Register. This executes a full reset of the FUSB307B similar to POR where all the I2C registers go to their default state.

When powered down, the FUSB307B is configured as a UFP with CC1 and CC2 have their respective Rd pull−downs enabled such that a SOURCE can detect this as a UFP and turn on VBUS.

For the FUSB307B device, power may become available from VBUS when VDD is not present. This state is still considered “Dead Battery” until VDD is present. During Dead Battery, the FUSB307B will continue presenting Rd.

Once VDD is available, the TCPM can start the DRP toggle by setting COMMAND.LOOK4CON on the FUSB307B device.

Dead Battery Power−up

During a dead battery condition in a mobile application, the FUSB307B will be powered by VBUS and provide an LDO output to power a µController or TCPM to establish a USB−PD contract.

The FUSB307B will enable the Sink Path when attached to a source with any advertised current.

Systems with more than one Type−C port, the TCPM can enable or disable the appropriate sink paths.

Once VDD is greater than V_{DDGOOD}, the internal LDO is bypassed and the device switches from VBUS to VDD power.

Figure 5 demonstrates a dead battery power up sequence for FUSB307B.

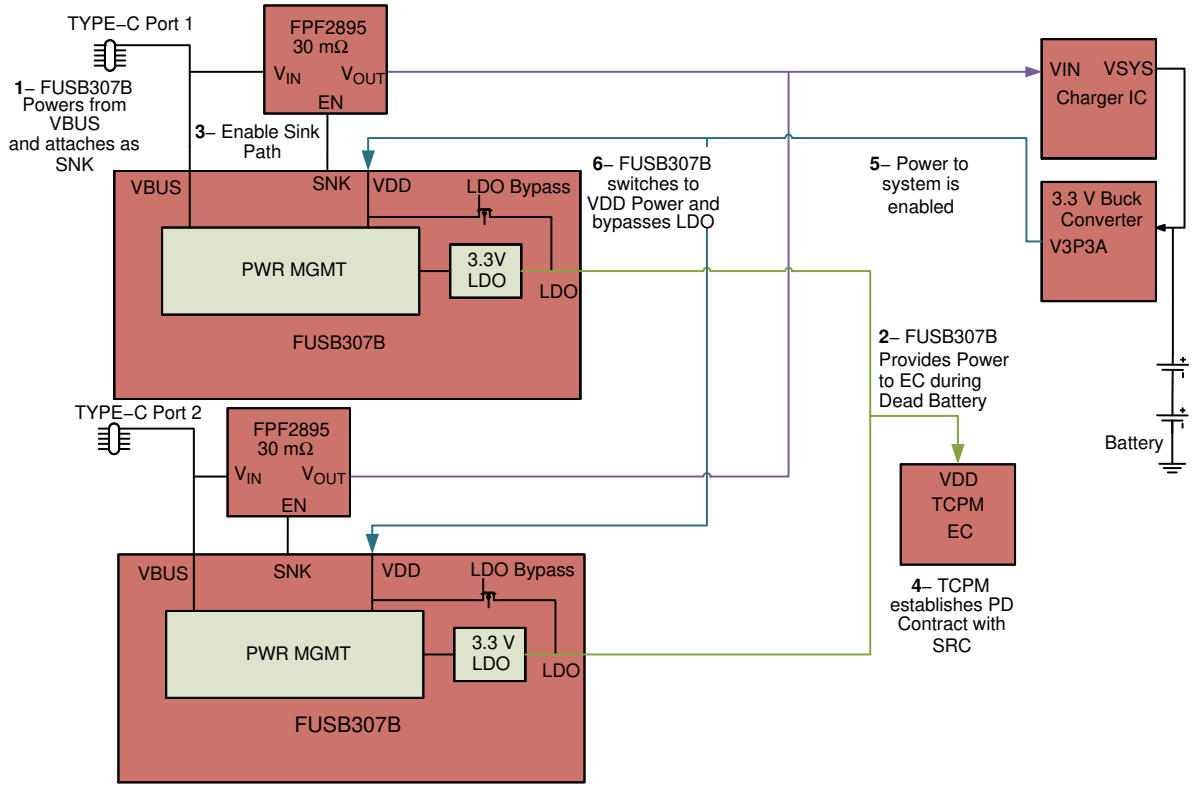


Figure 5. FUSB307B Dead Battery Operation

Programmable GPIOx

The FUSB307B has two programmable GPIOs. These can be programmed to be Inputs, CMOS Outputs or Open Drain Outputs. To configure them, the TCPM writes to GPIO1_CFG and GPIO2_CFG. If the GPIO is configured as an input, its logic value can be read in GPIO_STAT and ALERT_VD registers.

Standard Outputs

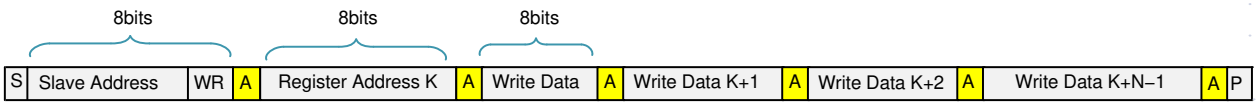
The FUSB307B implements Orientation and supports Debug Accessory detection output as indicated in STD_OUT_CAP register.

To configure the Orientation, Mux selection, and Debug Accessory, the TCPM writes to STD_OUT_CFG.

I²C Interface

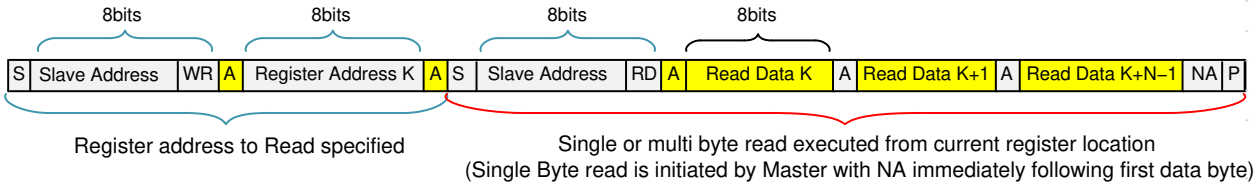
The FUSB307B includes a full I²C slave controller. The I2C slave fully complies with the I2C specification version 6 requirements. This block is designed for fast mode plus signals.

Examples of an I²C write and read sequence are shown in Figure 7 and Figure 8 respectively.



NOTE: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 6. I2C Write Example



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

From Master to Slave
From Slave to Master

S Start Condition
A Acknowledge (SDA Low)
NA NOT Acknowledge (SDA High)
WR Write = 0
RD Read =1
P Stop Condition

Figure 7. I2C Read Example

I²C Address Selection

I2C Slave addresses can be changed by configuring the I2C_ADDR_GPO input on power up with a pull−up or pull−down resistor and routing the SCL and SDA lines according to Table 3.

Interrupt Operation

The INT_N pin is an active low, open drain output which indicates to the host processor that an interrupt has occurred in the FUSB307B which needs attention. The INT_N pin is asserted after power−up or device reset RESET.SW_RES set to 1b (due to ALERTL.I_PORT_PWR and PWRSTAT.TCPC_INIT).

When an interruptible event occurs, INT_N is driven low and is high−Z again when the processor clears the interrupt by writing a 1 to the corresponding interrupt bit position. Writing a 0 to an interrupt bit has no effect.

A processor firmware has additional control of INT_N through individual event mask bits which can be set or cleared to enable or disable INT_N from being driven low when each event occurs.

Table 3. I²C ADDRESSES

I2C_ADDR	SCLx/SDAx	Slave Address							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SCL1/SDA1	1	0	1	0	0	0	0	R/W
1	SCL1/SDA1	1	0	1	0	0	0	1	R/W
0	SCL2/SDA2	1	0	1	0	0	1	0	R/W
1	SCL2/SDA2	1	0	1	0	0	1	1	R/W

I²C Idle Mode

Entering I²C Idle Mode

The FUSB307B does not need to enter I²C Idle Mode in order to save power. Entering this mode has no effect on I²C function. The FUSB307B can enter idle mode if 0xFF is written to the COMMAND register. Once in Idle mode, the FUSB307B will not set the PWRSTAT.TCPC_INIT to one.

Exiting I²C Idle Mode

The FUSB307B will exit I²C Idle mode when any I²C communication is addressed to the slave. The ALERTL.I_PRT_PWR interrupt will be set and no PWRSTAT bits will be set.

The device's I²C block is always on without power penalties.

VCONN Control

The FUSB307B integrates a CCx to VCONN switch with programmable OCP capability via the VCONN_OCP register. If PWRCTRL.VCONN_PWR is set to 0, the standard VCONN current limit is used (210.5 mA). If PWRCTRL.VCONN_PWR is set to 1, the programmable VCONN_OCP is used.

The VCONN switch can be enabled via the PWRCTRL register bits EN_VCONN and TCPC_CTRL.ORIENT bits (for CC1/2 selection).

A VCONN valid voltage is monitored and reported on PWRSTAT.VCONN_VAL. The valid voltage threshold is fixed at 2.4 V.

Debug Accessory Support

The FUSB307B implements autonomous detection of Source and Sink debug accessories. A debug accessory detection is indicated via a standard output. The FUSB307B powers on looking for a debug accessories without processor intervention.

If debug accessory detection is not wanted, the processor can write TCPC_CTRL.DEBUG_ACC_CTRL = 1b.

Type−C Manual Mode Detection

The CC pull up (Rp) or pull down (Rd) resistors and DRP toggle are setup via the ROLECTRL register.If a TCPM wishes to control Rp/Rd directly, it can write ROLECTRL.DRP = 0b and the desired ROLECTRL bits [3:0] (CC1/CC2).

The FUSB307B can autonomously toggle the Rp/Rd by setting ROLECTRL.DRP = 1b and the starting value of Rp/Rd in ROLECTRL.bits [3:0]. DRP toggling starts by writing to the COMMAND register

If ROLECTRL.DRP = 1b, the only allowed values for CC1/CC2 in ROLECTRL bits [3:0] are Rp/Rp or Rd/Rd.

When ROLECTRL bits 3:0 are set to Open and ROLECTRL.DRP = 0b, the PHY and CC comparators are powered down.

The FUSB307B updates the CCSTAT register on a Connect, Disconnect, a change in ROLECTRL.DRP or a change (tTCPCFilter debounced) on the CC1 or CC2 wire.

The TCPM reads CCSTAT upon detecting an interrupt and seeing the ALERTL.I_CCSTAT = 1. The FUSB307B indicates the DRP status, the DRP result, and the current CC status in this register.

The FUSB307B will set CCSTAT.LOOK4CON = 0b when it has stopped toggling as a DRP.

The TCPM reads the CCSTAT.LOOK4CON to determine if the FUSB307B is toggling Rp/Rd when operating as a DRP, it then reads CCSTAT.CON_RES to determine if the FUSB307B is presenting an Rp or Rd and read the CCSTAT.CC1_STAT and CCSTAT.CC2_STAT to determine the CC1 and CC2 states.

The FUSB307B debounces the CC lines for tTCPCfilter before reporting the status on CCSTAT. The TCPM must complete the debounce as defined in Type−C Specification.

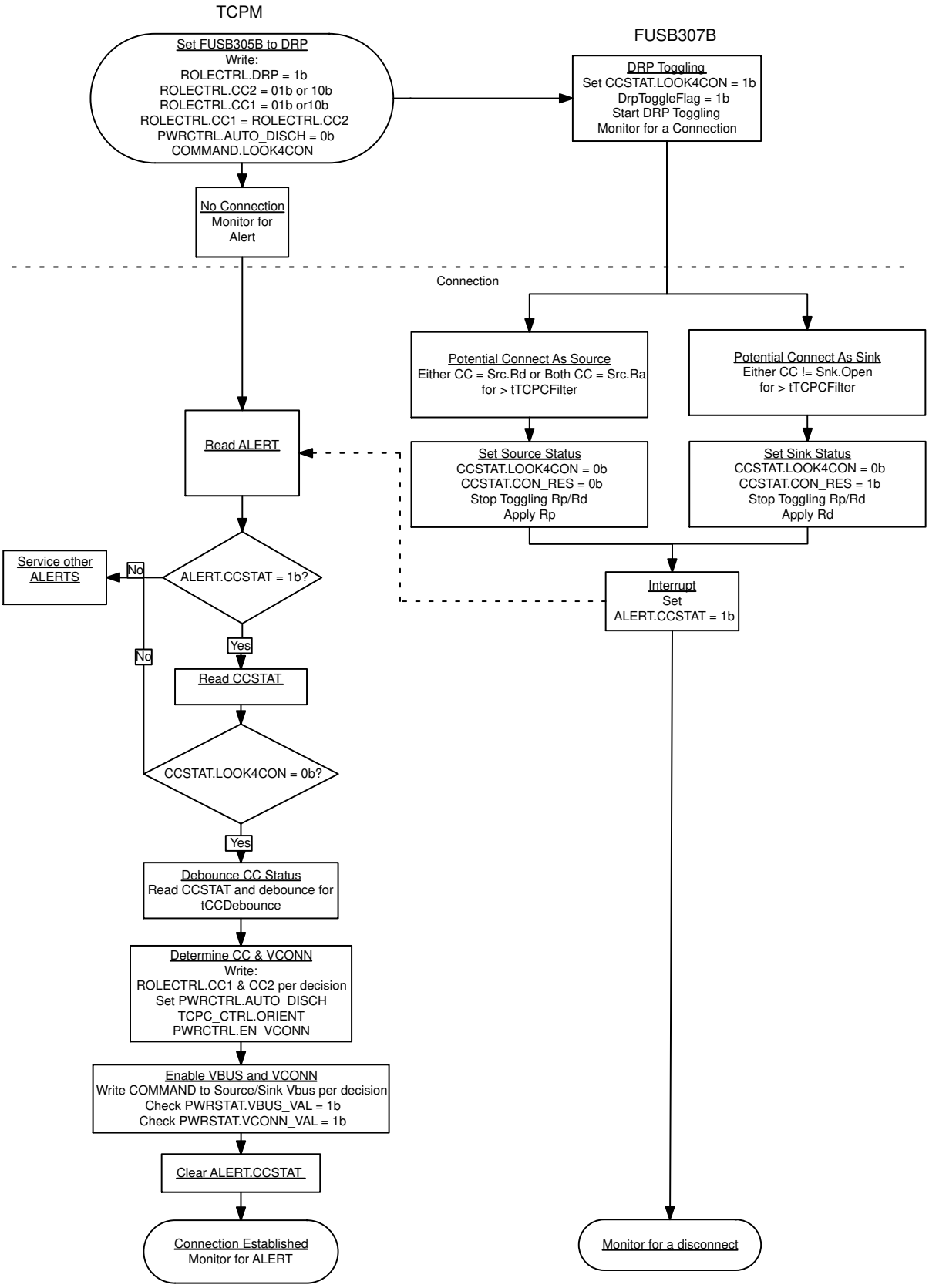


Figure 8. DRP Initialization and Connection Detection

BMC Power Delivery

The Type−C connector allows USB Power Delivery (PD) to be communicated over the connected CC pin between two ports. The communication method is the BMC Power Delivery protocol and is used for many different reasons with the Type−C connector. Possible uses are outlined below.

- Negotiating and controlling charging power levels
- Alternative Interfaces such as MHL, Display Port
- Vendor specific interfaces for use with custom docks or accessories
- Role swap for dual−role ports that want to switch who is the host or device
- Communication with USB3.1 full featured cables

The FUSB307B integrates a thin BMC PD client which includes the BMC physical layer and packet buffers which allows packets to be sent and received by the host software through I^2C accesses.

Receive State Machine

The TCPM can setup the desired types of messages to be received by the FUSB307B via the RXDETECT register. This register defaults to 0x00 (Receiver disabled) upon power up, reset, Hard Reset transmission and reception, and upon detecting a cable disconnect. A message is not received unless it is first enabled. Figure 9 shows the FUSB307B receive state machine.

Upon a successfully transmitting GoodCRC, the RXSTAT register is updated with the type of message received and the TCPM is alerted via ALERTL.I_RXSTAT bit (see transition from PRL_Rx_Send_GoodCRC to PRL_Rx_Report_SOP* in Figure 9). The total number of bytes in the receive buffer RXDATA is stored in RXBYTECNT This number includes the header bytes that are stored in RXHEADL and RXHEADH and the RXSTAT register.

The RXBYTECNT, RXSTAT registers and the internal receive buffer will be cleared after the ALERTL.I_RXSTAT bit is cleared.

The FUSB307B will automatically transmit a GoodCRC message for valid enabled messages within tTransmit.

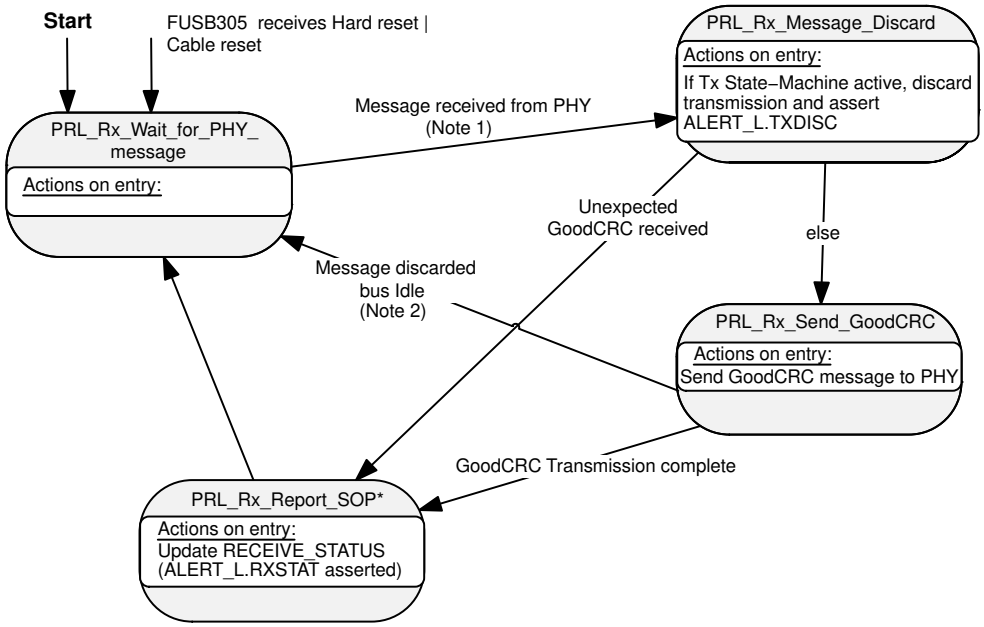
A received message is valid when:

- It is not a GoodCRC message
- The calculated CRC is correct
- The SOP* type is enabled

The makeup of the GoodCRC message is formed by the received SOP* type and the contents of MSGHEADR register.

When an expected GoodCRC message or a Hard Reset signaling is received, they will not be replied with a GoodCRC message (see Note 2 in Figure 9). If a GoodCRC message received was not expected due to the SOP* type or mismatched Message ID, the receive state machine will not send a GoodCRC message and will transition to PRL_Rx_Report SOP* to inform the TCPM.

If a Hard Reset message is received, the FUSB307B will reset the RXDETECT preventing the reception of future messages until the TCPM re−enables it.



1. This indication is sent by the PHY when a message has been discarded due to CC being busy, and after CC becomes idle again (see USB PD Spec).
2. Messages do not include Hard Reset or Cable Reset signals or expected GoodCRC messages (GoodCRC messages are only expected after the FUSB305 PHY has received the tx message and the FUSB305 Tx state−machine is in the PRL_Tx_Wait_for_PHY_response state).

Figure 9. Receive State Machine

Transmit State Machine

To transmit a message, the TCPM must first write the entire message in the following registers: TXHEADL, TXHEADH, TXBYTECNT and the TXDATA.

The actual transmission starts when the TCPM writes the TRANSMIT register.

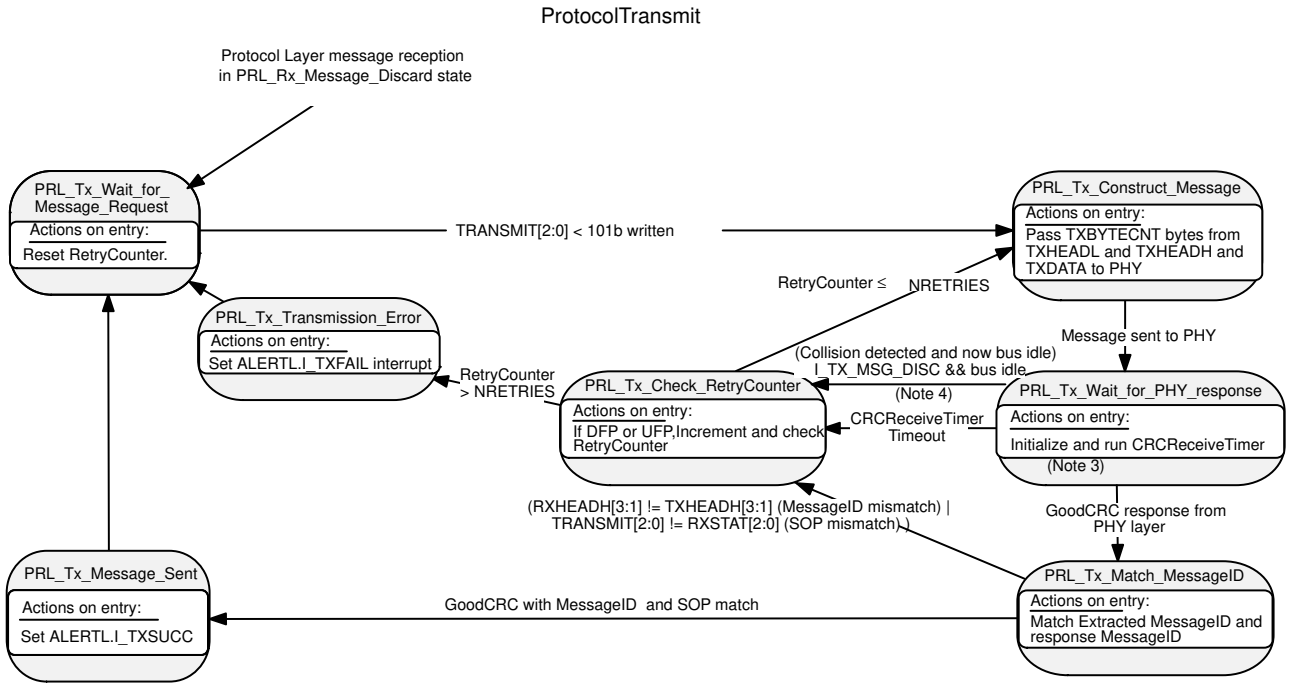
The TRANSMIT register is where the message selection is done and it must be written once per transmission.

The TRANSMIT and TXBYTECNT will be reset after executing a successful or failed transmission.

If the TRANSMIT.RETRY_CNT is set to a number greater than 0, the FUSB307B will automatically retry sending the same message if a GoodCRC is not received within tCRCReceiveTimer. An automatic retry is not performed when sending Hard−Resets, Cable−Resets, or BIST Carrier Mode 2 signaling.

The TCPM must not write the TRANSMIT register again until ALERTL.I_TXSUCC, I_TXFAIL, I_TX_DISC have been asserted and cleared.

The TCPM will not write the TRANSMIT register to request a transmission other than a Hard reset until it has cleared all received message alerts. If a TRANSMIT is written when ALERTL.I_RXSTAT = 1 or ALERTL. I_RXHRDRST = 1, the transmit request is discarded and ALERTL.I_TX_DISC is asserted.



3. The CRCReceiveTimer is only started after the FUSB305 has sent the message. If the message is not sent due to a busy channel then the CRCReceiveTimer will not be started.
4. This Indication is sent by the PHY layer when a message has been discarded due to CC being busy, and after CC becomes idle again. The CRCReceiveTimer is not running in this case since no message has been sent.

Figure 10. Receive State Machine

Hard Reset/ Cable Reset State Machine

The TCPM will write the TRANSMIT register to initiate the Hard Reset/Cable Reset state machine, see Figure 11. If a the FUSB307B is in the middle of a transmission when instructed to send a Hard or Cable reset, it will set the ALERTL.I_TXDISC bit and send the hard reset signaling as soon as possible. The FUSB307B implements the HardResetCompleteTimer. A Hard Reset or Cable Reset will be attempted until the HardResetCompleteTimer times out. After a successful transmission or timeout, the FUSB307B will indicate that a Hard Reset or Cable Reset has been sent by asserting both ALERTL.I_TXSUCC and ALERTL.I_TXFAIL registers simultaneously. The bits in RXDETECT and RXBYTECNT will be reset to disable PD message passing after a Hard Reset is received or transmitted.

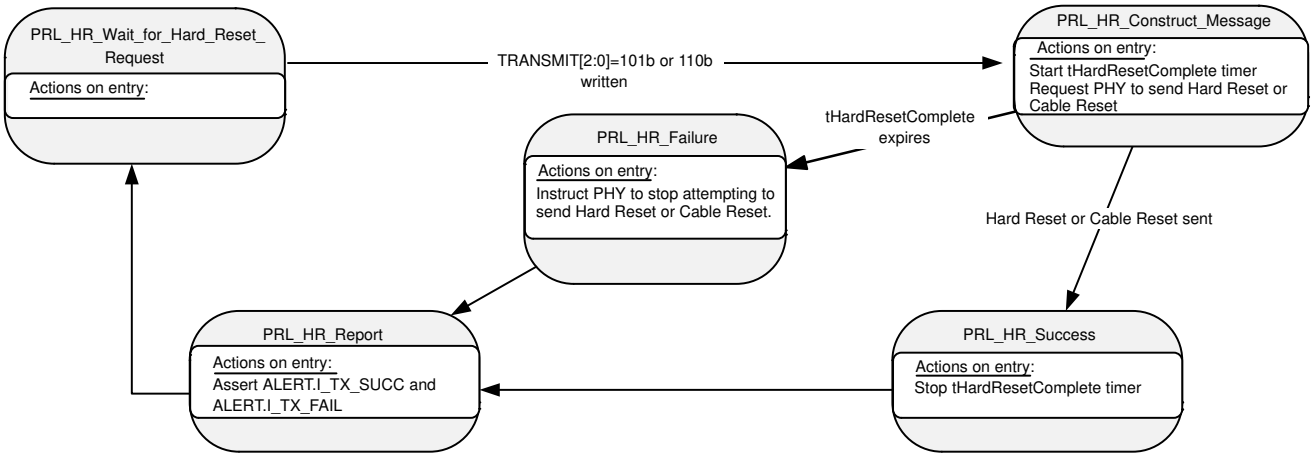


Figure 11. Hard Reset and Cable Reset State Machine

Automatic GoodCRC Response

Power Delivery packets require a GoodCRC acknowledge packet to be sent for each received packet where the calculated CRC is the correct value. This calculation is done by the FUSB307B.

The FUSB307B will automatically send the GoodCRC control packet in response to alleviate the local processor from responding quickly to the received packet. Once the GoodCRC packet is sent the FUSB307B will trigger the ALERTL.I_RXSTAT interrupt.

The following sequence of events occur internally within the FUSB307B without processor intervention when it is determined that the receive message has the correct CRC. If the host processor attempts a packet transmission during an Automatic GoodCRC response, the FUSB307B will set the ALERTL.I_TXDISC bit interrupting the processor. The processor should only transmit a new packet once ALERTL.I_TXSUCC or ALERTL.I_TX_FAIL has been received.

It is assumed that the processor will set the PWRCTRL.ORIENT to specify which channel USB−PD traffic will be transmitted or received.

BIST Mode

Bist Transmit

The FUSB307B will transmit Bist Carrier Mode 2 signaling when directed by the TCPM via TRANSMIT register. The FUSB307B will exit Bist Mode after tBISTContMode timer expires.

Bist Receive

When the FUSB307B is in Bist receive mode via TCPC_CTRL register, it will acknowledge these packets with a GoodCRC and automatically flush the buffer to allow for thousands of packets to be received without filling the receive buffer. Bist Receive mode will exit on a cable disconnect or a Hard Reset received.

VBUS Source and Sink Control

The FUSB307B can control a source and sink path via two outputs: SRC for the source path and SNK for the sink VBUS path.

These two outputs are controlled via the COMMAND register.

The SNK and SRC outputs will autonomously disable upon a cable detach.

Voltage Transitions

The FUSB307B device can control a vSafe5V path via its SRC output.

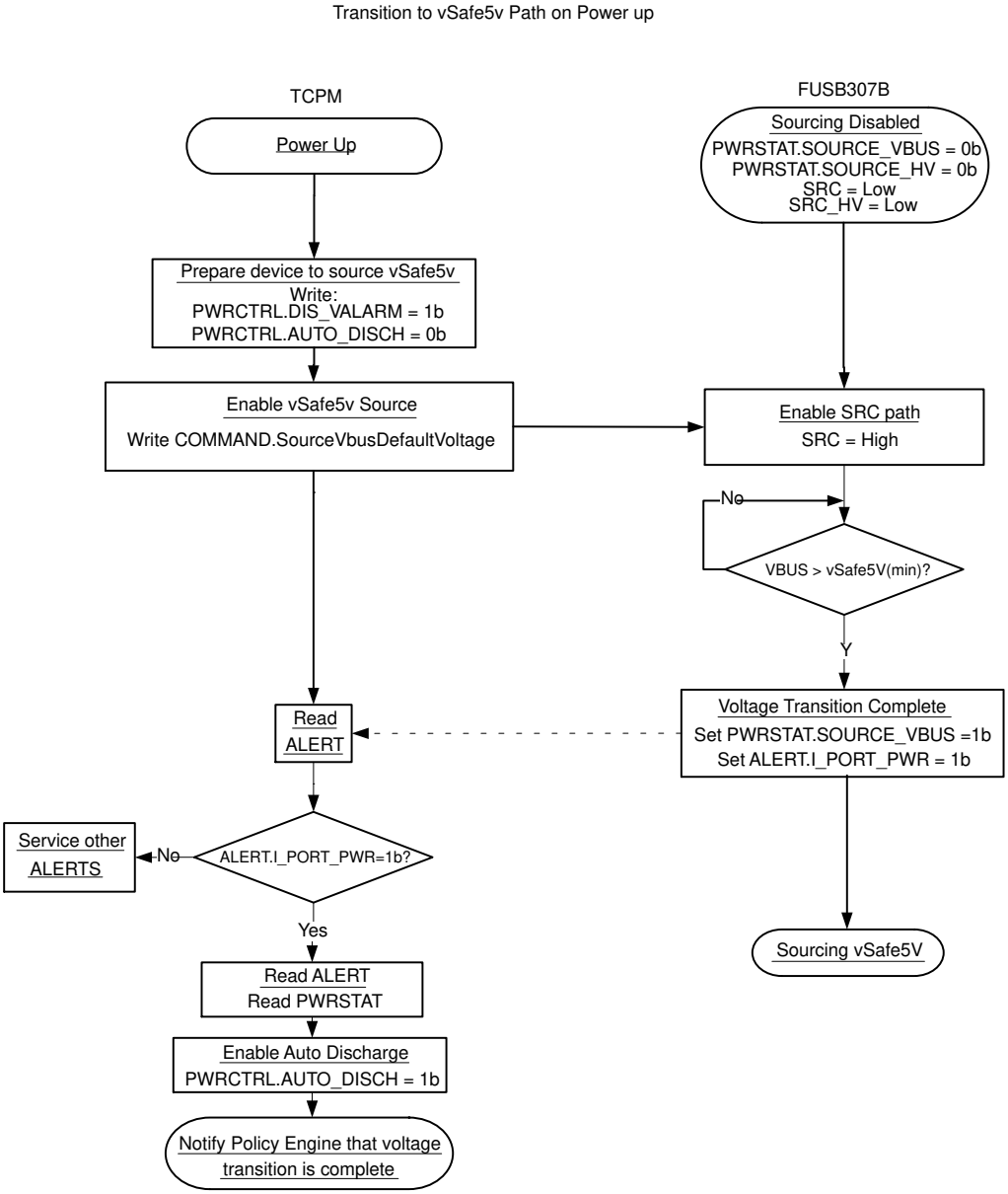
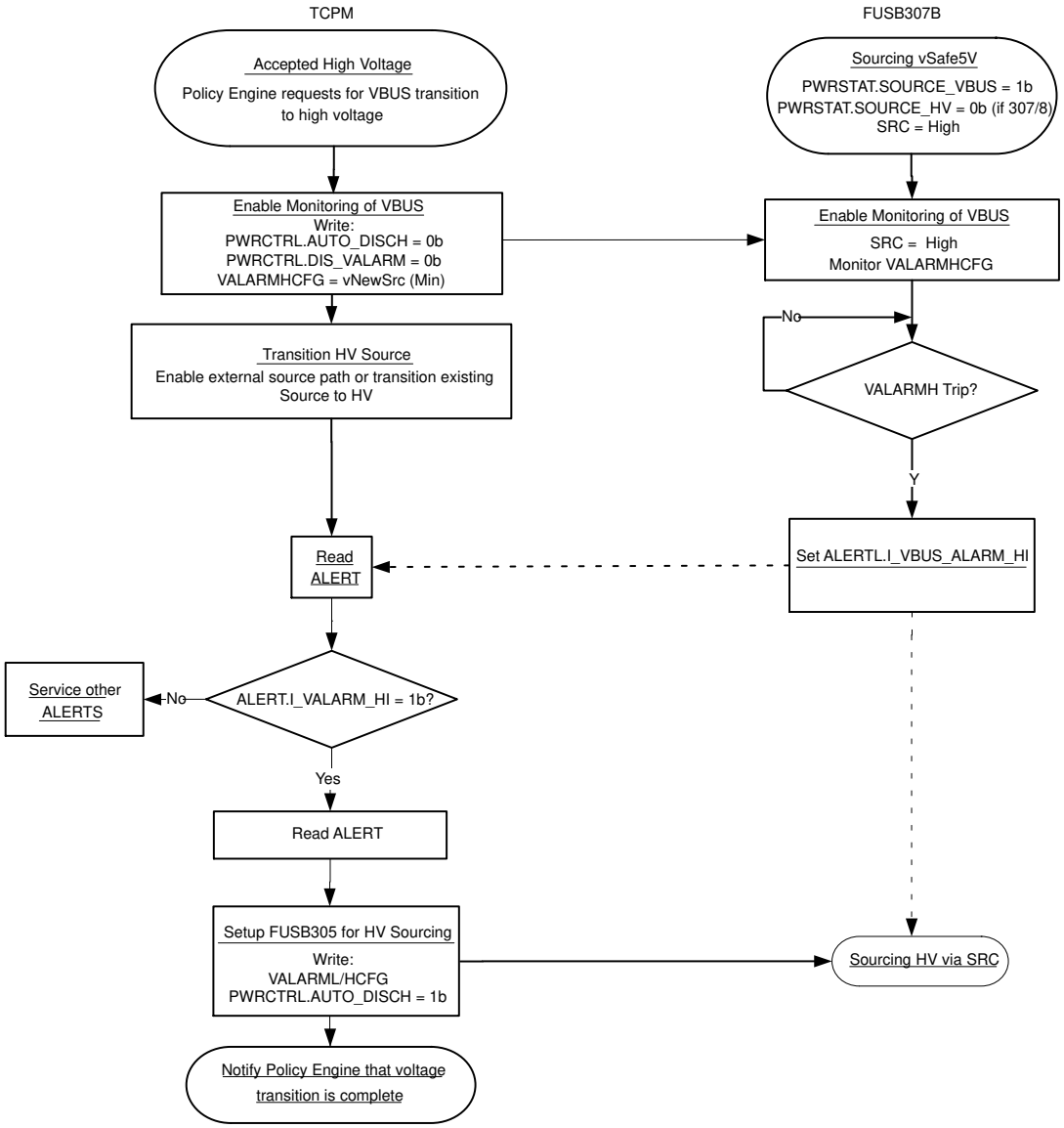


Figure 12. Transition to vSafe5V on Power Up

Transition to HV using SRC enabled Path



NOTE: Transitioning from HV on SRC to vSafe5v also on SRC can be done by using Voltage Alarm Low. Power supply is responsible for transitioning voltages to meet USB PD spec– no discharge necessary.

Figure 13. Transition to vSafe5V on Power Up

VBUS Monitoring and Measurement

The FUSB307B can monitor the presence of VBUS and will report it on PWRSTAT.VBUS_VAL and interrupt ALERT.I_PORT_PWR.

VBUS_VAL is set according to VBUS thresholds in *vVBUSthr*.

The FUSB307B also supports a more precise voltage measurement via an on−board ADC. The voltage on VBUS is measured at a rate of tVBUSsample and it is reported on VBUS_VOLTAGE_L/H register. The precision of the measurement is +/2% with a resolution of 25 mV LSB.

In addition to providing the µProcessor an accurate measurement of VBUS, the measurement in VBUS_VOLTAGE will be used when monitoring various user defined thresholds:

- Voltage alarms in registers VALARMLCFG and VALARMHCFGL
- VBUS Disconnect Threshold in registers VBUS_SNK_DISCL and VBUS_SNK_DISCH
- VBUS Stop Discharge Threshold in registers VBUS_STOP_DISCL and VBUS_STOP_DISCH
- The FUSB307B implements Low and High VBUS Voltage Alarms that can be programmable via VALARMLCFG and VALARMHCFG respectively. If the High or the Low thresholds are crossed, the FUSB307B will signal an interrupt on ALERTL.I_VBUS_ALRM_HI or ALERTH.I_VBUS_ALRM_LO respectively. These alarms can be disabled by writing PWRCTRL.DIS_VALARM to one

ALERTL.I_PORT_PWR is asserted if the bit−wise AND of PWRSTAT and PWRSTAMSK results in any bits that have the value 1.

VBUS Discharge

Manual Discharge

There are two types of manual discharge circuits implemented: A bleed discharge for low current and a force discharge. The bleed discharge can be manually enabled by writing a one to register bit PWRCTRL.EN_BLEED_DISCH. When enabled, the bleed discharge provides a low current load on VBUS of 7 kΩ (max.) via RBLEED. The force discharge is used to quickly discharge VBUS to vSafe0V by applying a dynamic load to VBUS via RFULL_DISCH. The force discharge can be manually enabled by writing a one to register bit PWRCTRL.FORCE_DISCH. When RFULL_DISCH is applied, the maximum slew rate allowed for discharging VBUS does not exceed vSrcSlewNeg 30 mV/µs as it is specified in the USB−PD spec.

Automatic discharge bit PWRCTRL. AUTO_DISCH must be disabled before enabling force discharge.

Automatic Source Discharge after a Disconnect

Automatic discharge can be enabled by setting PWRCTRL. AUTO_DISCH register bit. When in Source mode the FUSB307B will fully discharge VBUS to vSafe5V (max.) within tSafe5V and to vSafe0V within tSafe0V when a Disconnect occurs. The FUSB307B is in Source mode when the SRC output is asserted.

The FUSB307B in Source mode will detect a Disconnect if the CCSTAT.CCx_STAT field for the monitored CC pin indicates SRC.Open and enable the FULL Discharge pull−down device. The monitored CC pin is specified by TCPC_CTRL.ORIENT.

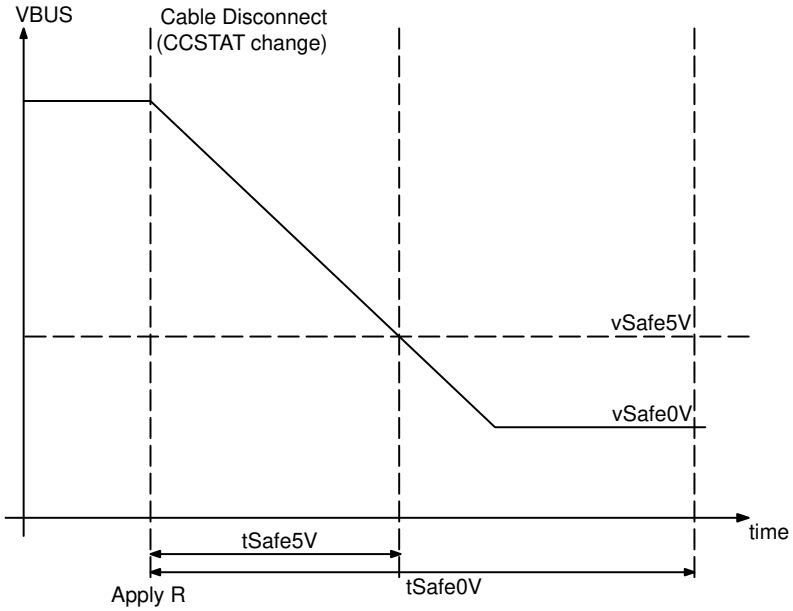


Figure 14. VBUS Auto Discharge as Source

Automatic Sink Discharge after a Disconnect

Automatic discharge can be enabled by setting PWRCTRL. AUTO_DISCH register bit. When in Sink mode the FUSB307B will fully discharge VBUS to vSafe5V (max.) within tSafe5V and to vSafe0V within tSafe0V when a disconnect occurs. The FUSB307B is in Sink mode any time MSGHEADR.POWER_ROLE = 0.

Whenever the system is sinking voltages greater than vSafe5V, a disconnect will be detected based on VBUS_SNK_DISC registers.

If the system is only sinking vSafe5V, a disconnect will be detected when VBUS_VAL goes low.

Due to the high capacitance on VBUS (up to 100 ¿F) the FUSB307B may not immediately know if VBUS has been removed. The FUSB307B with Automatic Discharge on will apply RBLEED discharge load to VBUS until it crosses below VBUS_SNK_DISC.

The FUSB307B has to detect a disconnect within tDisconnectDetect (6 ms) from VBUS crossing VBUS_SNK_DISCL. Once the FUSB307B has detected a Disconnect, RFULL_DISCH will be enabled bringing the VBUS voltage down to vSafe0V.

Whenever the FUSB307B detects a Disconnect, it will not present Rd (or Rp) until VBUS reaches vSafe0V.

When the VBUS voltage goes below vSafe0V, the auto−discharge circuit will disable.

If the discharge of VBUS to below vSafe0V is not accomplished by tSafe0V (650 ms), the FUSB307B will set the interrupt

NOTE: ALERTL.I_PORT_PWR is asserted if the bit−wise AND of PWRSTAT and PWRSTAMSK results in any bits that have the value 1.

ALERTH. I_FAULT bit and the status FAULTSTAT.DISCH_FAIL. The discharge circuit is not turned off when this happens.

In tSinkDischargeBleed + tSinkDischargeFull have to be less than tSafe5V to comply with USB−PD spec.

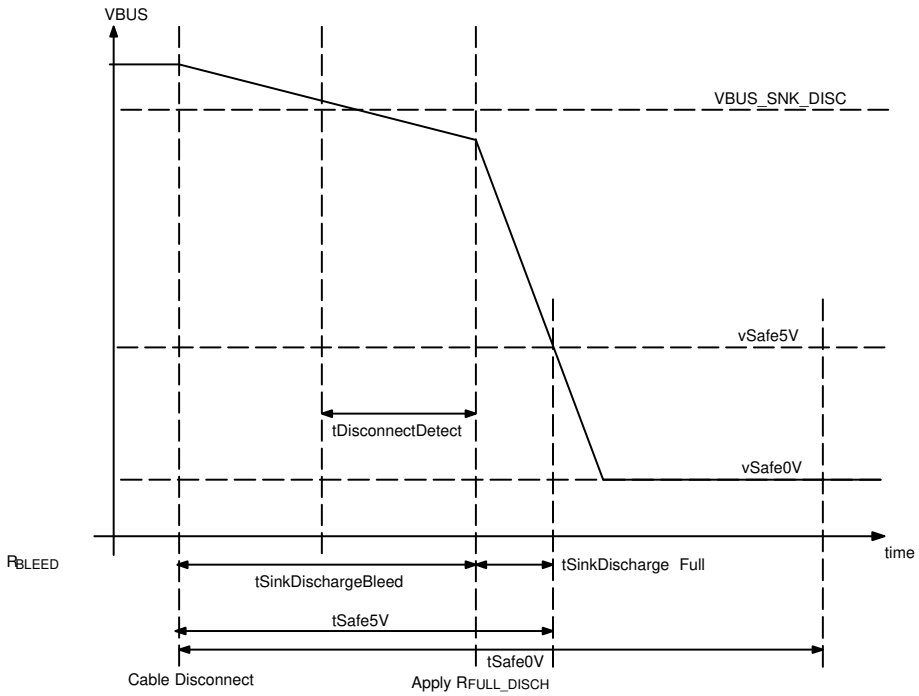


Figure 15. VBUS Auto Discharge as SinkSource

Discharge during a Connection

The discharge functions can be manually activated via the PWRCTRL.FORCE_DISCH register. The discharge pull−down is specified by *RFULL_DISCH*. The FUSB307B will automatically disable discharge when VBUS reaches VBUS_STOP_DISC threshold

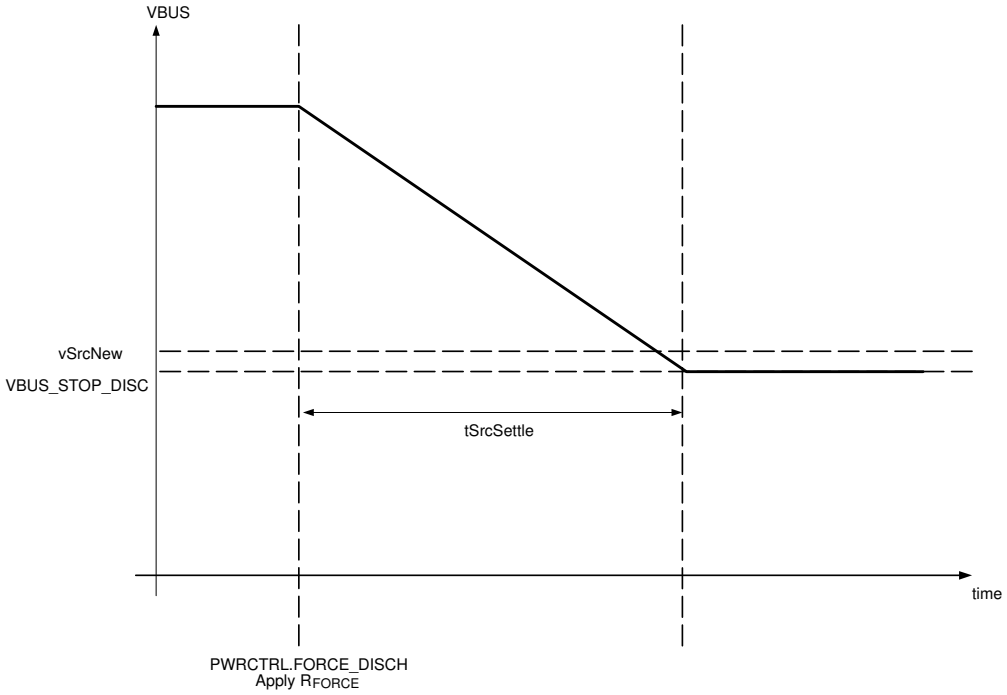


Figure 16. Sink Discharge during a Connection

Sink Discharge during a Connection

When the device is operating as a sink and it receives a Hard Reset or a Power Role Swap, the automatic discharge circuitry and SNK output will be disabled by the host processor to avoid a disconnect detection.

Watchdog Timer

The watchdog timer functionality is enabled whenever TCPC_CTRL.EN_WATCHDOG is set to 1b. The watchdog timer should only be enabled after an attach when the device is in Attached.Src, Attached.Snk or Apply.ROLECONTROL states. The watchdog timer starts when any of the interrupts that are not masked in the Alert register are set or when the INTB pin is asserted. The watchdog timer is cleared on an I2C access by the TCPM (either read or write). If the INTB pin is still asserted after this I2C access, the watchdog timer will reinitialize and start monitoring again until all of the Alerts are cleared or until the INTB pin is de−asserted.

When the watchdog timer expires, the FUSB307B will immediately disconnect the CC terminations by setting ROLE_CONTROL bits 3..0 to 1111b, disable all SRC/SRC_HV or SNK outputs, discharge VBUS to vSafe0V, and set FAULT_STATUS.I2CInterfaceError.

USB−PD Rev 3.0 Features

Extended Data Messages

Extended Data Messages is only supported via Chunking where large messages are broken into 2 or more 26 byte chunks.

SinkTx

The USB−PD Rev 3.0 has added this feature to allow the Sink to safely transmit a message reducing the risk of collisions.

The Protocol layer in the Source will request to set the Rp value to SinkTxOk to indicate that the Sink can initiate an Atomic Message Sequence (AMS). The Protocol layer in the Source will request to set the Rp value to SinkTxNG to indicate that the Sink cannot initiate an AMS since the Source is about to initiate an AMS.

The Sink TCPM that desires to transmit will write the TX Buffers and SINK_TRANSMIT register. The FUSB307B will wait for the Rp value to be set to SinkTxOk before transmitting the message. If Rp is already set to SinkTxOk, a SINK_TRANSMIT will transmit immediately.

In the case where the Sink TCPM wants to abort the message transmission before the Rp value has changed to SinkTxOk, it can write SINK_TRANSMIT.EN_SNK_TX = 0b. If a transmission has already started, writing this register will be ignored and a FAULTSTAT.I2C_ERR interrupt will be generated.

If TXBYTECNT is less than 2h when a SINK_TRANSMIT.TXSOP <101 is requested, a FAULTSTAT.I2CERR interrupt is generated.

The ALERTL.I_RXSTAT must be cleared when SINK_TRANSMIT is written or an ALERTL.I_TX_DISC is asserted.

Table 4. R_P SETTINGS FOR SINK T_X

Source Rp	Parameter	Description	Sink Operation	Source Operation
1.5 A @5 V	SinkTxNG	Sink Transmit “No Go”	Sink cannot initiate an AMS. Sink can only respond to Messages as part of an AMS	Source can initiate an AMS tSinkTx after setting Rp to this value (Note 5)
3.0 A @5 V	SinkTxOk	Sink Transmit “OK”	Sink can initiate an AMS	Source cannot initiate an AMS while this value is set

5. The TCPM is responsible for tSinkTx timer.

Fast Role Swap

Fast Role Swap is the process of exchanging the Source and Sink roles between Port Partners rapidly due to the disconnection of an external power supply.

The Fast Role Swap process is intended for use by a PDUSB HUB that presently has an external wall supply, and is providing power both through its downstream Ports to USB Devices and upstream to a USB Host such as a notebook. On removal of the external wall supply Fast Role Swap enables a VBUS supply to be maintained by allowing the USB Host to apply vSafe5V after having detected Fast Role Swap signaling.

The initial Source will signal a Fast Role Swap request by driving CC to ground with a resistance of less than *rFRSwapTx* for *tFRSwapTx*. The initial Source shall only signal a Fast Role Swap when it has an Explicit Contract. On transmission of the Fast Role Swap signal any pending Messages will be Discarded by internally toggling PD_RESET. The Fast Role Swap signal may override any active transmissions. Since the initial Sink’s response to the Fast Role Swap signal is to send a FR_Swap Message, the initial Source shall ensure Rp is set to *SinkTxOk* once the Fast Role Swap signal is complete.

The flow diagram in Figure 17 demonstrates the HUB and Host function during the initial Fast Role Swap process. The AMS and Power Role swap necessary to complete the Fast Role Swap is performed by the respective TCPMs.

Fast Role Swap Cable Disconnect (Informational Only)

The Initial Sink device waiting for FRSwap will not disconnect on VBUS since PWRCTRL.AUTO_DISCH will be set to zero by the TCPM. If the Type−C cable detaches while the Initial Sink is ready for a FRSwap, it will look like the Initial Source has initiated a FRSwap; The CC lines will be driven to GND by Rd.

The initial Sink will perform the FRSwap and the TCPM will initiate the FR_Swap message. Since there is no device attached, there will be no GoodCRC response which will transition to Type−C Error Recovery.

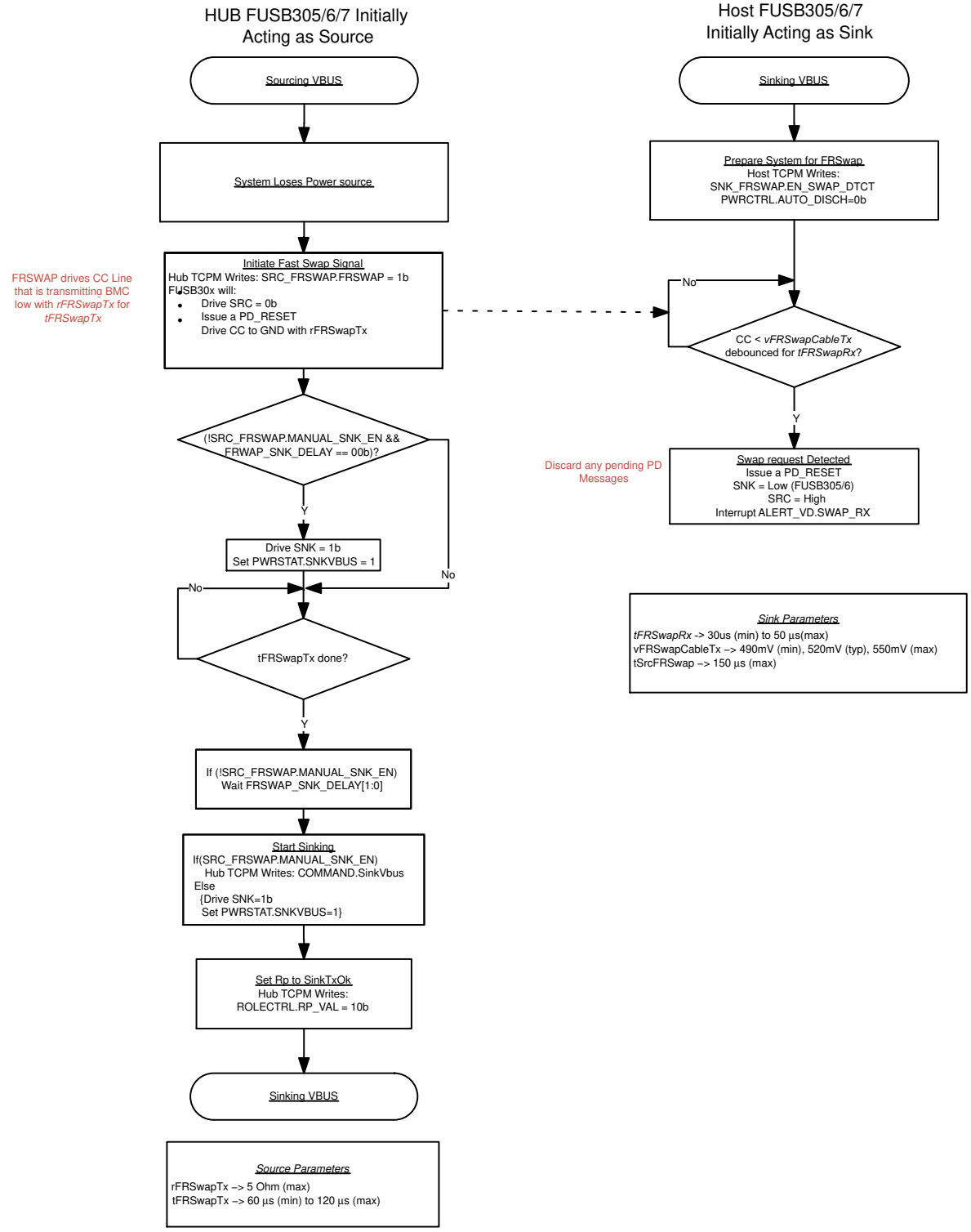


Figure 17. Fast Role Swap Flow Diagram

Table 5. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{DDAMR}	Supply Voltage from VDD		−0.5	6.0	V
V_{CC_HDDRP} (Note 6)	CC pins when configured as Host, Device or Dual Role Port		−0.5	6.0	V
V_{VBUS}	VBUS Supply Voltage		−0.5	28.0	V
$T_{STORAGE}$	Storage Temperature Range		−65	+150	C
T_J	Maximum Junction Temperature			+150	C
T_L	Lead Temperature (Soldering, 10 seconds)			+260	C
ESD	Human Body Model, JEDEC JESD22−A114	Connector Pins (VBUS, CCx)	4		kV
		Others	2		kV
	Charged Device Model, JEDEC LESD22−C101	All Pins	1		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. As host, device drives CC, VConn.

Table 6. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{BUS}	VBUS Supply Voltage (Note 7)	4.0	5.0	21.5	V
V_{DD}	VDD Supply Voltage	2.8 (Note 8)	3.3	5.5	V
V_{CONN}	VCONN Supply Voltage (Note 9)	2.7		5.5	V
I_{CONN}	VCONN Supply Current			560	mA
T_A	Operating Temperature	−40		+85	C
T_A	Operating Temperature (Note 10)	−40		+105	C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. 20 V PD + 5% Tolerance per spec + 0.5 V Load Transition.
8. This is for functional operation only and isn't the lowest limit for all subsequent electrical specifications below. All electrical parameters have a minimum of 3 V operation.
9. For powered accessories Vconn minimum is 2.7 V.
10. Automotive part only, FUSB307BVMPX.

DC and Transient Characteristics

Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified.

Table 7. CURRENT CONSUMPTION

Symbol	Parameter	T_A = –40 to +85°C T_A = –40 to +105°C (Note 17) T_J = –40 to +125°C			Unit
		Min	Typ	Max	
$I_{DISABLE}$	Disable Current (ROLECTRL = 0x0F)			10	μA
I_{STBY}	Unattached Sink		6	10	μA
	Unattached DRP or Source		7	20	μA
I_{ATTACH_TypeC}	Attached as Sink (No PD, AUTO_DISCH = 0)		11	26	μA
	Attached as Source (No PD)		12	22	μA

Table 8. BASEBAND PD

Symbol	Parameter	T_A = –40 to +85°C T_A = –40 to +105°C (Note 17) T_J = –40 to +125°C			Unit
		Min	Typ	Max	
UI	Unit Interval	3.03	3.33	3.70	μs
TRANSMITTER					
zDriver	TX output impedance at 750 kHz with an external 220 pF or equivalent load	33		75	Ω
tEndDriveBMC	Time to cease driving the line after the end of the last bit of the Frame			2	UI
tHoldLowBMC	Time to cease driving the line after the final high−to−low transition	1			μs
tStartDrive	Time before the start of the first bit of the preamble when the transmitter shall start driving the line	−1		1	μs
tBISTContMode	Time a BIST Carrier Mode 2 transmission is performed	30		60	ms
tBUFFER2CC	Time from I2C Stop from writing to TRANSMIT register to first bit of Preamble transmitted			195	μs
t_R	Rise Time	300			ns
t_F	Fall Time	300			ns
RECEIVER					
cReceiver	Receiver capacitance when driver isn't turned on (Note 11)		25		pF
zBmcRx	Receiver Input Impedance	1			MΩ
tCC2BUFFER	Time between last bit of EOP to I_RXSTAT			50	μs
tRxFilter	Rx bandwidth limiting filter (Note 11)	100			ns
nTransitionCount	Transitions count in a time window of 20 μs max	3			Edges
tTransitionWindow	Time window for detecting non−idle	12		20	μs

11. Guaranteed by characterization and/or design. Not production tested.

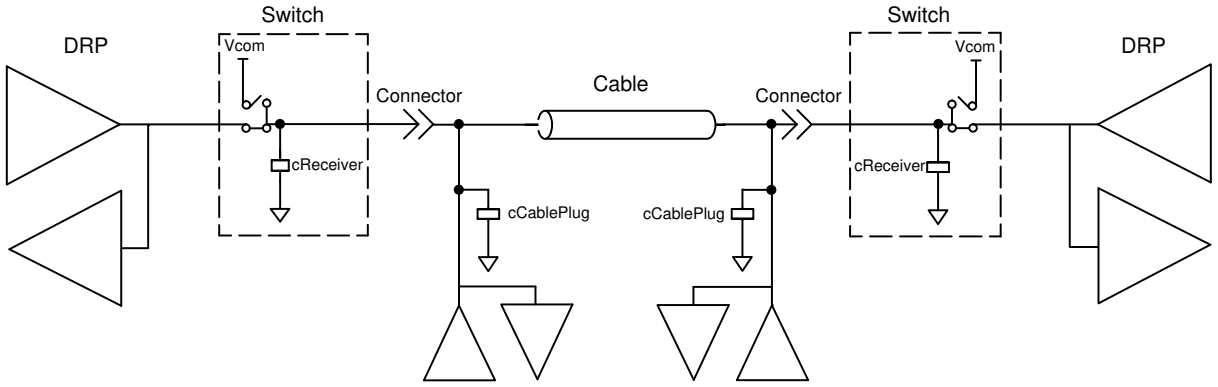


Figure 18. Transmitter Test Load

Table 9. USB-PD R3.0 SPECIFIC PARAMETERS

Symbol	Parameter	T_A = –40 to +85°C T_A = –40 to +105°C (Note 17) T_J = –40 to +125°C Min	Typ	Max	Unit
TRANSMITTER					
rFRSwapTx	Fast Role Swap request transmit driver resistance Measured from V_{CCx} = 0 to vFRSwapCableTx			5	Ω
tFRSwapTx	Fast Role Swap request transmit duration	60		120	μs
RECEIVER					
tFRSwapRx	Fast Role Swap request detection time	30		50	μs
vFRSwapCableTx	Fast Role Swap request voltage detection threshold	490	520	550	mV

Table 10. TYPE C SPECIFIC PARAMETERS

Symbol	Parameter	T_A = –40 to +85°C T_A = –40 to +105°C (Note 17) T_J = –40 to +125°C Min	Typ	Max	Unit
R_{SW_CCx}	R_{DSON} for VCONN to CC1 or VCONN to CC2		0.4	1.0	Ω
I_{SW_CCX}	Over Current Protection (OCP) limit at which VCONN switch shuts off over the entire VCONN voltage range VCONN_OCP = 0Fh	600	800	1000	mA
$t_{SoftStart}$	Time taken for the VCONN switch to turn on during which Over–Current Protection is disabled		1.5		ms
I_{80_CCX}	DFP 80 μA CC Current (Default) ROLECTRL = 05h	64	80	96	μA
I_{180_CCX}	DFP 180 μA CC Current (1.5 A) ROLECTRL = 15h	166	180	194	μA
I_{330_CCX}	DFP 330 μA CC Current (3 A) ROLECTRL = 25h	304	330	356	μA
V_{UFPDB}	UFP pull–down voltage in dead battery under all pull–up DFP loads			2.18	V
R_{DEVICE}	Device pull–down resistance (Note 12)	4.6	5.1	5.6	kΩ
Ra	Powered Accessory Termination	800		1200	Ω
vRa–SRCdef	Ra Detection Threshold for CC Pin for Source for Default Current on VBUS	0.15	0.20	0.25	V
vRa–SRC1.5A	Ra Detection Threshold for CC Pin for Source for 1.5 A Current on VBUS	0.35	0.40	0.45	V

Table 10. TYPE C SPECIFIC PARAMETERS (continued)

Symbol	Parameter		T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J = −40 to +125°C Min	Typ	Max	Unit
vRa−SRC3A	Ra Detection Threshold for CC Pin for Source for 3 A Current on VBUS		0.75	0.80	0.85	V
vRd−SRCdef	Rd Detection Threshold for Source for Default Current (HOST_CUR1/0 = 01)		1.50	1.60	1.65	V
vRd−SRC1.5A	Rd Detection Threshold for Source for 1.5 A Current (HOST_CUR1/0 = 10)		1.50	1.60	1.65	V
vRd−SRC3A	Rd Detection Threshold for Source for 3 A Current (HOST_CUR1/0 = 11)		2.45	2.60	2.75	V
vRa−SNK	Ra Detection Threshold for CC Pin for Sink		0.15	0.20	0.25	V
vRd−def	Rd Default Current Detection Threshold for Sink		0.61	0.66	0.70	V
vRd−1.5A	Rd 1.5 A Current Detection Threshold for Sink		1.16	1.23	1.31	V
vRd−3.0A	Rd 3 A Current Detection Threshold for Sink		2.04	2.11	2.18	V
zOPEN	CC resistance for disabled state, ROLECTRL = 0Fh		126			kΩ
vVCONNthr	Valid VCONN Voltage Assumes PWRCTRL.EN_VCONN = 1b				2.4	V
tTCPCfilter	Debounce time on CC lines to prevent CCSTAT change in case of minor changes in voltage on CC because of noise		4		500	μs
tCCDebounce	Debounce Time for CC Attach Detection		100	150	200	ms
tPDDebounce (Note 13)	Time a port shall wait before it can determine there has been a change in USB Type−C current due to the potential for USB−PD BMC signaling on CC		10	15	20	ms
tSetReg	Time between CC status change and I2C registers updated				50	μs
tTCPCSampleRate	CC Sample rate for indicating changes on CC lines				1	ms
tDRP	Sum of tToggleSrc and tToggleSnk timers		50		100	ms
tToggleSrc	Time Spent in Apply Rp before transitioning to Apply Rd	DRPTOGGLE = 00	15		30	ms
		DRPTOGGLE = 01	20		40	ms
		DRPTOGGLE = 10	25		50	ms
		DRPTOGGLE = 11	30		60	ms
tToggleSnk	Time Spent in Apply Rd before transitioning to Apply Rp	DRPTOGGLE = 00	35		70	ms
		DRPTOGGLE = 01	30		60	ms
		DRPTOGGLE = 10	25		50	ms
		DRPTOGGLE = 11	20		40	ms

12. RDEVICE minimum and maximum specifications are only guaranteed when power is applied.
13. Only Applicable to Autonomous Debug State machine.

Table 11. VBUS MEASUREMENT CHARACTERISTICS

Symbol	Parameter		T_A = –40 to +85°C T_A = –40 to +105°C (Note 17) T_J = –40 to +125°C			Unit
			Min	Typ	Max	
vMDACstepVBUS	VBUS Measure block LSB reported on VBUS_VOLTAGE[9:0] register			25		mV
pMDACVBUS	Accuracy of VBUS Voltage Measurement	T_A = –40 to +85°C			±2	%
		T_A = +85 to +105°C (Note 12)			±5	%
tVBUSsample	Sampling period of VBUS Measurement			3		ms
vVBUSthr	VBUS threshold at which VBUS_VAL interrupt is triggered. Assumes VBUS present detection is enabled	VDD > V_{DDGOOD}	3.5		4.0 (Note 14)	V
		VDD < V_{DDGOOD} (Dead Battery)	3.4		4.0	
vVBUShys	Hysteresis on VBUS Comparator			50		mV
vSafe0Vthr	Safe Operating Voltage at “Zero Volts” Threshold				0.8	V
vSafe0Vhys	vSafe0V Hysteresis			40		mV
vALARMLSB	LSB of VBUS thresholds for VBUS_SNK_DISCL VBUS_STOP_DISCL VALARMHCFGL VALARMLCFGL			50		mV
pALARM	Accuracy of VBUS thresholds for VBUS_SNK_DISCL VBUS_STOP_DISCL VALARMHCFGL VALARMLCFGL				±5	%

14. FUSB307BVMPX vVBUSthr (max) = 4.05 V.

Table 12. SOURCE AND SINK CONTROL SPECIFICATIONS

Symbol	Parameter		T_A = –40 to +85°C T_A = –40 to +105°C (Note 17) T_J = –40 to +125°C			
			Min	Typ	Max	Unit
R_{BLEED}	Equivalent Resistance for bleed discharging VBUS	VBUS = 4.0 V to 21.5 V	4		7	kΩ
vSrcSlewNeg	Maximum slew rate allowed when discharging VBUS	VBUS = 4.0 V to 21.5 V			30	mV/μs
tSafe0V	Time to reach vSafe0V max				650	ms
tSafe5V	Time to reach vSafe5V max				275	ms
tSrcSettle	Time to discharge to vSrcNew				275	ms
tAUTO_DISCH_FAIL	Time to declare auto discharge failure to discharge to vSafe0V	Device configured as Source. Measure from CCSTAT change to Open	650			ms
		Device configured as Sink. Measure from I_VBUS_SNK_DISC	440			ms
tAUTO_DISCH_FAIL_5V	Time to declare auto discharge failure to discharge to vSafe5v	Device configured as Source. Measure from CCSTAT change to Open	275			ms
		Device configured as Sink. Measure from I_VBUS_SNK_DISC	60			ms

Table 13. LDO SPECIFICATIONS

Symbol	Parameter	V_{DD}	Conditions	T_A = –40 to +85°C T_A = –40 to +105°C (Note 17) T_J = –40 to +125°C			Unit
				Min	Typ	Max	Unit
V_{V3P3}	LDO Output Voltage	< V_{DDGOOD}	VBUS = 4.0 V to 21.5 V	3.0		3.6	V
V_{LDO_VALID}	Valid VBUS_IN range for LDO operation	< V_{DDGOOD}		4.0		21.5	V
V_{DDGOOD}	VDD Voltage where device is powered from VDD instead of VBUS			2.7		3.0	V
I_{LDO_MAX}	Max. Output Current	< V_{DDGOOD}	VBUS = 4.0 V to 21.5 V, V_{DROP} = 120 mV	30			mA

Table 14. OVER-TEMPERATURE SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
T_{SHUT}	Temp. for VCONN Switch Turn Off		145		°C
T_{HYS}	Temp. Hysteresis for VCONN Switch Turn On		10		°C

Table 15. WATCHDOG TIMER SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
$T_{HVWatchdog}$	Time from last I2C transaction or INTB pin assertion to entering ErrorRecovery	1500		2000	ms