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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Ordering number : ENA2066A

FW389

Power MOSFET

100V, 2A, 225mΩ, −100V, −2A, 300mΩ, Complementary Dual SOIC8

ON Semiconductor®

http://onsemi.com

Features

- ON-resistance Nch : $R_{DS}(on)1$=165mΩ(typ.)
  Pch : $R_{DS}(on)1$=230mΩ(typ.)
- Input Capacitance Nch : Ciss=490pF(typ.)
  Pch : Ciss=1000pF(typ.)
- 4V drive
- Halogen free compliance
- Protection diode in

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	N-channel	P-channel	Unit
Drain-to-Source Voltage	V_{DSS}		100	−100	V
Gate-to-Source Voltage	V_{GSS}		±20	±20	V
Drain Current (DC)	I_D		2	−2	A
Drain Current (PW≤100ms)	I_{DP}	Duty cycle≤1%	5	−5	A
Drain Current (PW≤10μs)	I_{DP}	Duty cycle≤1%	8	−8	A
Allowable Power Dissipation	P_D	When mounted on ceramic substrate (2000mm²×0.8mm) 1unit, (PW≤10s)	1.8		W
Total Dissipation	P_T	When mounted on ceramic substrate (2000mm²×0.8mm), (PW≤10s)	2.2		W
Channel Temperature	Tch		150		°C
Storage Temperature	Tstg		−55 to +150		°C
Avalanche Energy (Single Pulse) *1	E_{AS}		5.3	5.3	mJ
Avalanche Current *2	I_{AV}		2	−2	A

*1 N-Channel:V_{DD}=10V, L=2mH, I_{AV}=2A(Fig.1)
P-Channel:V_{DD}=−10V, L=2mH, I_{AV}=−2A(Fig.1)

*2 L≤2mH, single pulse

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

lectrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[N-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0V	100			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V			1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	$V_{GS}(off)$	V_{DS}=10V, I_D=1mA	1.5		2.6	V
Forward Transfer Admittance	| yfs |	V_{DS}=10V, I_D=2A		2.9		S
Static Drain-to-Source On-State Resistance	$R_{DS}(on)1$	I_D=2A, V_{GS}=10V		165	225	mΩ
	$R_{DS}(on)2$	I_D=1A, V_{GS}=4.5V		180	254	mΩ
	$R_{DS}(on)3$	I_D=1A, V_{GS}=4V		190	275	mΩ
Input Capacitance	Ciss	V_{DS}=10V, f=1MHz		490		pF
Output Capacitance	Coss			34		pF
Reverse Transfer Capacitance	Crss			13		pF
Turn-ON Delay Time	$t_d(on)$	See specified Test Circuit.		9.3		ns
Rise Time	t_r			5.4		ns
Turn-OFF Delay Time	$t_d(off)$			42		ns
Fall Time	t_f			26		ns

Continued on next page.

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

Semiconductor Components Industries, LLC, 2014
February, 2014

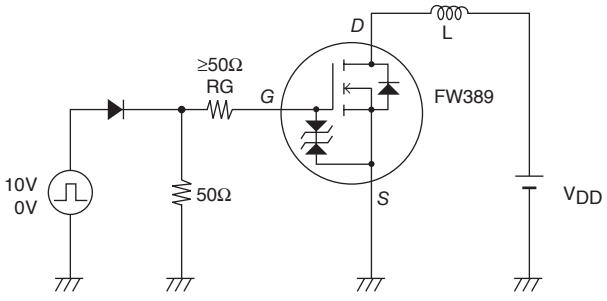
Continued from preceding page

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
N-channel]						
Total Gate Charge	Qg	V_{DS}=50V, V_{GS}=10V, I_D=2A		10		nC
Gate-to-Source Charge	Qgs			1.4		nC
Gate-to-Drain “Miller” Charge	Qgd			2.1		nC
Diode Forward Voltage	V_{SD}	I_S=2A, V_{GS}=0V		0.78	1.2	V
Gata Resistance	Rg	V_{DS}=0V, V_{GS}=0V, f=1MHz	0		12	Ω
[P-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0V	−100			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−100V, V_{GS}=0V			−1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−10V, I_D=−1mA	−1.2		−2.6	V
Forward Transfer Admittance	| yfs |	V_{DS}=−10V, I_D=−2A		4.7		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=−2A, V_{GS}=−10V		230	300	mΩ
	R_{DS}(on)2	I_D=−1A, V_{GS}=−4.5V		240	336	mΩ
	R_{DS}(on)3	I_D=−1A, V_{GS}=−4V		250	355	mΩ
Input Capacitance	Ciss	V_{DS}=−20V, f=1MHz		1000		pF
Output Capacitance	Coss			77		pF
Reverse Transfer Capacitance	Crss			47		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		12		ns
Rise Time	t_r			16		ns
Turn-OFF Delay Time	t_d(off)			110		ns
Fall Time	t_f			40		ns
Total Gate Charge	Qg	V_{DS}=−50V, V_{GS}=−10V, I_D=−2A		21		nC
Gate-to-Source Charge	Qgs			2.8		nC
Gate-to-Drain “Miller” Charge	Qgd			4.4		nC
Diode Forward Voltage	V_{SD}	I_S=−2A, V_{GS}=0V		−0.79	−1.2	V
Gata Resistance	Rg	V_{DS}=0V, V_{GS}=0V, f=1MHz	0		50	Ω

Fig.1 Unclamped Inductive Switching Test Circuit

[N-channel]



[P-channel]

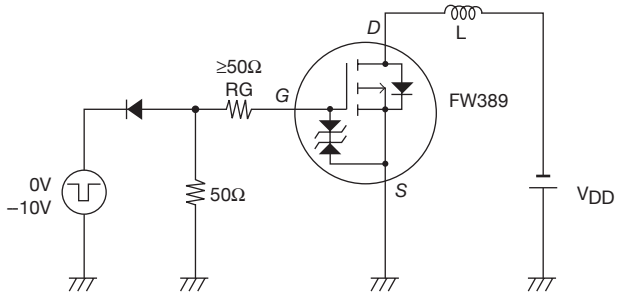
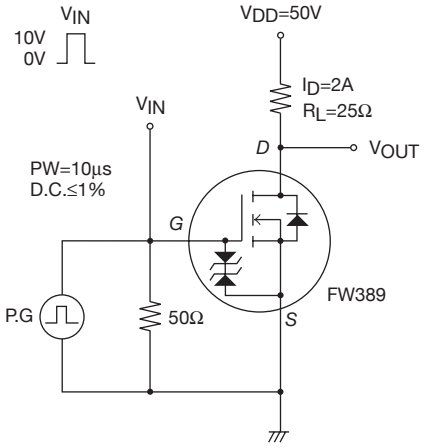
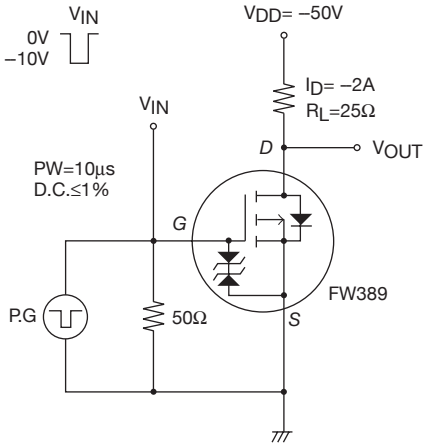


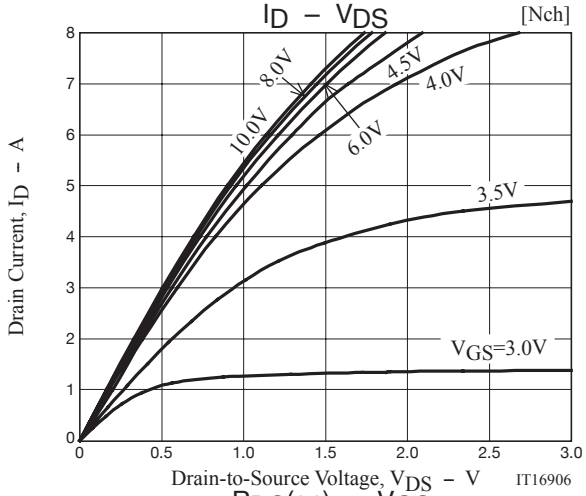
Fig.2 Switching Time Test Circuit

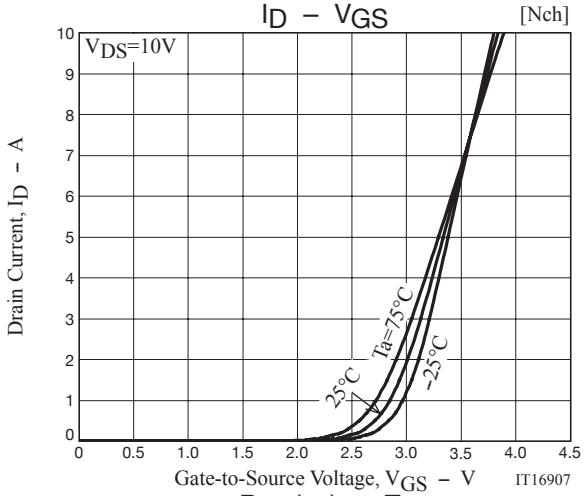
[N-channel]

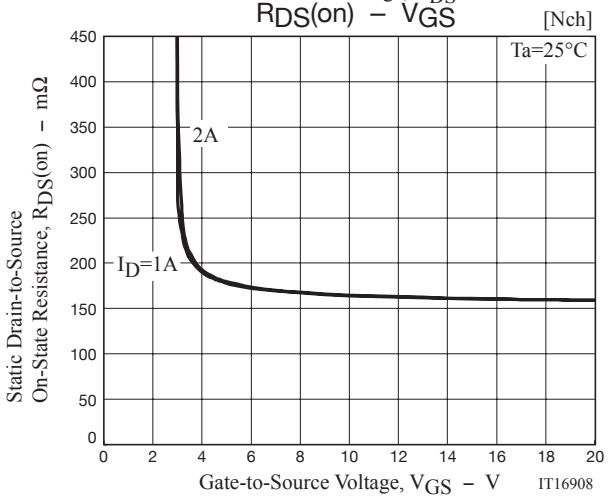


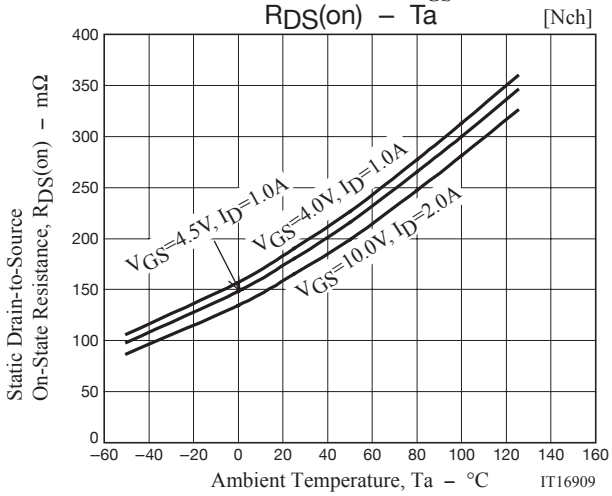
[P-channel]

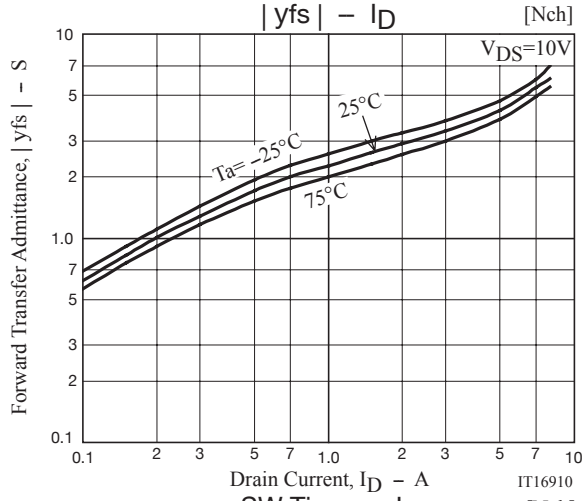


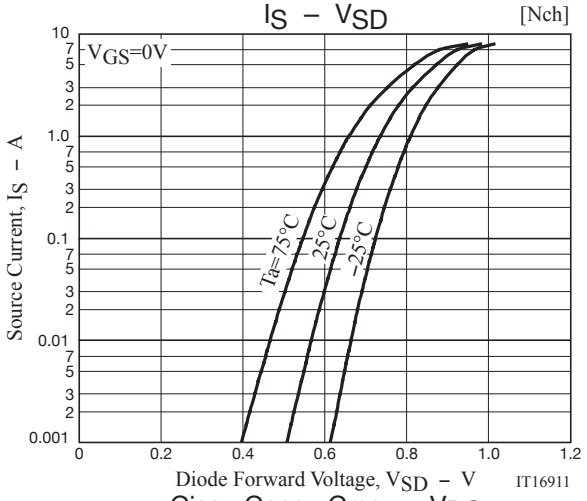


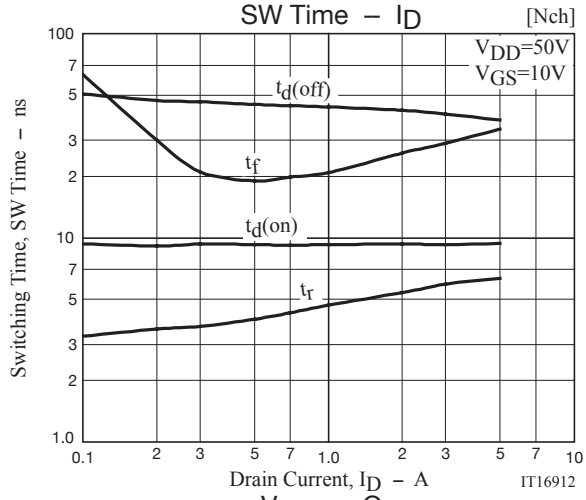


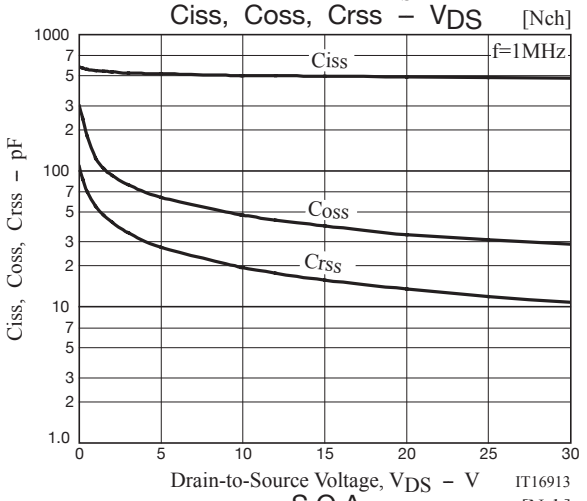


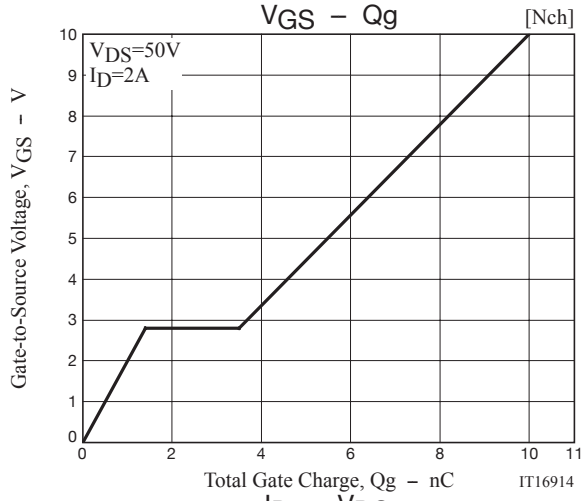


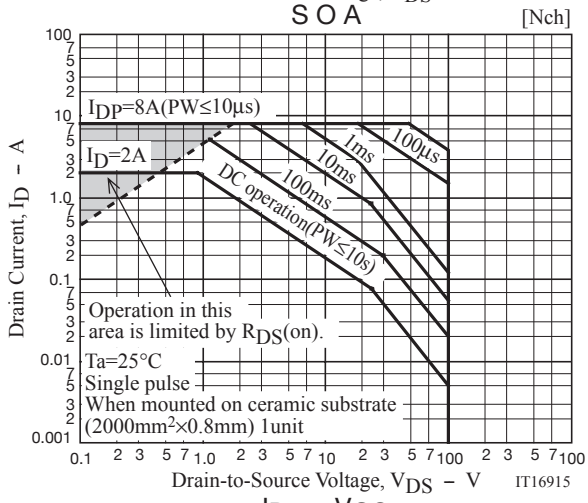

| yfs | – ID
[Nch]
VDS=10V
25°C
Ta= –25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT16910

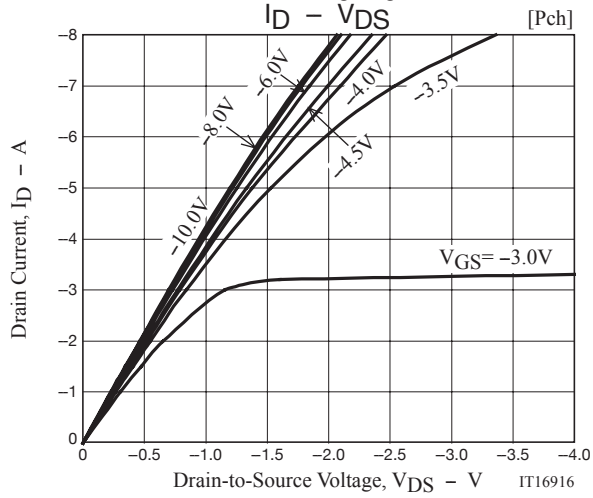

IS – VSD
[Nch]
VGS=0V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT16911

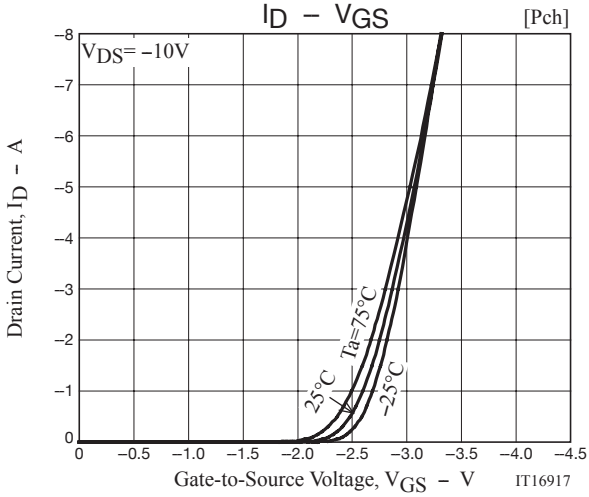

SW Time – ID
[Nch]
VDD=50V
VGS=10V
td(off)
tf
td(on)
tr
Switching Time, SW Time – ns
Drain Current, ID – A
IT16912

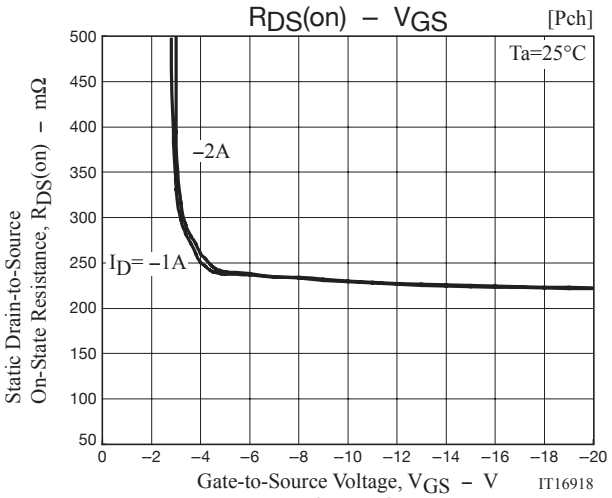

Ciss, Coss, Crss – VDS
[Nch]
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT16913

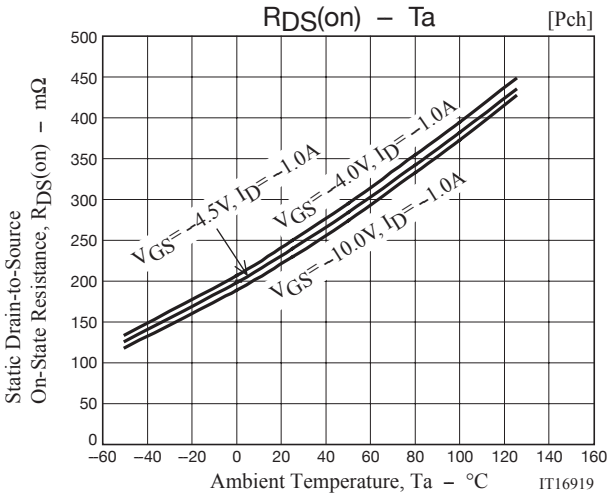

VGS – Qg
[Nch]
VDS=50V
ID=2A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT16914

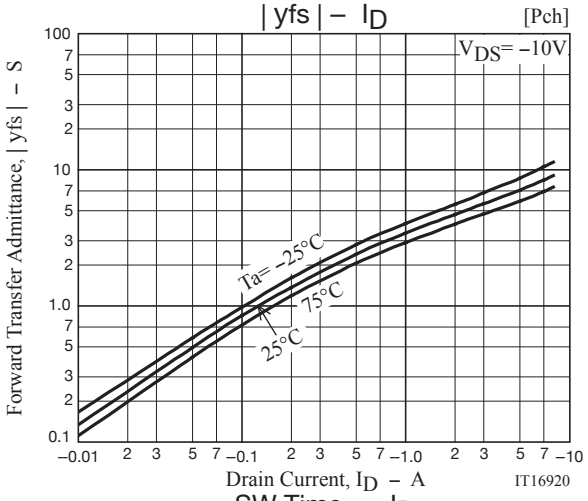

S O A
[Nch]
IDP=8A(PW≤10μs)
ID=2A
1ms
10ms
100ms
100μs
DC operation(PW≤10s)
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate
(2000mm2×0.8mm) 1unit
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT16915

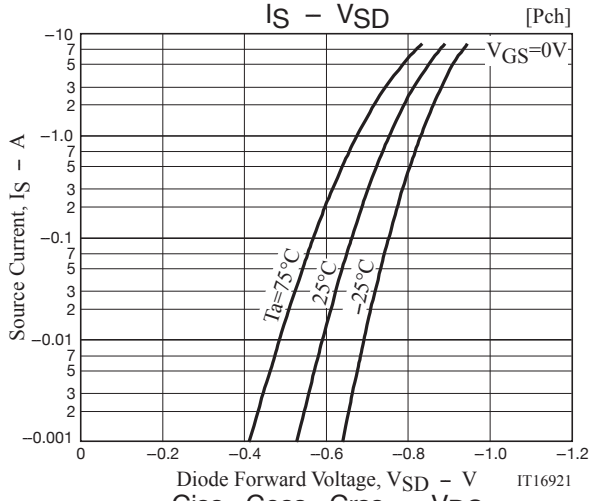

ID – VDS
[Pch]
–6.0V
–8.0V
–4.0V
–3.5V
–4.5V
–10.0V
VGS= –3.0V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT16916

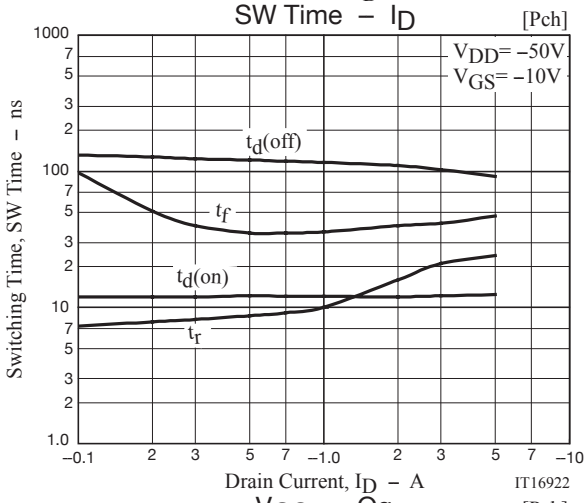

ID – VGS
[Pch]
VDS= –10V
Ta=75°C
25°C
–25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT16917

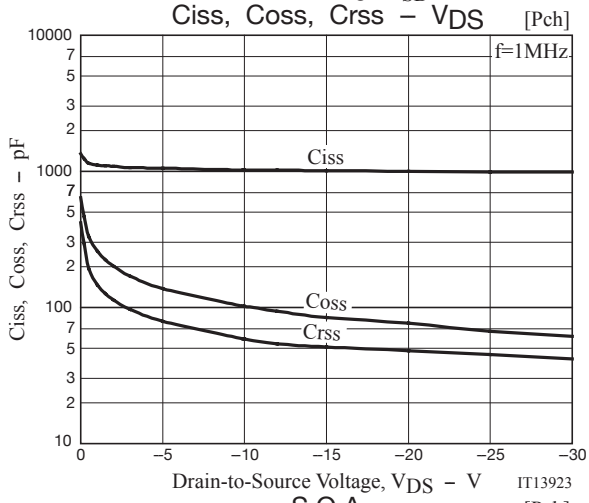

RDS(on) – VGS
[Pch]
Ta=25°C
–2A
ID= –1A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT16918

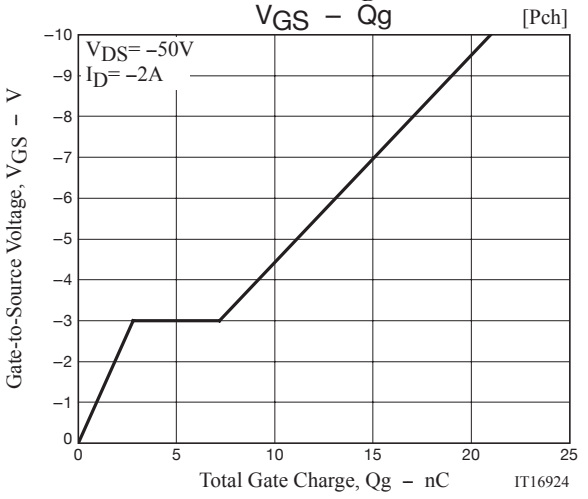

RDS(on) – Ta
[Pch]
VGS= –4.5V, ID= –1.0A
VGS= –4.0V, ID= –1.0A
VGS= –10.0V, ID= –1.0A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT16919

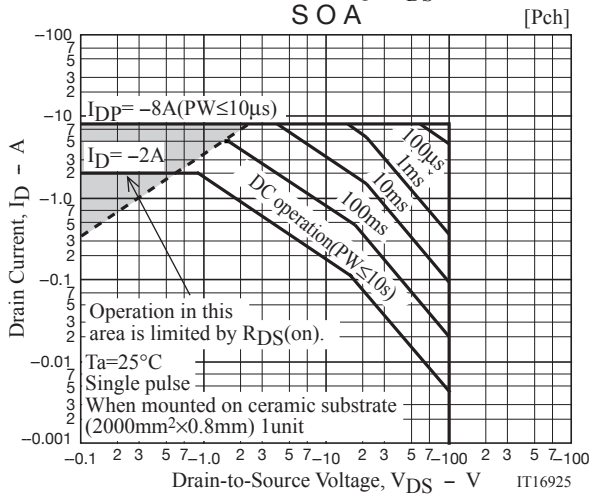

| yfs | – ID
[Pch]
VDS= –10V
Ta= –25°C
25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT16920

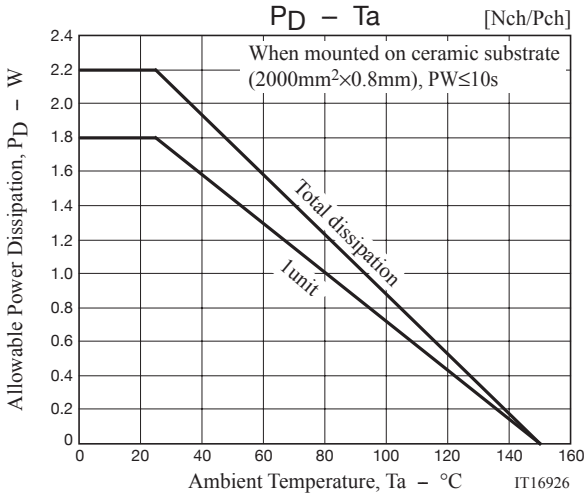

IS – VSD
[Pch]
VGS=0V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT16921

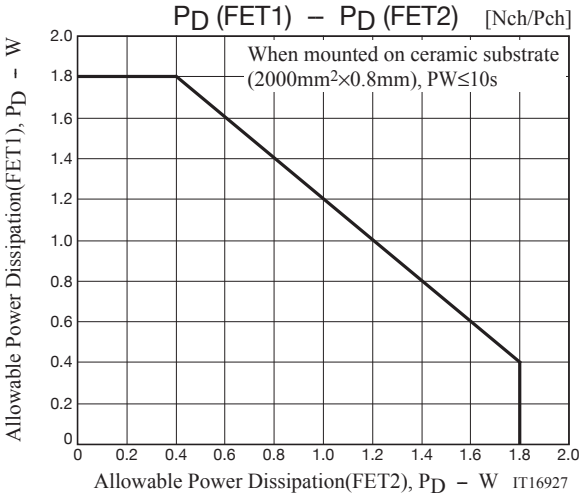

SW Time – ID
[Pch]
VDD= –50V
VGS= –10V
td(off)
tf
td(on)
tr
Switching Time, SW Time – ns
Drain Current, ID – A
IT16922

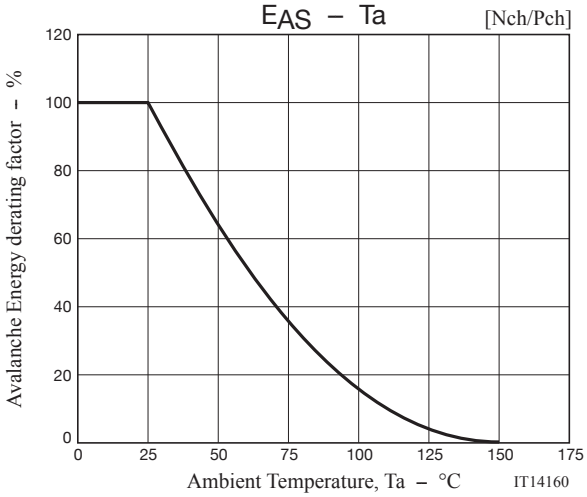

Ciss, Coss, Crss – VDS
[Pch]
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT13923


VGS – Qg
[Pch]
VDS= –50V
ID= –2A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT16924


S O A
[Pch]
IDP= –8A(PW≤10μs)
ID= –2A
100μs
1ms
10ms
100ms
DC operation(PW≤10s)
Operation in this area is limited by RDS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate (2000mm²×0.8mm) 1unit
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT16925


PD – Ta
[Nch/Pch]
When mounted on ceramic substrate
(2000mm2×0.8mm), PW≤10s
Total dissipation
1unit
Allowable Power Dissipation, PD – W
Ambient Temperature, Ta – °C
IT16926


PD (FET1) – PD (FET2)
[Nch/Pch]
When mounted on ceramic substrate
(2000mm2×0.8mm), PW≤10s
Allowable Power Dissipation(FET1), PD – W
Allowable Power Dissipation(FET2), PD – W
IT16927

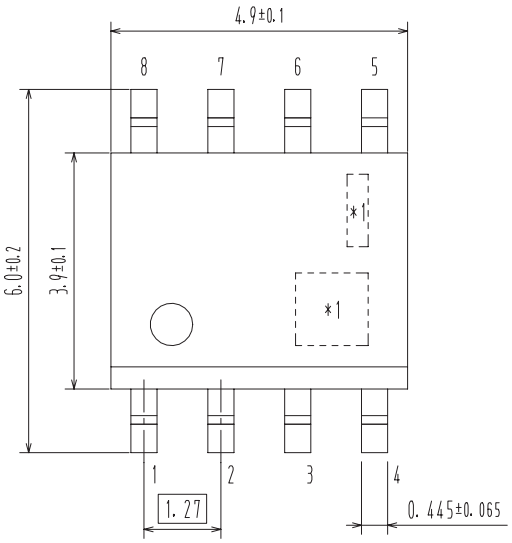

EAS – Ta
[Nch/Pch]
Avalanche Energy derating factor – %
Ambient Temperature, Ta – °C
IT14160

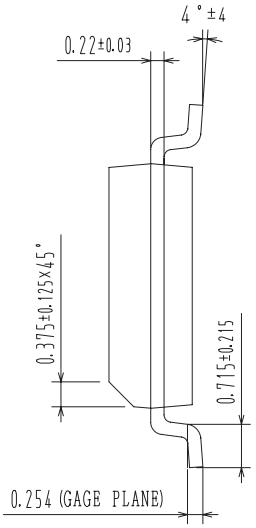
Package Dimensions

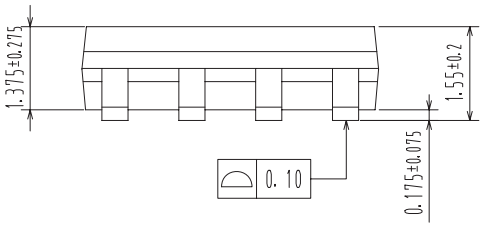
FW389-TL-2W

SOIC-8
CASE 751CR
ISSUE O
unit : mm

1:Source1
2:Gate1
3:Source2
4:Gate2
5:Drain
6:Drain
7:Drain
8:Drain



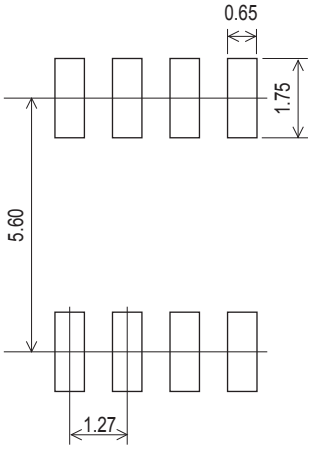




*1:Lot Indication.

*2:Lot Indication. Some products have no Lot indication.

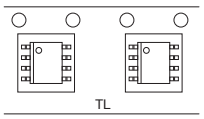
Land Pattern Example



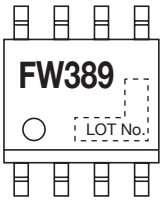
Ordering & Package Information

Device	Package	Shipping	note
FW389-TL-2W	SOIC8, SC-87, SOT-96	2,500 pcs. / reel	Pb-Free and Halogen Free

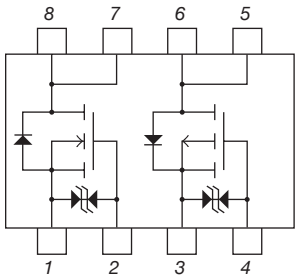
Packing Type:TL



Marking



Electrical Connection



Note on usage : Since the FW389 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.