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3-Axis Digital Angular Rate Gyroscope

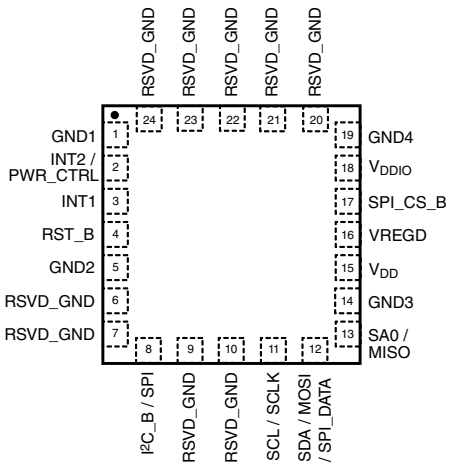
FXAS21002C

24 QFN
4 mm x 4 mm x 1 mm
Case 2209-01

FXAS21002C is a small, low-power, yaw, pitch, and roll angular rate gyroscope with 16 bit ADC resolution. The full-scale range is adjustable from ±250°/s to ±2000°/s. It features both I^2C and SPI interfaces.

FXAS21002C is capable of measuring angular rates up to ±2000°/s, with output data rates (ODR) from 12.5 to 800 Hz. An integrated Low-Pass Filter (LPF) allows the host application to limit the digital signal bandwidth. The device may be configured to generate an interrupt when a user-programmable angular rate threshold is crossed on any one of the enabled axes.

FXAS21002C is available in a plastic, 24-lead QFN package; the device is guaranteed to operate over the extended temperature range of –40 °C to +85 °C.



Pin Connections

Features

- Supply voltage (V_{DD}) from 1.95 V to 3.6 V
- Interface Supply voltage (V_{DDIO}) from 1.62 V to V_{DD} + 0.3 V
- 16-bit digital output resolution
- ±250/500/1000/2000°/s configurable full-scale dynamic ranges
- Full-Scale Range boost function enables FSR's up to ±4000 dps
- Angular rate sensitivity of 0.0625°/s in ±2000°/s FSR mode
- Noise spectral density of 25 mdps/√Hz at 64 Hz bandwidth (200 Hz ODR)
- Current consumption in Active mode is 2.7 mA
- Fast transition from Standby to Active mode (60 ms)
- Supported digital interfaces include:
  - I^2C Standard and Fast Mode (100/400 kHz)
  - SPI Interface (3- and 4-wire modes, up to 2 MHz)
- FIFO buffer is 192 bytes (32 X/Y/Z samples) with stop and circular operating modes
- Output Data Rates (ODR) from 12.5 to 800 Hz; programmable low-pass filter to further limit digital output data bandwidth
- Low power standby mode
- Power mode transition control via external pin for accelerometer-based power management (motion interrupt)
- Rate Threshold interrupt function
- Integrated self-test function
- 8-bit temperature sensor

Typical Applications

- Industrial and consumer grade robots, UAVs, and RC vehicles
- Game controller
- Gyro-stabilized electronic compass
- Orientation determination
- Gesture-based user interfaces and Human Machine Interface (HMI)
- Indoor navigation
- Mobile phones and tablets
- Virtual and augmented reality devices (including glasses)

Ordering Information

Part Number	Temperature Range	Package Description	Shipping
FXAS21002CQR1	–40 °C to +85 °C	QFN	Tape and reel (1 k)

Related Documentation

The FXAS21002C device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents, go to freescale.com/FXAS21002C, and then click on the Documentation tab.

Table of Contents

1 General Description

1.1 Block Diagram

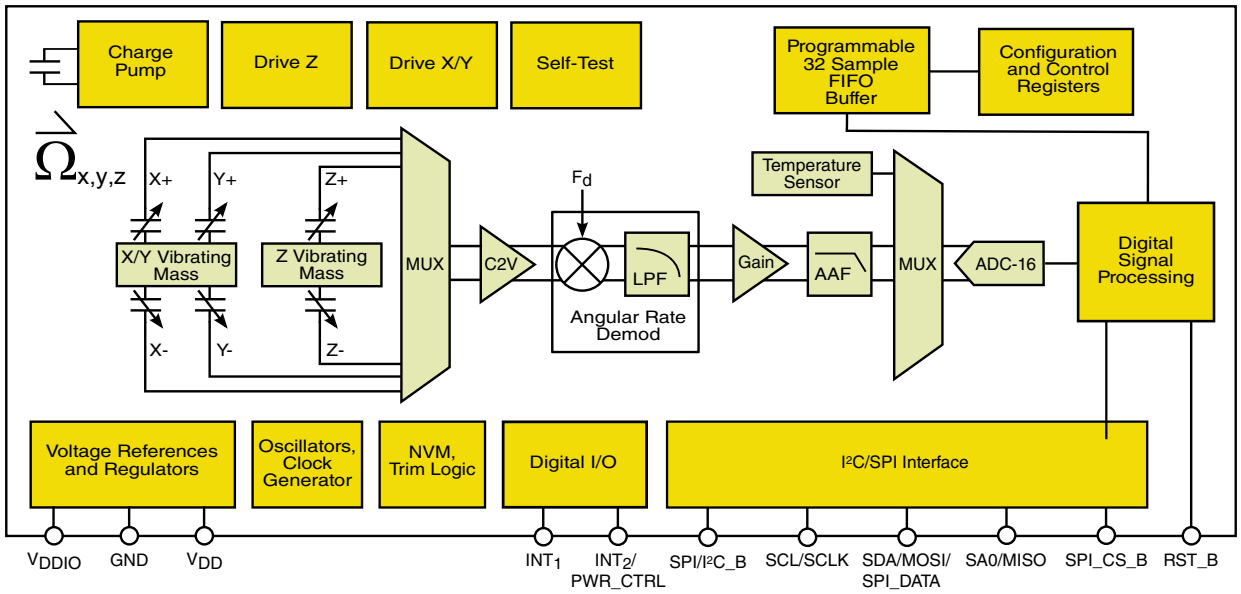


Figure 1. Block Diagram

1.2 Pinout

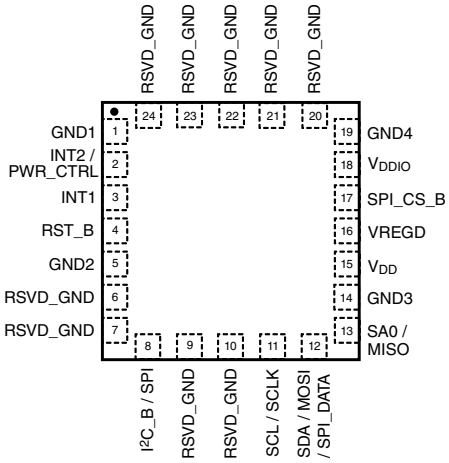


Figure 2. Device pinout (top view)

Table 1. Pin functions

Pin	Name	Function
1	GND1	Ground
2	INT2 / PWR_CTRL[1]	Interrupt Output 2 / Power state transition control input
3	INT1	Interrupt Output 1
4	RST_B	Reset input, active low. Connect this pin to V_{DDIO} if unused.
5	GND2	Ground
6	RSVD_GND	Reserved - Must be tied to ground
7	RSVD_GND	Reserved - Must be tied to ground
8	I^2C_B / SPI	Digital interface selection pin. This pin must be tied high to select SPI interface mode, or low to select I^2C interface mode.
9	RSVD_GND	Reserved pin—must be tied to ground
10	RSVD_GND	Reserved pin—must be tied to ground
11	SCL/SCLK	I^2C / SPI clock
12	SDA / MOSI / SPI_Data	I^2C data / SPI 4-wire Master Out Slave In / SPI 3-wire data In/Out[2]
13	SA0/MISO	I^2C address bit0 / SPI 4-wire Master In Slave Out
14	GND3	Ground
15	V_{DD}	Supply voltage
16	V_{REGD}	Digital regulator output. Connect a 0.1 µF capacitor between this pin and ground
17	SPI_CS_B	SPI chip select input, active low. This pin must be held logic high when operating in I^2C interface mode (I^2C_B/SPI set to ground) to ensure correct operation.
18	V_{DDIO}	Interface supply voltage
19	GND4	Ground
20	RSVD_GND	Reserved - Must be tied to ground
21	RSVD_GND	Reserved - Must be tied to ground
22	RSVD_GND	Reserved - Must be tied to ground
23	RSVD_GND	Reserved - Must be tied to ground
24	RSVD_GND	Reserved - Must be tied to ground

1. INT2/PWR_CTRL becomes a high-impedance input with weak internal pull-up resistor when **CTRLREG3[**EXTCTRLEN**]** = 1; the pull-up resistor is referenced to VDDIO.
2. MOSI becomes a bidirectional data pin when FXAS21002C is operated in 3-wire SPI mode with **CTRL_REG0[**SPIW**]**=1.

1.3 System Connections

The FXAS21002C offers the choice of interfacing with a host processor through either I^2C or SPI interfaces. Figure 3 and Figure 4 show the recommended circuit connections for implementing both interface options.

1.3.1 Typical Application Circuit—I²C Mode

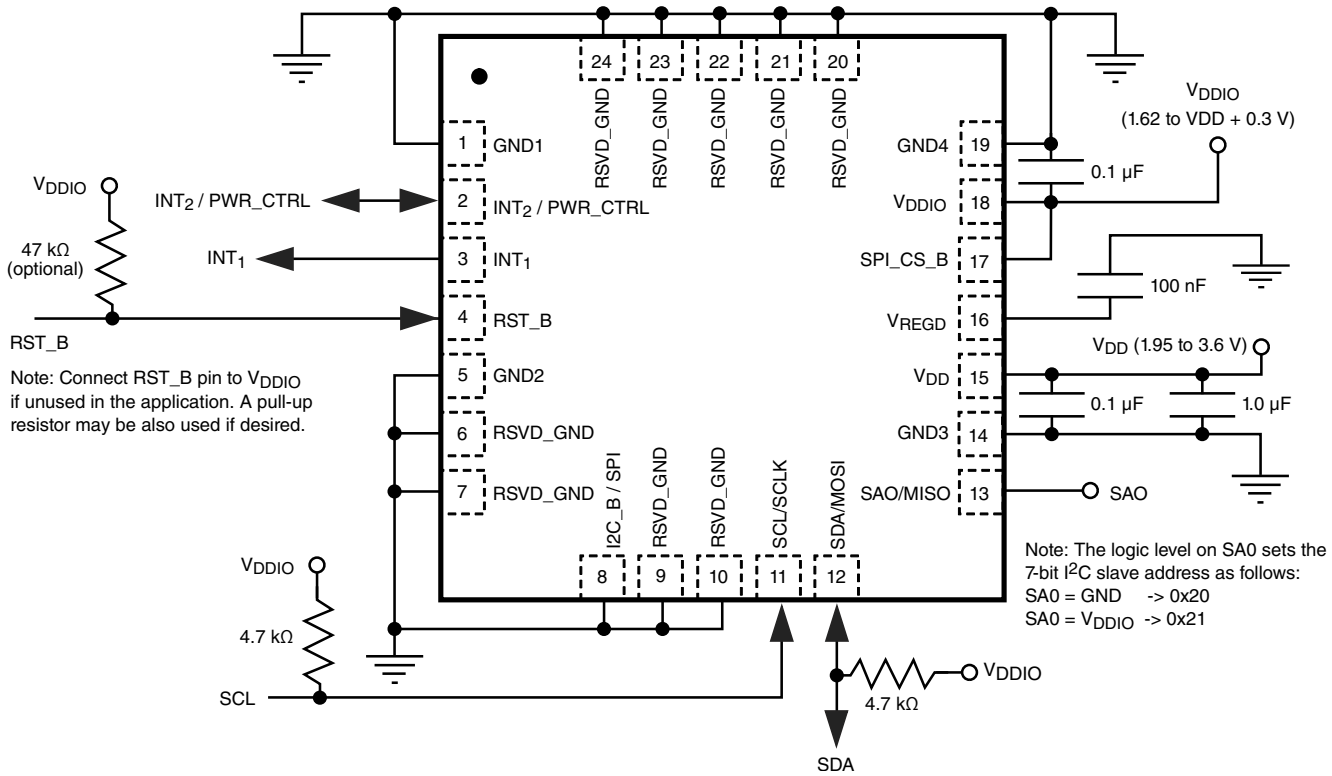


Figure 3. I²C mode electrical connections

1.3.2 Typical Application Circuit—SPI Mode

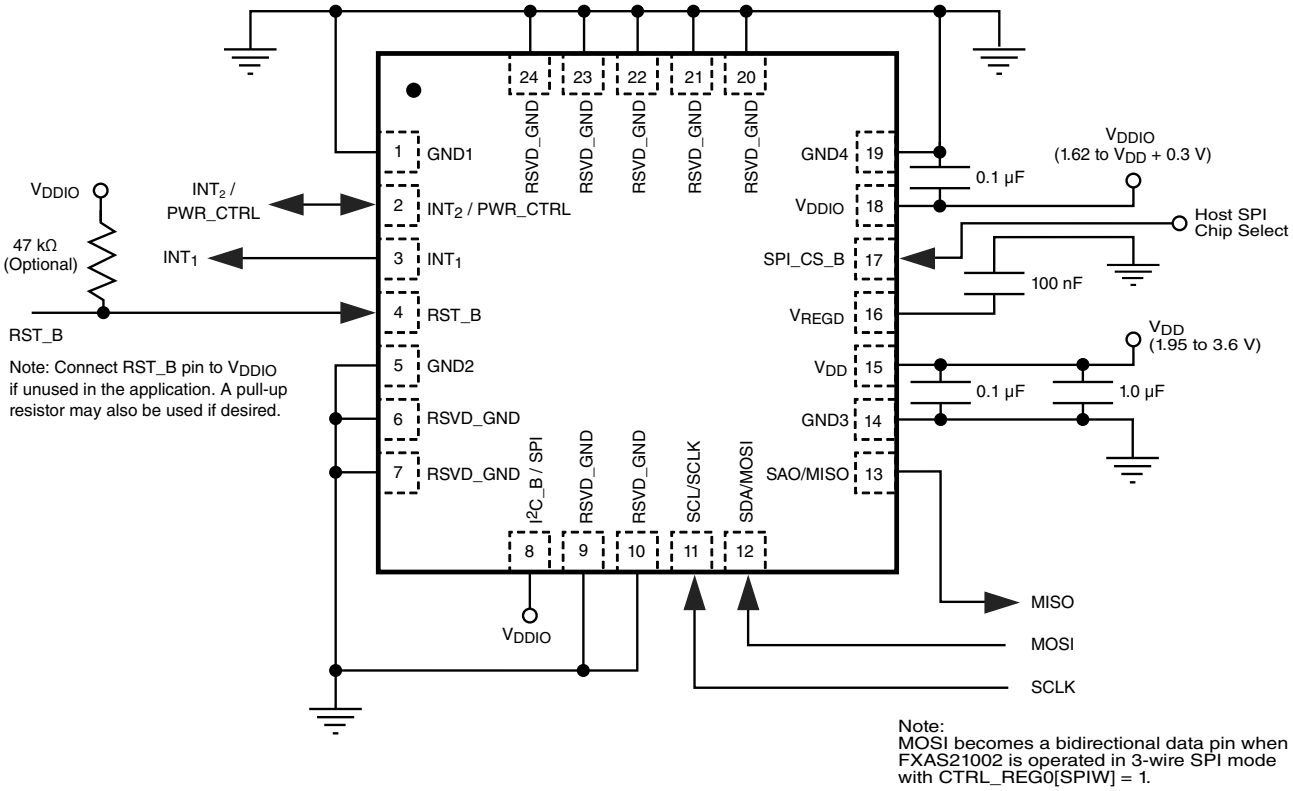


Figure 4. SPI mode electrical connections

1.4 Sensitive Axes Orientations and Polarities

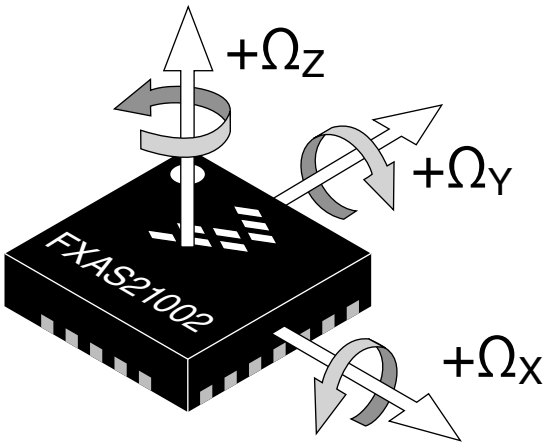


Figure 5. Reference frame for rotational measurement

2 Mechanical and Electrical Specifications

2.1 Absolute Maximum Ratings

Absolute maximum ratings are the limits the device can be exposed to without permanently damaging it. Absolute maximum ratings are stress ratings only; functional operation at these ratings is not guaranteed. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

This device contains circuitry to protect against damage due to high static voltage or electrical fields. It is advised, however, that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either GND or V_{DD}).

Table 2. Absolute maximum ratings

Rating	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	3.6	V
Interface supply voltage	V_{DDIO}	–0.3	3.6	V
Input voltage on any control pin (SA0, SCL, SDA, RST_B, PWR_CTRL)	V_{IN}	–0.3	V_{DDIO} +0.3	V
Maximum Acceleration (all axes, 100 µs)	g_{max}	—	5000	*g*
Operating temperature	T_{OP}	–40	+85	°C
Storage temperature	T_{STG}	–40	+125	°C

Table 3. ESD and latch-up protection characteristics

Rating	Symbol	Value	Unit
Human body model (HBM)	V_{HBM}	±2000	V
Machine model (MM)	V_{MM}	±200	V
Charge device model (CDM)	V_{CDM}	±500	V
Latch-up current at T = 85 °C	I_{LU}	±100	mA

	Caution
	This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

	Caution
	This is an ESD sensitive device, improper handling can cause permanent damage to the part.

2.2 Operating Conditions

Table 4. Nominal operating conditions

Rating	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	1.95	—	3.6	V
Interface supply voltage	V_{DDIO}	1.62	—	V_{DD} + 0.3	V
Digital high level input voltage: SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, SPI/ I^2C_B, RST_B, INT2/PWR_CTRL, SPI_CS_B pins	VIH	0.7 * V_{DDIO}	—	—	V
Digital low level input voltage: SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, SPI/ I^2C_B, RST_B, INT2/PWR_CTRL, SPI_CS_B pins	VIL	—	—	0.3 * V_{DDIO}	V
Operating temperature	Top	–40	+25	+85	°C

2.3 Mechanical Characteristics

Table 5. Mechanical characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC Resolution	n	—	—	16	—	bits
Full-scale range	FSR	**CTRL_REG0**[FS] = 00 **CTRL_REG0**[FS] = 01 **CTRL_REG0**[FS] = 10 **CTRL_REG0**[FS] = 11	—	±2000 ±1000 ±500 ±250	—	dps
Sensitivity	S_o	**CTRL_REG0**[FS] = 00 **CTRL_REG0**[FS] = 01 **CTRL_REG0**[FS] = 10 **CTRL_REG0**[FS] = 11	—	62.5 31.25 15.625 7.8125	—	mdps/LSB
Sensitivity Temperature Coefficient	ε_T	–40 to +85 °C	—	XY: ±0.08 Z: ±0.01	—	%/°C
Zero-rate Offset	D_O	**CTRL_REG0**[FS] = 00	—	±25	—	LSB
Zero-rate Offset, Post-Board Mount[1]	$D_{O\text{-}PBM}$	**CTRL_REG0**[FS] = 00	—	±50	—	LSB

Table continues on the next page...

Table 5. Mechanical characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Zero Rate Bias Temperature Coefficient	D_T	–40 to +85 °C	—	XY: ±0.02 Z: ±0.01	—	dps/°C
Cross axis sensitivity	CAS	max(S_{XY}, S_{XZ}, S_{YX}, S_{YZ}, S_{ZX}, S_{ZY})	—	±1.5	—	%
Integral nonlinearity (deviation from linear response)	INL	**CTRL_REG0[**FS] = 00	—	±0.5	—	%FSR
Self-test output change[2]	STOC	**CTRL_REG0[**FS] = 00	7000	16000	25000	LSB
Maximum output data rate	ODR_{MAX}	—	—	800	—	Hz
Noise density	ND	ODR = 200 Hz, **CTRL_REG0[**FS] = 00, **CTRL_REG0[**BW] = 00	—	0.025	—	dps/√Hz
Test conditions (unless otherwise noted): • V_{DD} = 2.5 V • V_{DDIO} = 1.8 V • T = 25 °C						

1. Post Board Mount Offset Specifications are based on an eight-layer PCB.
2. The Self-Test function can be used to verify the correct functioning of the ASIC measurement chain and gyro drive circuitry. The Self-Test function will only produce a meaningful result when the device is maintained stationary during the test. The Self-Test output value will be either positive or negative due to factory trimming, therefore, the absolute value of the Self-Test result should be used.

2.4 Electrical Characteristics

Table 6. Electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	1.95	2.5	3.6	V
Interface supply	V_{DDIO}	—	1.62	—	V_{DD}+0.3	V
Current consumption in Active mode	Idd_{Act}	Active mode	—	2.7	—	mA
Current consumption in Ready mode	Idd_{Rdy}	Ready mode	—	1.6	—	mA
Supply current drain in Standby mode	Idd_{Stby}	Standby mode	—	2.8	—	µA
Supply current in Standby mode over temperature	$IDD_{STBY-OT}$	–40 ≤ T ≤ 85 °C	—	—	7.5	µA
Digital high level input voltage SCL/SCLK, SDA/MOSI/ SPI_DATA, SA0/MISO, SPI/ I^2C_B, RST_B, INT2/ PWR_CTRL, SPI_CS_B	VIH	—	0.7 * V_{DDIO}	—	—	V

Table continues on the next page...

Table 6. Electrical characteristics (continued)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Digital low level input voltage SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, SPI/I^2C_B, RST_B, INT2/PWR_CTRL, SPI_CS_B	VIL	—	—	—	0.3 * V_{DDIO}	V
High-level output voltage INT1, INT2/PWR_CTRL, SDA/MOSI/SPI_DATA, SA0/MISO	VOH	I_O = 1 mA	0.9 * V_{DDIO}	—	—	V
Low-level output voltage INT1, INT2/PWR_CTRL, SDA/MOSI/SPI_DATA, SA0/MISO	VOL	I_O = 1 mA	—	—	0.1 * V_{DDIO}	V
Low-level output voltage SDA	VOL_{SDA1}	I_O = 3 mA, V_{DDIO} ≥ 2V	—	—	0.4 * V_{DDIO}	V
	VOL_{SDA2}	I_O = 3 mA, V_{DDIO} < 2V	—	—	0.2 * V_{DDIO}	
Output Data Rate frequency tolerance	ODR_{TOL}	—	—	±2.5	—	% ODR
Output Signal bandwidth	BW	—	4	< ODR/2	256	Hz
Standby to Active mode transition time	$T_{Stdy\text{-}Act}$	—	—	1/ODR + 60	—	ms
Ready to Active mode transition time	$T_{Rdy\text{-}Act}$	—	—	1/ODR + 5	—	ms
Test conditions (unless otherwise noted):						
• V_{DD} = 2.5 V • V_{DDIO} = 1.8 V • T = 25°C						

2.5 Temperature Sensor Characteristics

Table 7. Temperature sensor characteristics

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Full-scale range	T_{FSR}	—	–40	—	+85	°C
Operating temperature	T_{OP}	—	–40	+25	+85	°C
Sensitivity	T_{SENS}	—	—	1	—	°C/LSB
Test conditions (unless otherwise noted):						
• V_{DD} = 2.5 V • V_{DDIO} = 1.8 V						

3 Digital Interfaces

The registers embedded inside the device are accessed through either an I^2C or an SPI serial interface. To enable either interface, the V_{DDIO} line must be connected to the interface supply voltage. If V_{DD} is not present and V_{DDIO} is present, FXAS21002C is in shutdown mode and communications on the interface are ignored. If V_{DDIO} is maintained, V_{DD} can be powered off and the communications pins will be in a high impedance state. This will allow communications to continue on the bus with other devices.

Table 8. Serial interface pin descriptions

Pin name	Pin description
V_{DDIO}	Digital interface power
SPI_CS_B	SPI chip select
SCL/SCLK	I^2C/SPI serial clock
SDA/MOSI/SPI Data	I^2C serial data/SPI master serial data out slave serial data in /SPI 3-wire data input/output
SA0/MISO	I^2C least significant bit of the device address/SPI master serial data in slave serial data out
I^2C_B/SPI	Digital interface mode selection pin

3.1 I^2C Interface

To use the I^2C interface, the I^2C_B/SPI (pin 8) pin must be connected to GND (logic low) and the SPI_CS_B (pin 17) must be made logic high (by providing it a voltage equal to V_{DDIO}). FXAS21002C's I^2C interface is compliant with I^2C interface specification for Standard and Fast modes as outlined in the *I^2C-bus specification and user manual - Rev 4*, published by NXP Semiconductors. The 7-bit slave addresses that may be assigned to the device are 0x20 (with SA0 = 0) and 0x21 (with SA0 = 1). When I^2C_B/SPI is held low, the SA0/MISO pin is used to define the LSB of this I^2C address. This part does not implement clock stretching. See Table 9 for the I^2C slave addresses.

Table 9. I^2C Slave Addresses

Command	Device Address Bit[0] (SA0 pin state)	Slave Address Bits[6:0]	R/W Bit	Slave Address Byte Transmitted by Master
Read	0	0x20	1	0x41
Write	0	0x20	0	0x40
Read	1	0x21	1	0x43
Write	1	0x21	0	0x42

The key bus timing constraints are shown in Table 10. The I²C timing diagram is shown in Figure 6.

Table 10. Slave timing values

Parameter	Symbol	I²C Standard Mode[1, 2]		I²C Fast Mode[1, 2]		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Bus free time between STOP and START conditions	t_{BUF}	4.7	—	1.3	—	µs
Hold time (repeated) START condition	$t_{HD;STA}$	4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	—	0.6	—	µs
Set-up time for a STOP condition	$t_{SU;STO}$	4.0	—	0.6	—	µs
SDA valid time[2]	$t_{VD;DAT}$	—	3.45[3]	—	0.9[3]	µs
SDA valid acknowledge time[4]	$t_{VD;ACK}$	—	3.45[3]	—	0.9[3]	µs
SDA setup time	$t_{SU;DAT}$	250	—	100[5]	—	ns
SCL clock low time	t_{LOW}	4.7	—	1.3	—	µs
SCL clock high time	t_{HIGH}	4.0	—	0.6	—	µs
SDA and SCL rise time	t_r	—	1000	20	300	ns
SDA and SCL fall time[6]	t_f	—	300	$20*(V_{DDIO}/5.5\ V)$	300	ns
Capacitive load for each bus line[7]	C_b	—	400	—	400	pF
Pulse width of spikes on SDA and SCL that must be suppressed by the internal input filter	t_{SP}	0	50	0	50	ns

1. All values refer to VIH (min) and VIL (max) levels.
2. $t_{VD;DAT}$ refers to the time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
3. The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard mode and Fast mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.
4. $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5. A Fast-mode I²C device can be used in a Standard-mode I²C system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. Also, the acknowledge timing must meet this set-up time.
6. The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
7. C_b is the total capacitance of one bus line in pF; the maximum bus capacitance allowable may vary from this value depending on the application operating voltage and frequency.

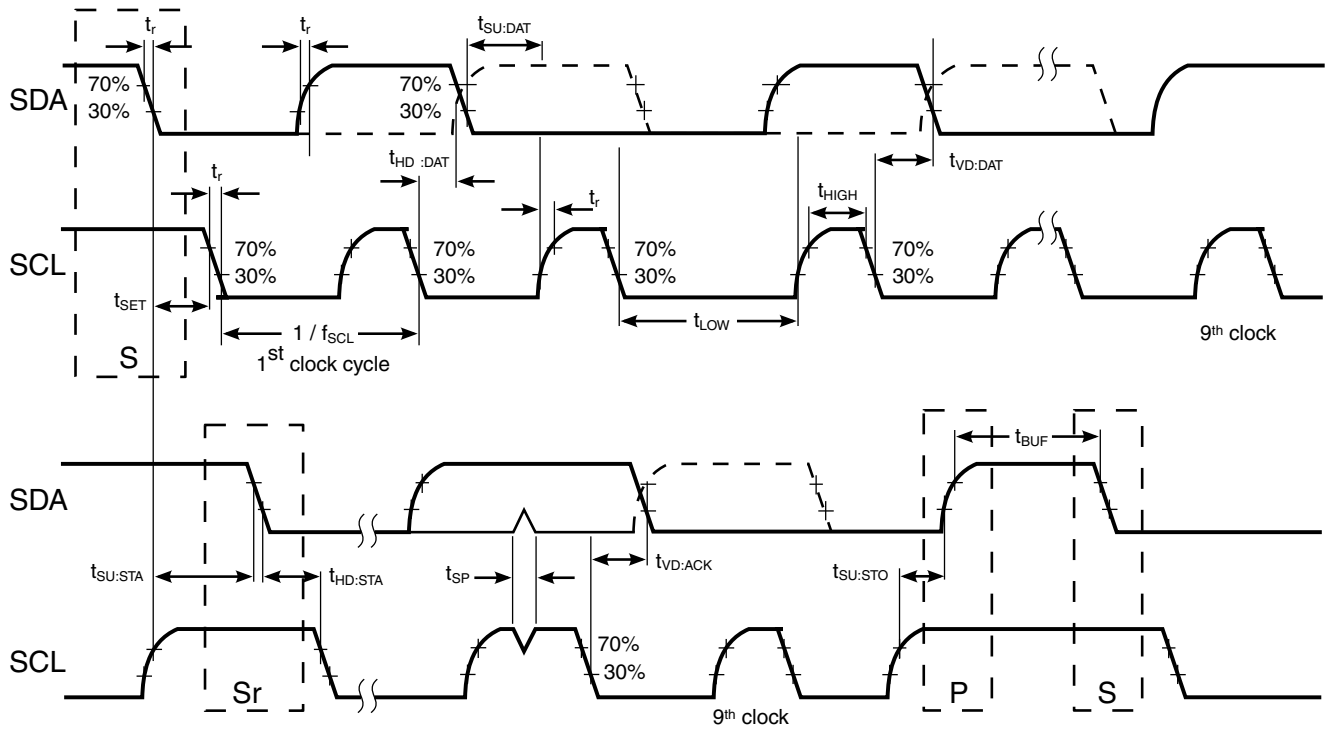


Figure 6. I²C timing diagram

3.1.1 I²C Operation

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The SDA is a bidirectional line used for sending and receiving the data to and from the interface. External pull-up resistors connected to V_{DDIO} are required for SDA and SCL. When the bus is free, the lines are high.

The maximum practical operating frequency for I²C in a given system implementation depends on several factors including the pull-up resistor values, and the total bus capacitance (trace + parasitic device capacitances).

A transaction on the bus is started through a start condition (ST) signal, which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After the ST signal has been transmitted by the master, the bus is considered busy. The next byte of data transmitted contains the slave address in the first seven bits, and the eighth bit, the read/write bit, indicates whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after the ST condition with its own address. If they match, the device considers itself addressed by the master. The ninth clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK).

The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains consistently low during the high period of the acknowledge clock period. The number of bytes per transfer is unlimited. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching. Not all receiver devices support clock stretching. Not all master devices recognize clock stretching.

A LOW-to-HIGH transition on the SDA line while SCL is high is defined as a stop condition (SP) signal. A write or burst write is always terminated by the master issuing the SP signal. A master should properly terminate a read by not acknowledging a byte at the appropriate time in the protocol. A master may also issue a repeated start signal (SR) during a transfer.

3.1.2 I²C Read Operations

3.1.2.1 Single-Byte Read

The master (or MCU) transmits an ST to the FXAS21002C, followed by the slave address, with the R/W bit set to “0” for a write, and the FXAS21002C sends an acknowledgement. Then, the MCU transmits the address of the register to read and the FXAS21002C sends an acknowledgement. The MCU transmits an SR, followed by the byte containing the slave address and the R/W bit set to “1” for a read from the previously selected register. The FXAS21002C then acknowledges and transmits the data from the requested register. The master transfers a NACK followed by an SP, signaling an end of transmission.

3.1.2.2 Multiple-Byte Read

When performing a multiple-byte or burst read, the FXAS21002C increments the register address read pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential registers after each FXAS21002C ACK is received. This continues until the master transfers a NACK followed by an SP, signaling an end of transmission.

3.1.3 I²C Write Operations

3.1.3.1 Single-Byte Write

To start a write command, the master transmits an ST to the FXAS21002C, followed by the slave address with the R/W bit set to “0” for a write, and the FXAS21002C sends an ACK. Then, the master transmits the address of the register to write to, and the FXAS21002C sends an ACK. Then, the master transmits the 8-bit data to write to the designated register and the FXAS21002C sends an ACK that it has received the data. Since this transmission is complete, the master transmits an SP to end the data transfer. The data sent to the FXAS21002C is now stored in the appropriate register.

3.1.3.2 Multiple-Byte Write

The FXAS21002C automatically increments the register address write pointer after a write command is received. Therefore, after following the steps of a single-byte write, multiple bytes of data can be written to sequential registers after each FXAS21002C ACK is received.

3.1.3.3 I²C Data Sequence Diagrams

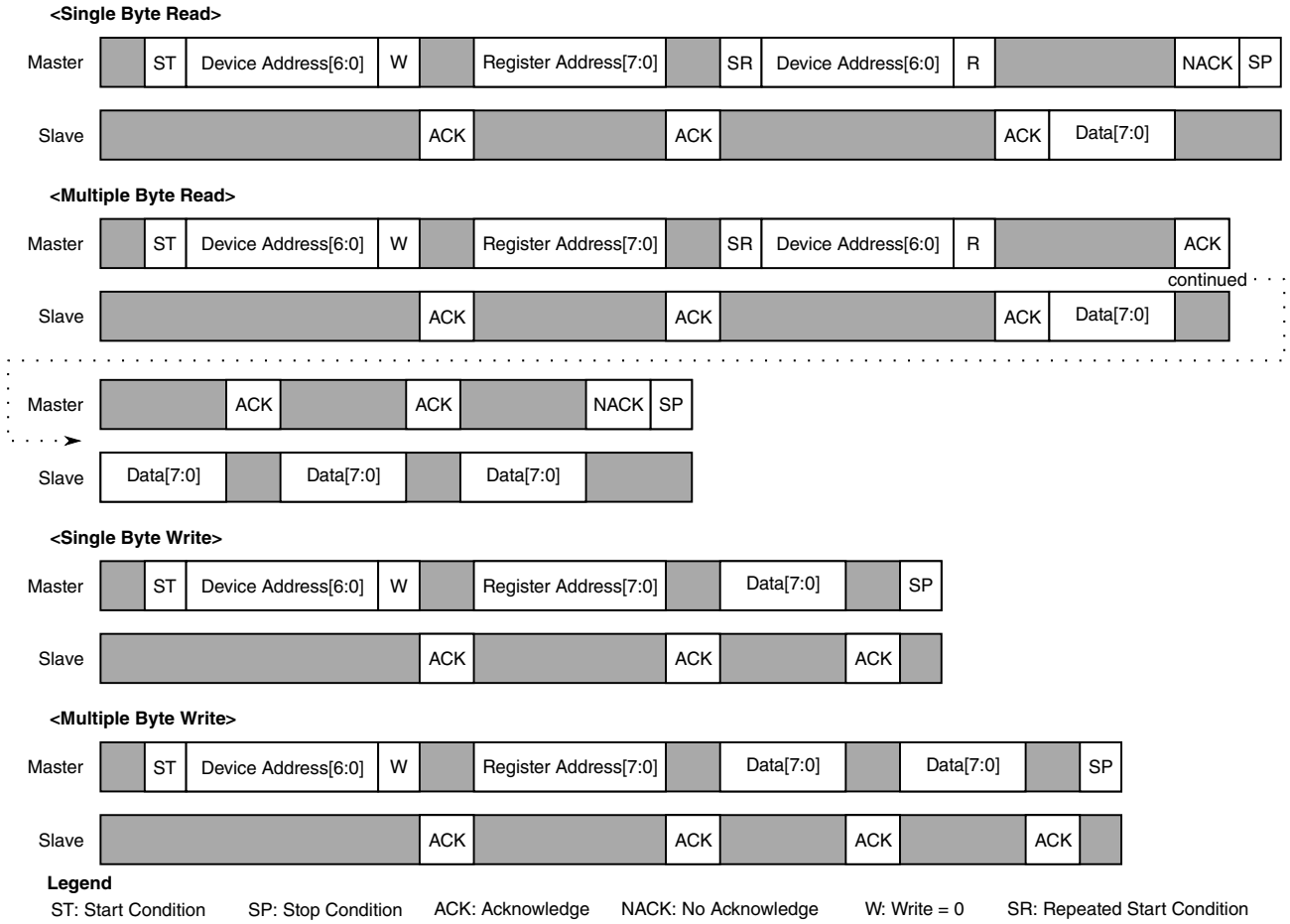


Figure 7. I²C data sequence diagram

3.2 SPI Interface

The SPI interface is a classical Master/Slave serial port. FXAS21002C is always considered to be the slave device and thus never initiates a communication with the host processor.

The SPI interface of FXAS21002C is compatible with SPI interface mode 00, corresponding to CPOL = 0 and CPHA = 0.

For CPOL = 0, the idle value of the clock is zero, and the active value of the clock is 1. For CPHA = 0, data is captured on the clock's rising edge (low to high transition) and data is propagated on the clock’s falling edge (high to low transition).

3.2.1 General SPI Operation

The SPI_CS_B pin is driven low at the start of a transaction, held low for the duration of the transfer, and then driven high again after the transaction is completed. During a transaction, the master toggles the clock (SCLK). The SCLK polarity is defined as having an idle value that is low, and an active phase that is high (CPOL = 0). Serial input and output data is captured on the clock's rising edge and propagated on the falling edge (CPHA = 0). Single byte read and single byte write operations are completed in 16 SCLK cycles; multiple byte reads and writes are completed in additional multiples of 8 SCLK cycles. The first SCLK cycle latches the most significant bit on MOSI to select whether the desired operation is a read (R/W = 1) or a write (R/W = 0). The following seven SCLK cycles are used to latch the slave register read or write address.

NOTE

4-wire SPI interface mode is the default out of POR or after a hard/soft reset. The 3-wire interface mode may be selected by setting **CTRL_REG0[**SPIW**]** = 1.

3.2.2 SPI Write Operations with 3- and 4-Wire Modes

A write operation is initiated by transmitting a 0 for the R/W bit. Then, the 7-bit register write address, A[6:0], is transmitted in MSb first order. The data byte to be written is then transferred during the second 8 SCLK cycle period (again, with MSb first). Figure 8 and Figure 9 shows the bus protocol for a single byte register write operation in either 3- or 4-wire SPI modes.

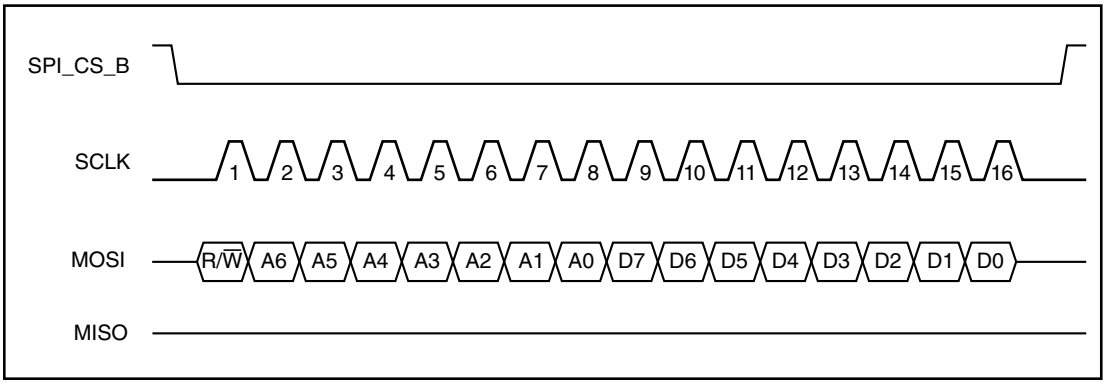


Figure 8. SPI single byte write protocol diagram (4-wire mode), R/W = 0

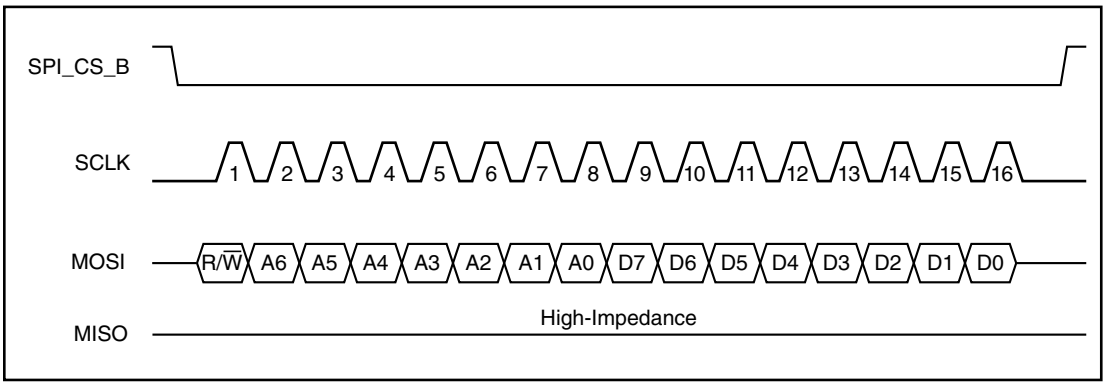


Figure 9. SPI single byte write protocol diagram (3-wire mode), R/W = 0

Multiple-byte write operations are performed similarly to the single-byte write sequence, but with additional data bytes transferred over every 8 SCLK cycle period. The register write address is internally auto-incremented by FXAS21002C so that every eighth clock edge will latch the address for the next register write address. When the desired number of bytes has been written, the rising edge on the SPI_CS_B pin terminates the transaction. Figure 10 and Figure 11 show the bus protocol for multiple byte register write operation in either 3- or 4-wire SPI modes.

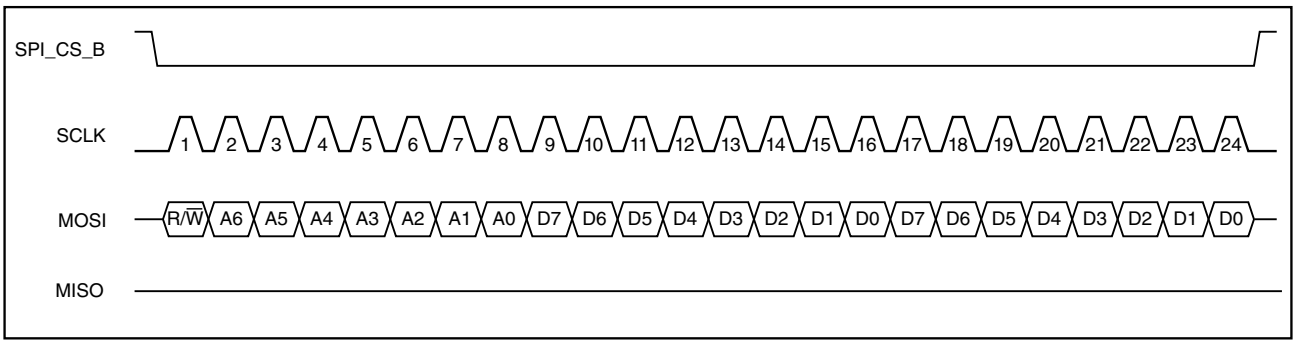


Figure 10. SPI multiple byte write protocol diagram (4-wire mode), R/W = 0

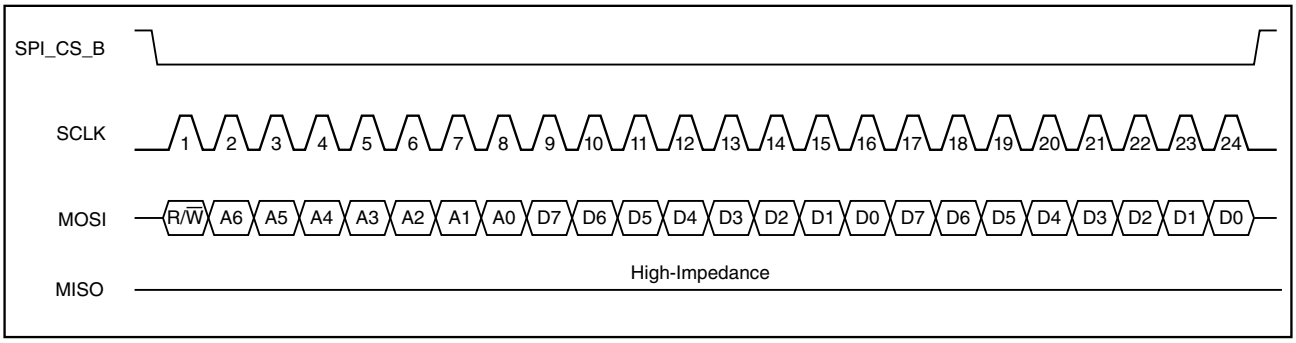


Figure 11. SPI multiple byte write protocol diagram (3-wire mode), R/W = 0

3.2.3 SPI Read Operations with 4-Wire Mode

NOTE

This description pertains only to the default SPI 4-wire interface mode (with CTRL_REG0[SPIW] = 0). This mode is the default out of POR, or after a hard/soft reset.

A register read operation is initiated by transmitting a 1 for the R/W bit. Then, the 7-bit register read address, A[6:0] is encoded in the first byte. The data is read from the MISO pin (MSB first). Figure 12 shows the bus protocol for a single byte read operation.

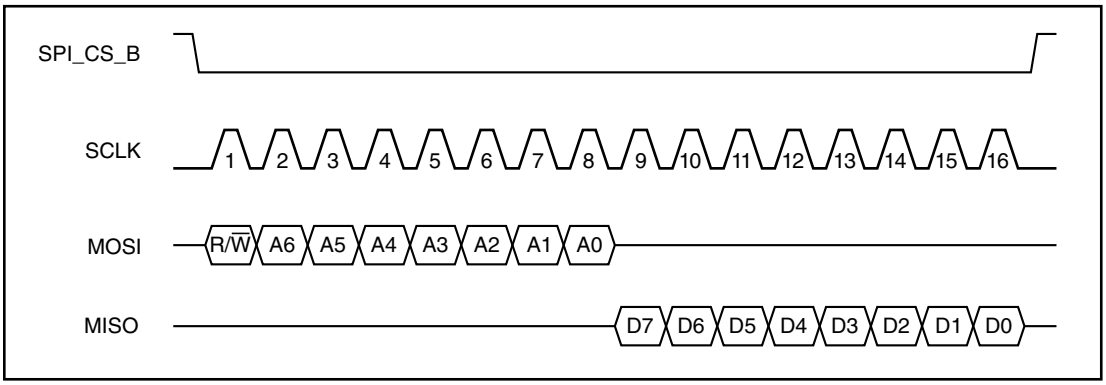


Figure 12. SPI single byte read protocol diagram (4-wire mode), R/W = 1

Multiple-byte read operations are performed similarly to single-byte reads; additional bytes are read in multiples of eight SCLK cycles. The register read address is auto-incremented by FXAS21002C so that every eighth clock edge will latch the address of the next register read address. When the desired number of bytes has been read, the rising edge on the SPI_CS_B terminates the transaction.

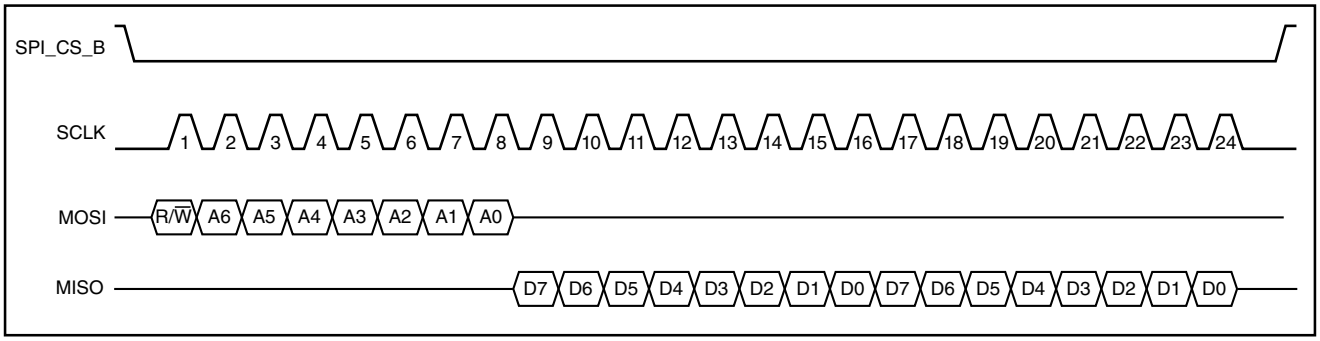


Figure 13. SPI multiple byte read protocol diagram (4-wire mode), R/W = 1

3.2.4 SPI Read Operations with 3-Wire Mode

NOTE

This description pertains only to the 3-wire SPI interface mode (with **CTRL_REG0[**SPIW**]** = 1). This interface mode is not the default and must be selected after a POR, or hard/soft reset.

FXAS21002C can be configured to operate in 3-wire SPI mode. In this mode the MISO pin is left unconnected or high-z, and the MOSI pin becomes a bi-directional input/output pin (SPI_DATA). 3-wire mode is selected by setting the SPIW bit in **CTRL_REG0**. Read operations in 3-wire mode are the same as in 4-wire mode except that at the end of address cycle, the MOSI (SPI_DATA) pin automatically switches from an input to an output.

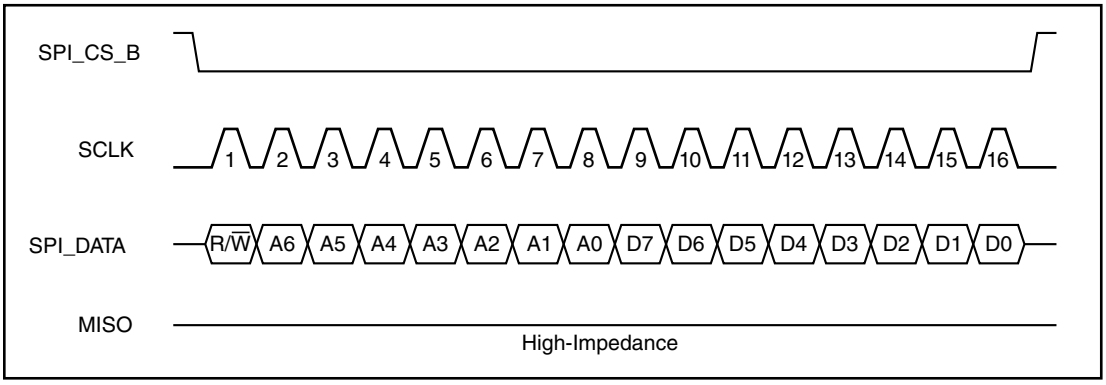


Figure 14. SPI single byte read protocol diagram (3-wire mode)

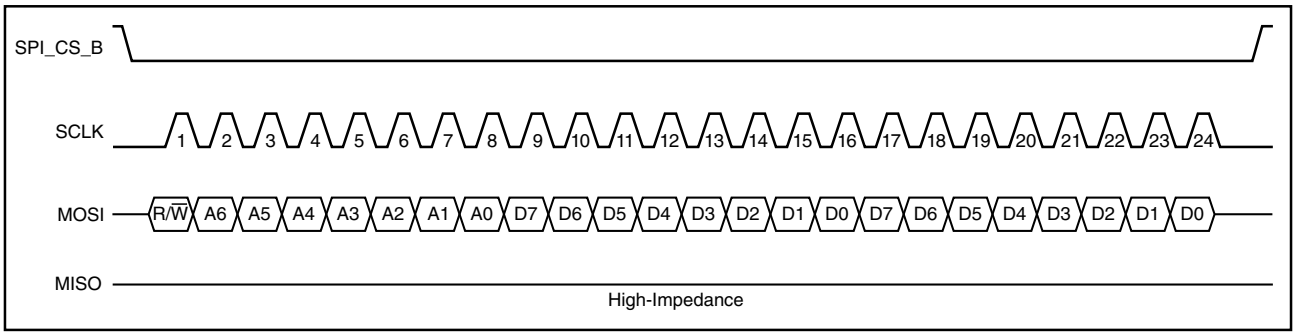


Figure 15. SPI multiple byte read protocol diagram (3-wire mode)

3.2.5 SPI Timing Specifications (4-wire mode)

Table 11 and Figure 16 specify and illustrate the minimum and maximum timing parameter values for correct SPI interface functionality when FXAS21002C is operated in 4-wire SPI mode. The timing delays given in Table 11 are taken at 70% of the rising edge and 30% of the falling edge. FXAS21002C only supports SPI mode 00, corresponding to CPOL = 0, and CPHA = 0. In this mode, the active state of the clock is high and the idle state is low. Data is latched on the rising edge of the clock and propagated on the falling edge. Please note that the timing parameters shown in Table 11 are based on simulations performed across process, voltage, and temperature with a total bus capacitance of 80 pF and a 10 kΩ pull-up resistor to VDDIO on each SPI interface pin (SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, and SPI_CS_B).

NOTE

In 4-wire SPI mode the MISO pin is always placed in a high impedance state when CS_B is not asserted (logic high level).

Table 11. Slave timing values

Label	Description	Specifications		Unit
		Min.	Max.	
fSCLK	SCLK frequency	0	2	MHz
tSCLK	SCLK Period	500	—	ns
tSCLKH	SCLK high time	210	—	ns
tSCLKL	SCLK low time	210	—	ns
tSZ	Setup time for MISO signal (transition out of high-z state)	—	130	
tHZ	Hold time for MISO signal (transition back to high-z state)	—	110	
tSCS	Setup time for SPI_CS_B signal	250	—	ns
tHCS	Hold time for SPI_CS_B signal	200	—	ns
tWCS	Inactive time for SPI_CS_B signal	110	—	ns
tSET	Data setup time for MOSI signal	20	—	ns
tHOLD	Data hold time for MOSI signal	200	—	ns
tDDLY	Data setup time for MISO signal	—	210	ns

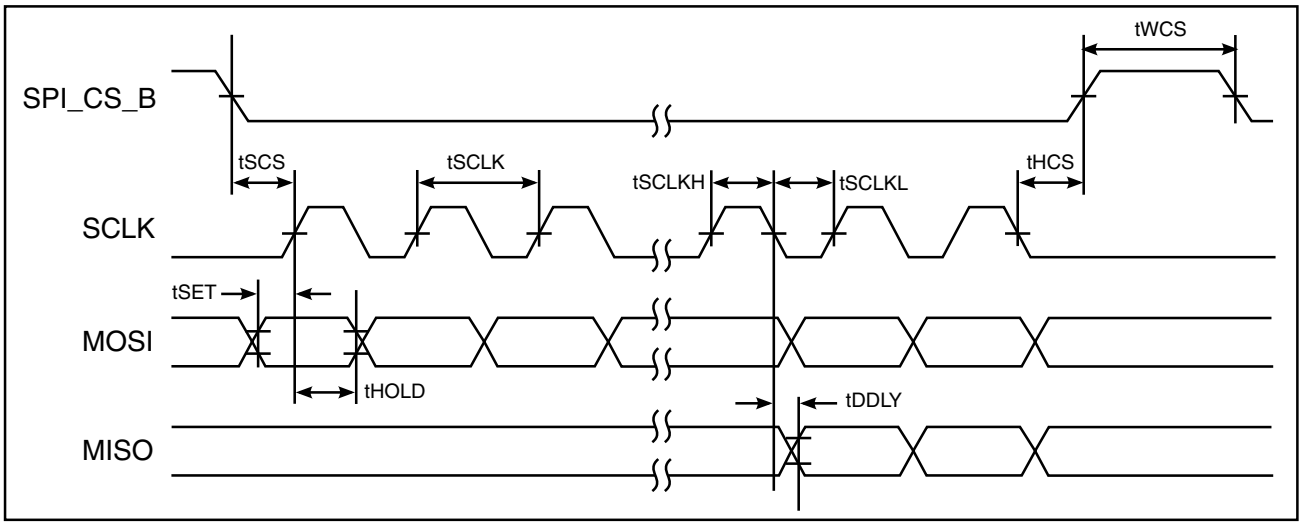


Figure 16. SPI timing diagram (4-wire mode)

3.2.6 SPI Timing Specifications (3-wire mode)

Table 12 and Figure 17 specify and illustrate the minimum and maximum timing parameter values for correct SPI interface functionality when FXAS21002C is operated in 3-wire SPI mode. The timing delays given in Table 12 are taken at 70% of the rising edge and 30% of the falling edge. FXAS21002C only supports SPI mode '00', corresponding to CPOL = 0, and CPHA = 0. In this mode, the active state of the clock is high and the idle state is low. Data is latched on the rising edge of the clock and propagated on the falling edge. Please note that the timing parameters shown in Table 12 are based on simulations performed across process, voltage, and temperature with a total bus capacitance of 80pF and a 10 kΩ pull-up resistor to VDDIO on each SPI interface pin (SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, and SPI_CS_B).

NOTE

When FXAS21002C is operated in 3-wire SPI mode - by setting CTRL_REG0[SPIW] = 1 - the SA0/MISO pin is always placed in a high impedance (high-z) state.

Table 12. Slave timing values

Label	Description	Specifications		Unit
		Min.	Max.	
fSCLK	SCLK frequency	0	1.4	MHz
tSCLK	SCLK Period	714	—	ns
tSCLKH	SCLK high time	300	—	ns

Table continues on the next page...

Table 12. Slave timing values (continued)

Label	Description	Specifications		Unit
		Min.	Max.	
tSCLKL	SCLK low time	300	—	ns
tHZ	Hold time for MISO signal (transition back to high-z state)	—	200	
tSCS	Setup time for SPI_CS_B signal	250	—	ns
tHCS	Hold time for SPI_CS_B signal	200	—	ns
tWCS	Inactive time for SPI_CS_B signal	200	—	ns
tSET	Data setup time for MOSI signal	20	—	ns
tHOLD	Data hold time for MOSI signal	200	—	ns
tDDLY	Data setup time for MISO signal	—	280	ns

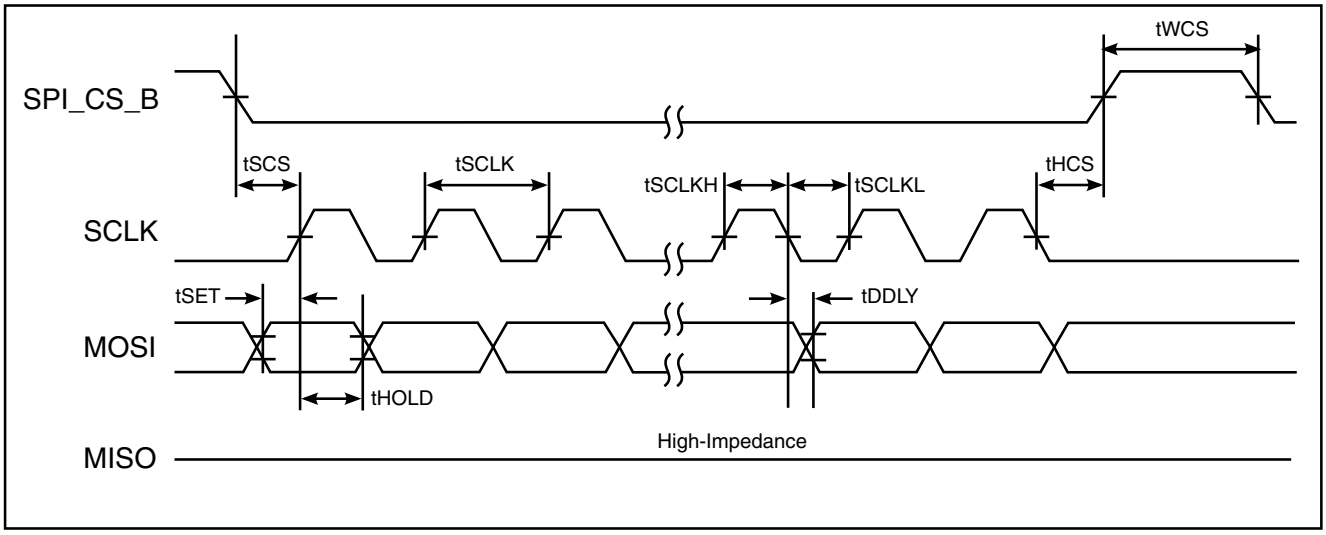


Figure 17. SPI timing diagram (3-wire mode)

4 Modes of Operation

The device may be placed into one of three functional modes:

- **Standby:** Some digital blocks are enabled; I^2C/SPI communication is possible. This mode is the minimum power consumption state for the device and is the default mode entered on POR or hard/soft reset. A transition from Standby mode to Active mode takes 1/ODR + 60 ms, typical.

- **Active:** All blocks are enabled (digital and analog); the device is actively measuring the angular rate at the ODR specified in 0x13: CTRL_REG1. This is the maximum power consumption state of the device.
- **Ready:** This mode is entered by setting **CTRL_REG1[**Ready**]** = 1. In this mode, the drive circuits are running but no measurements are being made. This mode offers the user the ability to significantly reduce the current draw of the device while providing a fast transition into Active mode within 1/ODR + 5 ms.

NOTE

When **CTRL_REG3[**EXTCTRLEN**]** = 0, the Active mode is entered/exited using the register interface (**CTRL_REG1[**ACTIVE**]** bit). When **CTRL_REG3[**EXTCTRLEN**]** = 1, the Active mode is entered/exited via the logic state on the PWR_CTRL input pin (pin 2).

The functional mode is selected using CTRL_REG1. After a POR (Power on Reset), a boot sequence is performed by the device and the registers are loaded with their preset values. After the boot sequence completes, the default operating mode of FXAS21002C is Standby mode.

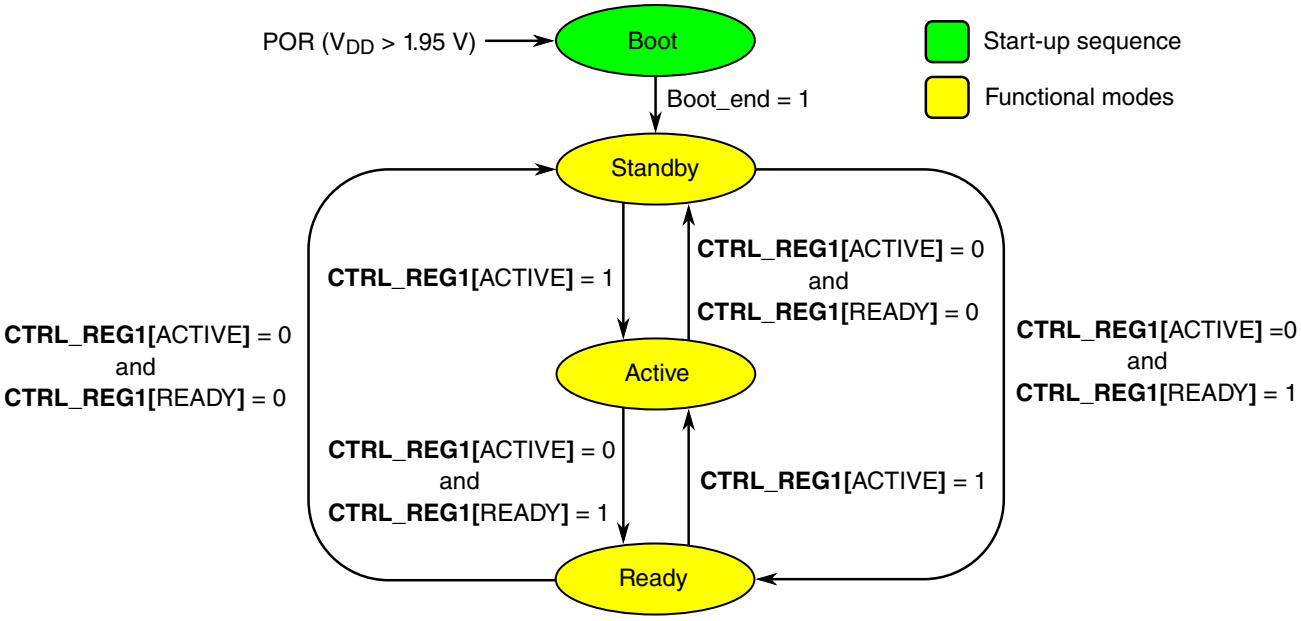


Figure 18. Functional mode transition diagram with CTRL_REG3[EXTCTRLEN] = 0