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FXTH870x6 Tire Pressure Monitor Sensor

The FXTH870x6 family is comprised of the following functions all within the same package.

Features

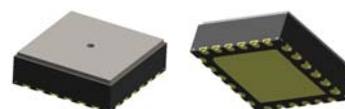
- Pressure sensor with one of two calibrated pressure ranges
 - 100 - 450 kPa
 - 100 - 900 kPa
- Temperature sensor
- Optional XZ- or Z-axis accelerometer with adjustable offset option
- Voltage reference measured by ADC10
- Six-channel, 10-bit analog-to-digital converter (ADC10) with two external I/O inputs
- 8-bit MCU
 - S08 Core with SIM and interrupt
 - 512 RAM
 - 8K FLASH (in addition to 8K providing factory firmware and trim data)
 - 64-byte, low-power, parameter registers
- Dedicated state machines to sequence routine measurement and transmission processes for reduced power consumption
- Internal 315-/434-MHz RF transmitter
 - External crystal oscillator
 - PLL-based output with fractional-n divider
 - OOK and FSK modulation capability
 - Programmable data rate generator
 - Manchester, Bi-Phase or NRZ data encoding
 - 256-bit RF data buffer variable length interrupt
 - Direct access to RF transmitter from MCU for unique formats
 - Low power consumption (less than 8 mA at 434 MHz, 5 dBm at 3.0 V, 25 °C)
- Differential input LF detector/decoder on independent signal pins
- Seven multipurpose GPIO pins
 - Four pins can be connected to optional internal pullups/pulldowns and STOP4 wakeup interrupt
 - Two of seven pins can be connected to a channel on the ADC10
 - Two of seven pins can be connected to a channel on the TPM1
- Real-Time Interrupt driven by LFO with interrupt intervals of 8, 16, 32, 64, 128, 256, 512 or 1024 ms
- Low-power, wakeup timer and periodic reset driven by LFO
- Watchdog timeout with selectable times and clock sources
- Two-channel general purpose timer/PWM module (TPM1)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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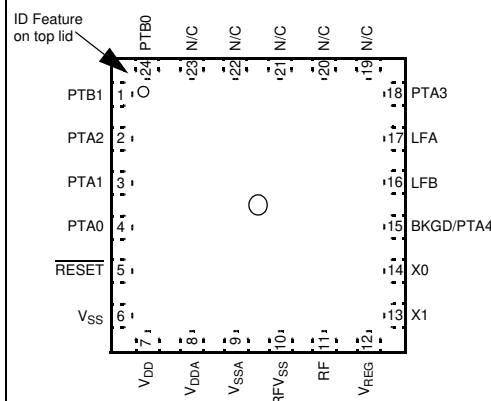
FXTH870x6

Top and bottom view



24-Pin, 1-hole lid
 7 x 7 QFN
 Case 2264-03

Top view



Pin connections

- Internal oscillators
 - MCU bus clock of 0.5, 1, 2 and 4 MHz (1, 2, 4 and 8 MHz HFO)
 - Low frequency, low power time clock (LFO) with 1 ms period
 - Medium frequency, controller clock (MFO) of 8 μ sec period
- Low-voltage detection
- Normal temperature restart in hardware (over- or under-temperature detected by software)

ORDERING INFORMATION					
Part number	Accelerometer axis	Package	Range	Code1	
FXTH8705026T1	Z	2264 (7 x 7, 1-hole lid)	100-450 kPa	\$08	
FXTH8705116T1	XZ	2264 (7 x 7, 1-hole lid)	100-450 kPa	\$0C	
FXTH8709026T1	Z	2264 (7 x 7, 1-hole lid)	100-900 kPa	\$18	
FXTH8709116T1	XZ	2264 (7 x 7, 1-hole lid)	100-900 kPa	\$1C	
FXTH8709126T1	XZ Ext. Range	2264 (7 x 7, 1-hole lid)	100-900 kPa	\$1E	
				Code1	Code0
FXTH8709226T1	XZ	2264 (7 x 7, 1-hole lid)	100-900 kPa	\$1C	Rel11

Related Documentation

The FXTH870x6 device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:
<http://www.freescale.com/>
2. In the Keyword search box at the top of the page, enter the device number FXTH870x6.

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1 General Information

1.1 Overall Block Diagram

The block diagram of the FXTH870x6 is shown in [Figure 1](#). This diagram covers all the main blocks mentioned above and their main signal interactions. Power management controls and bus control signals are not shown in this block diagram for clarity.

1.2 Multi-Chip Interface

The FXTH870x6 contains two to three devices using the best process technology for each.

- Microcontroller with accelerometer and pressure sensor interfaces, and RF transmitter (MCU)
- Optional ranges on pressure transducers
- Optional XZ- or Z-axis acceleration transducer

As shown in [Figure 1](#) the MCU interfaces to the RF transmitter using a standard memory mapped registers. The transducers connect to the MCU using custom analog interfaces and inter-chip bonding wires.

1.3 System Clock Distribution

The various clock sources and their distribution are shown in [Figure 2](#). All clock sources except the low frequency oscillator, LFO, can be turned off by software control in order to conserve power.

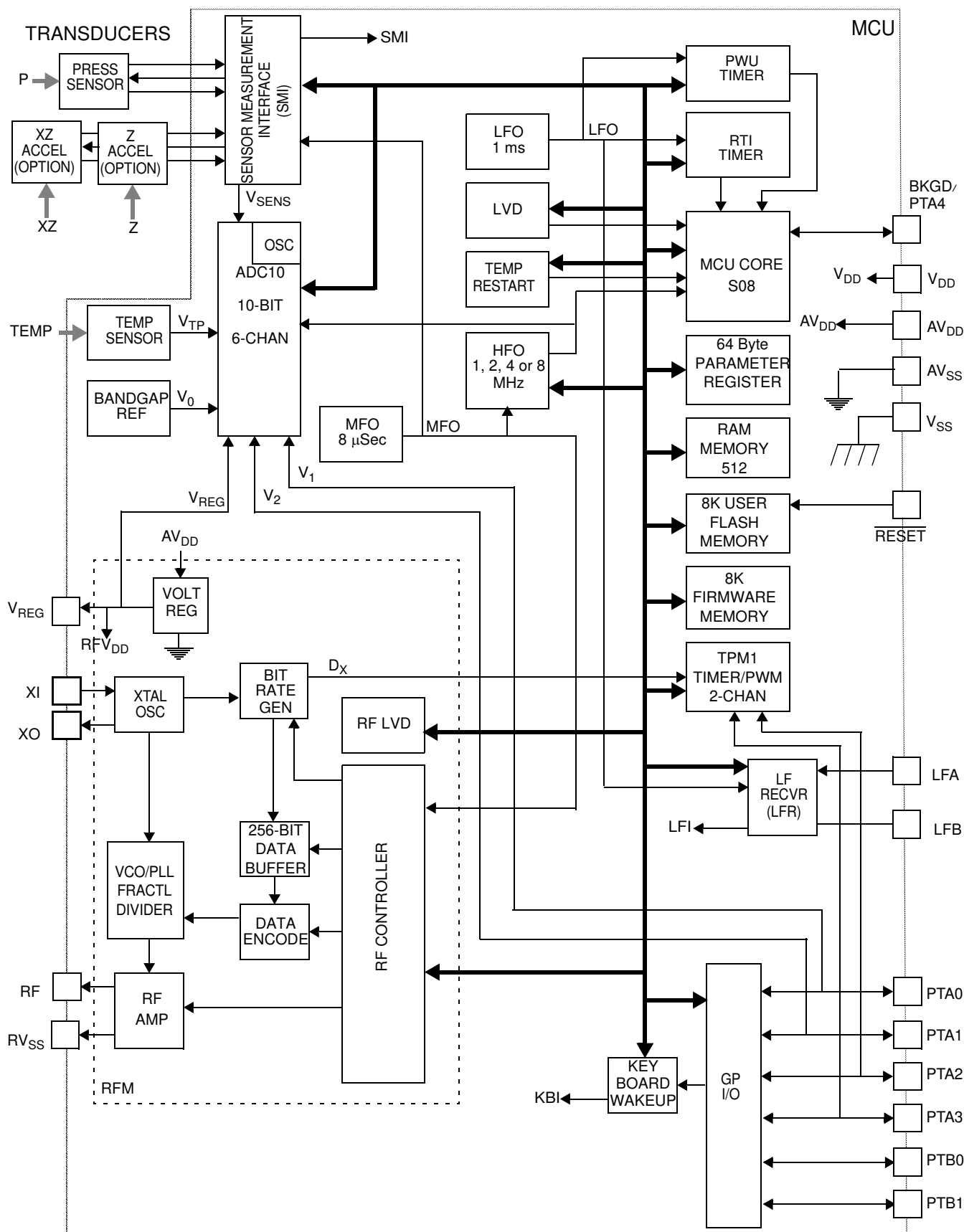


Figure 1. FXTH870x6 Overall Block Diagram

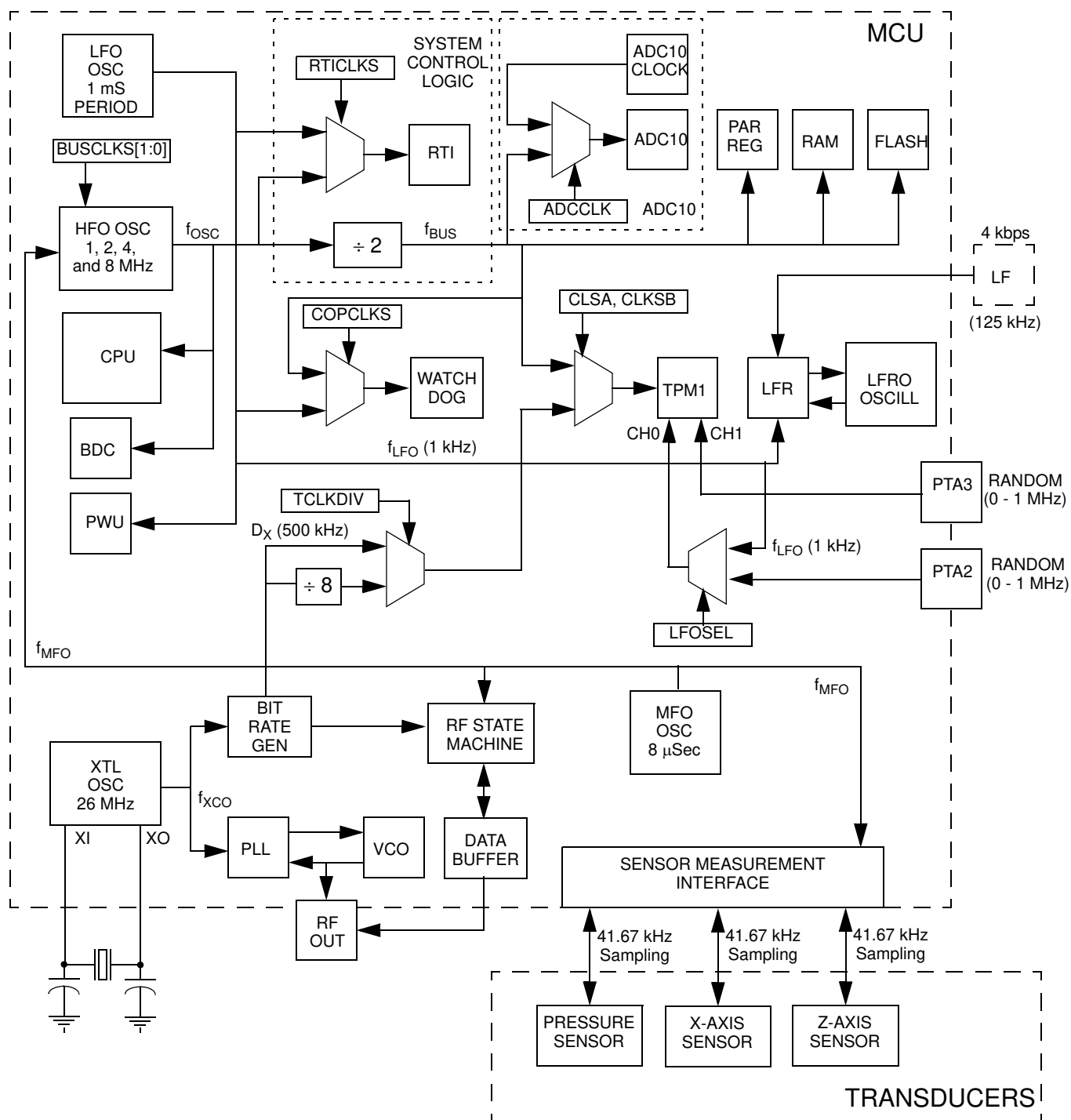


Figure 2. Clock Distribution

1.4 Reference Documents

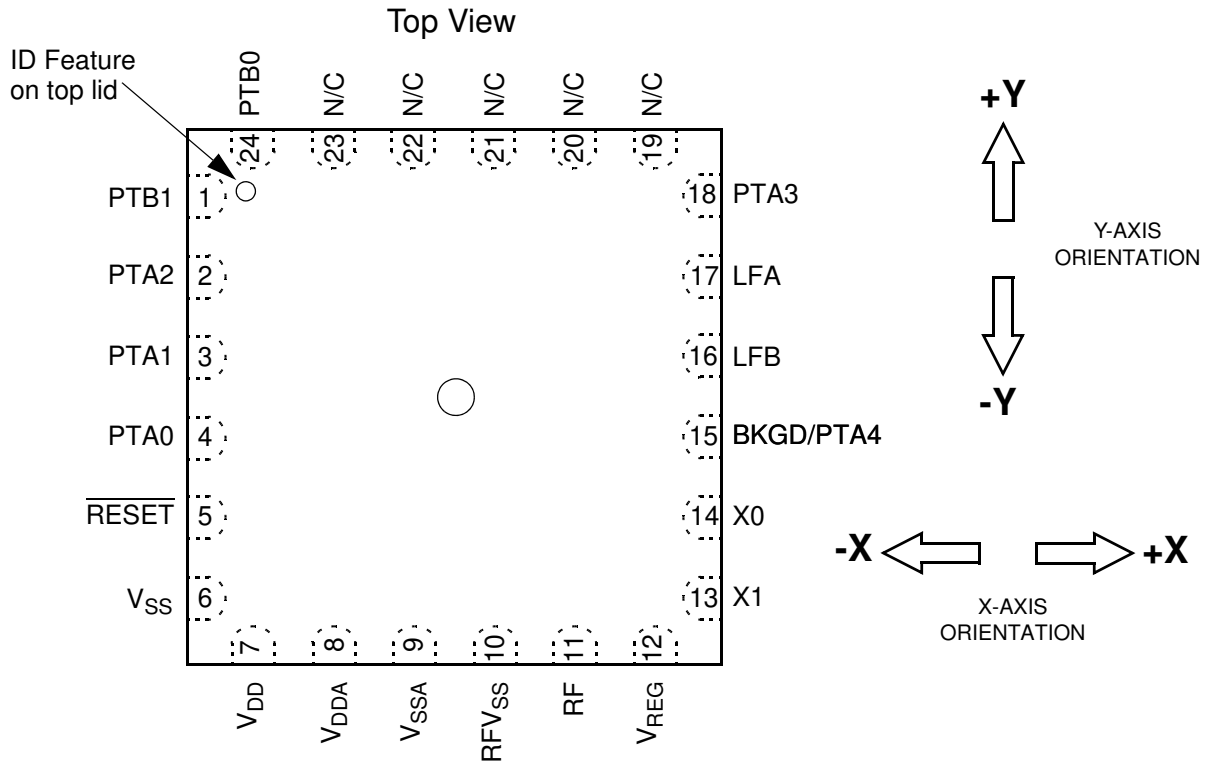
The FXTH870x6 utilizes the standard product MC9S08 CPU core. The user can obtain further detail on the full capabilities of this core by referring to the HCS08 Family Reference Manual (HCS08RMV1).

2 Pins and Connections

This section describes the pin layout and general function of each pin.

2.1 Package Pinout

The pinout for the FXTH870x6 device QFN package is shown in [Figure 3](#) for the orientation of the pressure port up. The orientation of the internal Z-axis accelerometer is shown in [Figure 4](#).



N/C = No Connect: Do not connect PCB pads to signal traces, power/ground or multi-layer via.

Figure 3. FXTH870x6 QFN Package Pinout

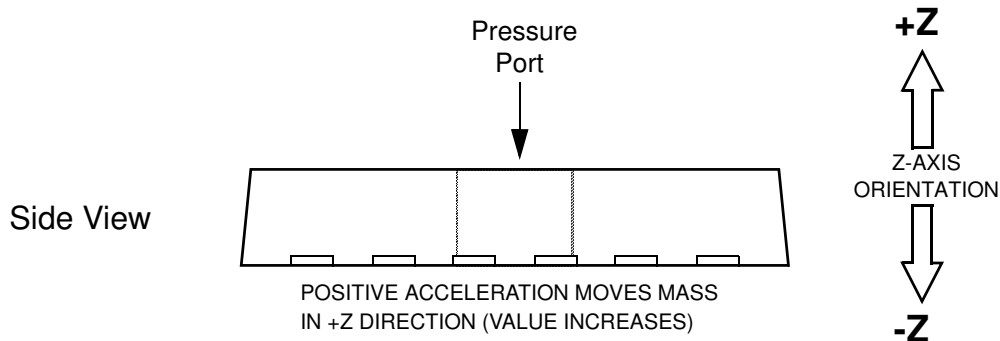


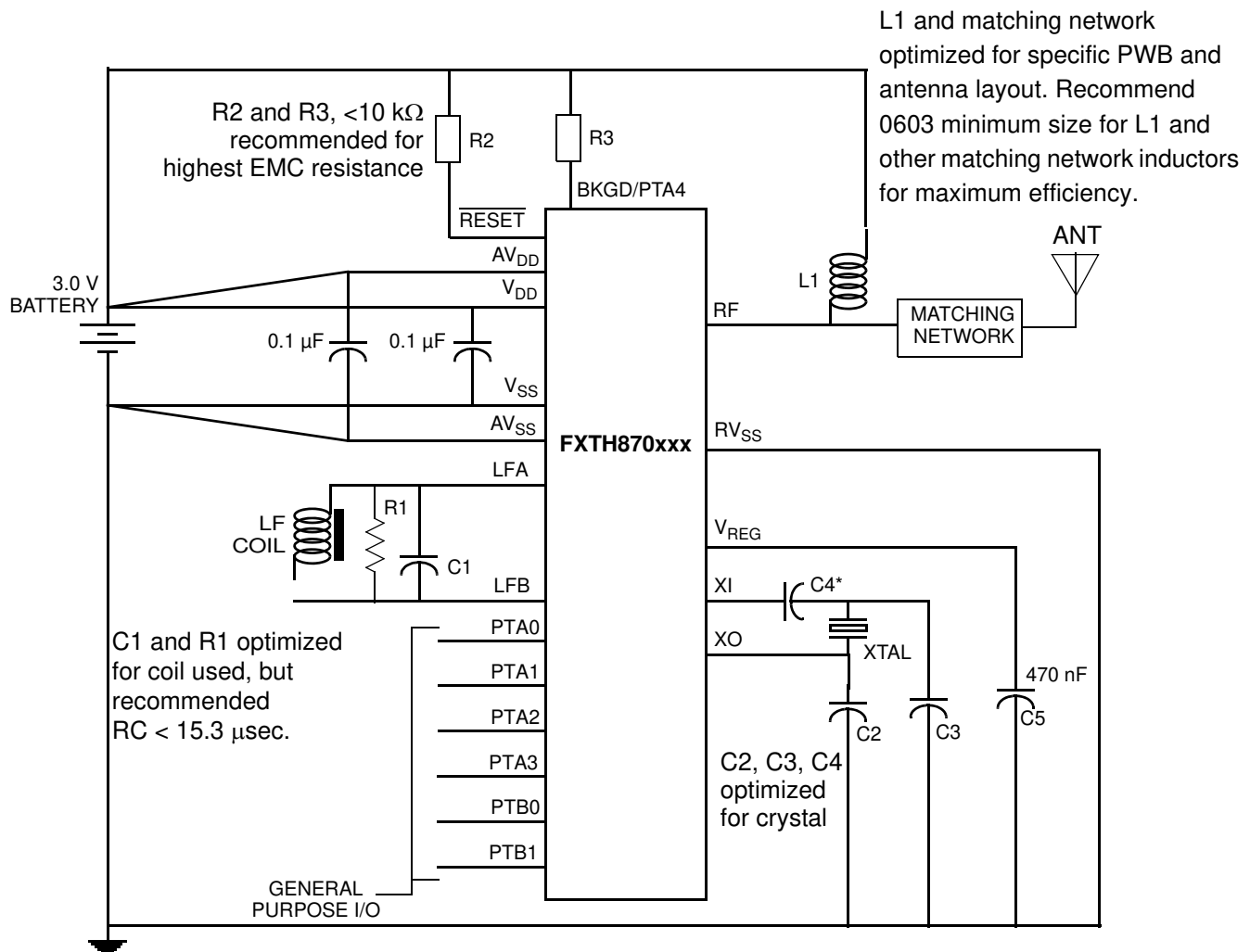
Figure 4. FXTH870x6 QFN Optional Z-axis Accelerometer Orientation

2.2 Recommended Application

Example of a simple OOK/FSK tire pressure monitors using the internal PLL-based RF output stage is shown in [Figure 5](#). Any of the PTA[3:0] pins can also be used as general purpose I/O pins. Any of the PTA[3:0] pins that are not used in the application should be handled as described in [Section 6.1](#).

2.3 Signal Properties

The following sections describe the general function of each pin.



The device C_4 , although drawn here as a capacitor, may be any type of passive component(s) sufficient to block or reduce unwanted external radiated signals from corrupting the crystal oscillator circuit: PCB traces for the LFA / LFB, AV_{DD} / V_{DD} , and V_{SS} / AV_{SS} pins and bypass capacitors should be minimized to reduce unwanted external radiated signals from corrupting the power input circuits.

Figure 5. FXTH870x6 Example Application

2.3.1 V_{DD} and V_{SS} Pins

The digital circuits operate from a single power supply connected to the FXTH870x6 through the V_{DD} and V_{SS} pins. V_{DD} is the positive supply and V_{SS} is the ground. The conductors to the power supply should be connected to the V_{DD} and V_{SS} pins and locally decoupled as shown in Figure 6.

Care should be taken to reduce measurement signal noise by separating the V_{DD} , V_{SS} , AV_{DD} , AV_{SS} and RV_{SS} pins using a “star” connection such that each metal trace does not share any load currents with other external devices as shown in Figure 6.

2.3.2 AV_{DD} and AV_{SS} Pins

The analog circuits operate from a single power supply connected to the FXTH870x6 through the AV_{DD} and AV_{SS} pins. AV_{DD} is the positive supply and AV_{SS} is the ground. The conductors to the power supply should be connected to the AV_{DD} and AV_{SS} pins and locally decoupled as shown in Figure 6.

Care should be taken to reduce measurement signal noise by separating the V_{DD} , V_{SS} , AV_{DD} , AV_{SS} and RV_{SS} pins using a “star” connection such that each metal trace does not share any load currents with other external devices as shown in Figure 6.

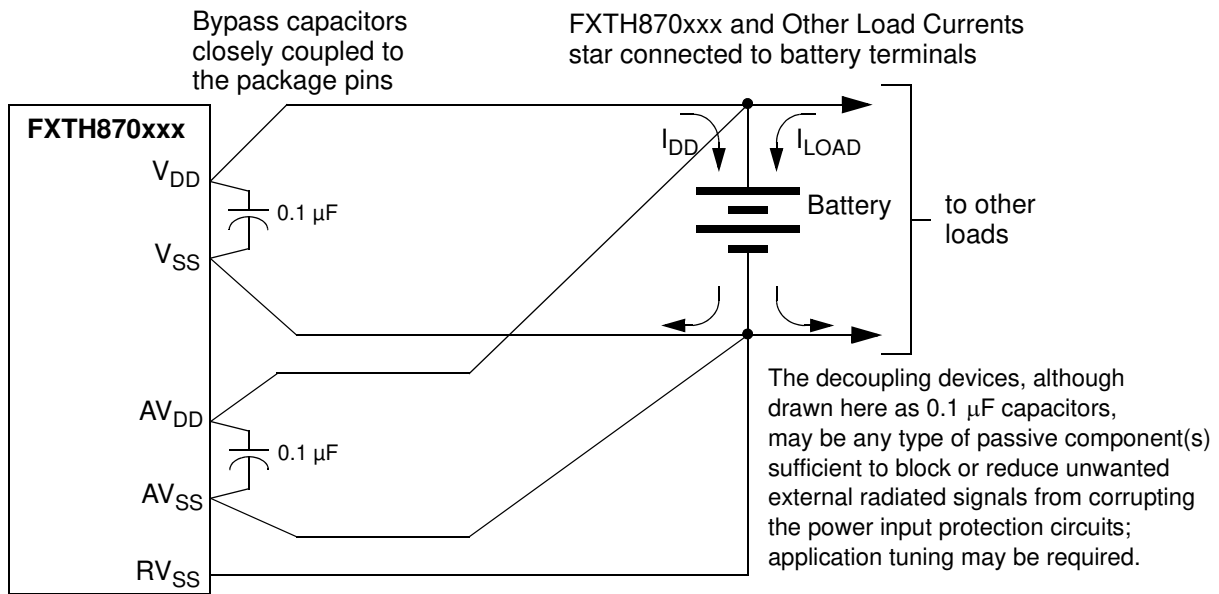


Figure 6. Recommended Power Supply Connections

2.3.3 V_{REG} Pin

The internal regulator for the analog circuits requires an external stabilization capacitor to AV_{SS} .

2.3.4 RV_{SS} Pin

Power in the RF output amplifier is returned to the supply through the RV_{SS} pin. This conductor should be connected to the power supply as shown in Figure 6 using a “star” connection such that each metal trace does not share any load currents with other supply pins.

2.3.5 RF Pin

The RF pin is the RF energy data supplied by the FXTH870x6 to an external antenna.

2.3.6 XO, XI Pins

The XO and XI pins are for an external crystal to be used by the internal PLL for creating the carrier frequencies and data rates for the RF pin.

2.3.7 LF[A:B] Pins

The LF[A:B] pins can be used by the LF receiver (LFR) as one differential input channel for sensing low level signals from an external low frequency (LF) coil. The external LF coil should be connected between the LFA and the LFB pins.

Signaling into the LFR pins can place the FXTH870x6 into various diagnostic or operational modes. The LFR is comprised of the detector and the decoder.

Each LF[A:B] pin will always have an impedance of approximately 500 k Ω to V_{SS} due to the LFR input circuitry. The LFA/LFB pins are used by the LFR when the LFEN control bit is set and are not functional when the LFEN control bit is clear.

2.3.8 PTA[1:0] Pins

The PTA[1:0] pins are general purpose I/O pins. These two pins can be configured as normal bidirectional I/O pins with programmable pullup or pulldown devices and/or wakeup interrupt capability; or one or both can be connected to the two input channels of the A/D converter module. The pulldown devices can only be activated if the wakeup interrupt capability is enabled. User software must configure the general purpose I/O pins so that they do not result in “floating” inputs as described in Section 6.1. PTA[1:02] map to keyboard Interrupt function bits [1:0].

2.3.9 PTA[3:2] Pins

The PTA[3:2] pins are general purpose I/O pin. These two pins can be configured as normal bidirectional I/O pin with programmable pullup or pulldown devices and/or wakeup interrupt capability; or one or both can be connected to the two input channels of the Timer Pulse Width (TPM1) module. The pulldown devices can only be activated if the wakeup interrupt capability is enabled. User software must configure the general purpose I/O pins so that they do not result in “floating” inputs as described in [Section 6.1](#). PTA[3:2] map to keyboard Interrupt function bits [3:2].

2.3.10 BKGD/PTA4 Pin

The BKGD/PTA4 pin is used to place the FXTH870x6 in the BACKGROUND DEBUG mode (BDM) to evaluate MCU code and to also transfer data to/from the internal memories. If the BKGD/PTA4 pin is held low when the FXTH870x6 comes out of a power-on reset the device will go into the ACTIVE BACKGROUND DEBUG mode (BDM).

The BKGD/PTA4 pin has an internal pullup device and can connected to V_{DD} in the application unless there is a need to enter BDM operation after the device as been soldered into the PWB. If in-circuit BDM is desired the BKGD/PTA4 pin can be left unconnected, but should be connected to V_{DD} through a low impedance resistor ($< 10\text{ k}\Omega$) which can be over-driven by an external signal. This low impedance resistor reduces the possibility of getting into the debug mode in the application due to an EMC event.

2.3.11 RESET Pin

The $\overline{\text{RESET}}$ pin is used for test and establishing the BDM condition and providing the programming voltage source to the internal FLASH memory. This pin can also be used to direct to the MCU to the reset vector as described in [Section 5.2](#).

The $\overline{\text{RESET}}$ pin has an internal pullup device and can connected to V_{DD} in the application unless there is a need to enter BDM operation after the device as been soldered to the PWB. If in-circuit BDM is desired the $\overline{\text{RESET}}$ pin can be left unconnected; but should be connected to V_{DD} through a low impedance resistor ($< 10\text{ k}\Omega$) which can be over-driven by an external signal. This low impedance resistor reduces the possibility of getting into the debug mode in the application due to an EMC event.

Activation of the external reset function occurs when the voltage on the RESET pin goes below $0.3 \times V_{DD}$ for at least 100 nsec before rising above $0.7 \times V_{DD}$ as shown in [Figure 7](#).

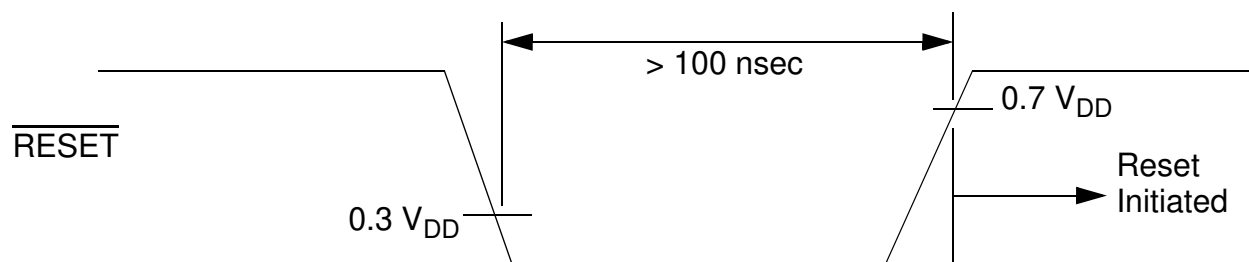


Figure 7. RESET Pin Timing

2.3.12 PTB[1:0] Pins

The PTB[1:0] pins are general purpose I/O pins. These two pins can be configured as nominal bidirectional I/O pins with programmable pullup. User software must configure the general purpose I/O pins so that they do not result in “floating” inputs as described in [Section 6.1](#).

3 Modes of Operation

The operating modes of the FXTH870x6 are described in this section. Entry into each mode, exit from each mode, and functionality while in each of the modes are described.

3.1 Features

- ACTIVE BACKGROUND DEBUG mode for code development
- STOP modes:
 - System clocks stopped
 - STOP1: Power down of most internal circuits, including RAM, for maximum power savings; voltage regulator in standby
 - STOP4: All internal circuits powered and full voltage regulation maintained for fastest recovery

3.2 RUN Mode

This is the normal operating mode for the FXTH870x6. This mode is selected when the BKGD/PTA4 pin is high at the rising edge of reset. In this mode, the CPU executes code from internal memory following a reset with execution beginning at address specified by the reset pseudo-vector (\$DFFE and \$DFFF).

3.3 WAIT Mode

The WAIT mode is also present like other members of the Freescale S08 family members; but is not normally used by the FXTH870x6 firmware or typical TPMS applications.

3.4 ACTIVE BACKGROUND Mode

The ACTIVE BACKGROUND mode functions are managed through the BACKGROUND DEBUG controller (BDC) in the HCS08 core. The BDC provides the means for analyzing MCU operation during software development.

ACTIVE BACKGROUND mode is entered in any of four ways:

- When the BKGD/PTA4 pin is low at the rising edge of a power up reset
- When a BACKGROUND command is received through the BKGD/PTA4 pin
- When a BGND instruction is executed by the CPU
- When encountering a BDC breakpoint

Once in ACTIVE BACKGROUND mode, the CPU is held in a suspended state waiting for serial BACKGROUND commands rather than executing instructions from the user's application program. Background commands are of two types:

- Non-intrusive commands, defined as commands that can be issued while the user program is running. Non-intrusive commands can be issued through the BKGD/PTA4 pin while the MCU is in RUN mode; non-intrusive commands can also be executed when the MCU is in the ACTIVE BACKGROUND mode. Non-intrusive commands include:
 - Memory access commands
 - Memory-access-with-status commands
 - BDC register access commands
 - The BACKGROUND command
- ACTIVE BACKGROUND commands, which can only be executed while the MCU is in ACTIVE BACKGROUND mode. ACTIVE BACKGROUND commands include commands to:
 - Read or write CPU registers
 - Trace one user program instruction at a time
 - Leave ACTIVE BACKGROUND mode to return to the user's application program (GO)

The ACTIVE BACKGROUND mode is used to program a bootloader or user application program into the FLASH program memory before the MCU is operated in RUN mode for the first time. When the FXTH870x6 is shipped from the Freescale factory, the FLASH program memory is erased by default (unless specifically requested otherwise) so there is no program that could be executed in RUN mode until the FLASH memory is initially programmed.

The ACTIVE BACKGROUND mode can also be used to erase and reprogram the FLASH memory after it has been previously programmed.

3.5 STOP Modes

One of two stop modes are entered upon execution of a STOP instruction when the STOPE bit in the system option register is set. In all STOP modes, all internal clocks are halted except for the low frequency 1 kHz oscillator (LFO) which runs continuously whenever power is applied to the V_{DD} and V_{SS} pins. If the STOPE bit is not set when the CPU executes a STOP instruction, the MCU will not enter any of the STOP modes and an illegal opcode reset is forced. The STOP modes are selected by setting the appropriate bits in SPMSC2. Table 1 summarizes the behavior of the MCU in each of the STOP1 and STOP4 modes. The STOP2 mode found in other Freescale S08 family members is not available; but the STOP3 mode is present like other members of the Freescale S08 family members.

3.5.1 STOP1 Mode

The STOP1 mode provides the lowest possible standby power consumption by causing the internal circuitry of the MCU to be powered down.

When the MCU is in STOP1 mode, all internal circuits that are powered from the voltage regulator are turned off. The voltage regulator is in a low-power standby state. STOP1 is exited by asserting either a reset or an interrupt function to the MCU.

Entering STOP1 mode automatically asserts LVD. STOP1 cannot be exited until the V_{DD} is greater than V_{LVDH} or V_{LV/DL} rising (V_{DD} must rise above the LVI re-arm voltage).

Upon wakeup from STOP1 mode, the MCU will start up as from a power-on reset (POR) by taking the reset vector.

NOTE

If there are any pending interrupts that have yet to be serviced then the device will not go into the STOP1 mode. Be certain that all interrupt flags have been cleared before entry to STOP1 mode.

3.5.2 STOP4 LVD Enabled in STOP Mode

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. If the LVD is enabled by setting the LVDE and the LVDSE bits in SPMSC1 when the CPU executes a STOP instruction, then the voltage regulator remains active during STOP mode. If the user attempts to enter the STOP1 with the LVD enabled in STOP (LVDSE = 1), the MCU will enter STOP4 instead.

Table 1. STOP Mode Behavior

Mode	STOP1	STOP4
LFO Oscillator, PWU	Always On & Clocking	
Real-Time Interrupt (RTI) ⁽¹⁾	Always On if using LFO as Clock	
MFO Oscillator ⁽²⁾	Optionally On	Optionally On
HFO Oscillator	Off	Off
CPU	Off	Standby
RAM	Off	Standby
Parameter Registers	On	On
FLASH	Off	Standby
TPM1 2-Chan Timer/PWM	Off	Off
Digital I/O	Disabled	Standby
Sensor Measurement Interface (SMI)	Off	Optionally On
Pressure P-cell	Off	Optionally On
Optional Acceleration g-cell	Off	Optionally On
Temperature Sensor (in ADC10)	Off	Optionally On ⁽³⁾
Normal Temperature Restart	Optionally On	Optionally On
Voltage Reference (in ADC10)	Off	Optionally On ⁽³⁾
LFR Detector ⁽⁴⁾	Periodically On	Periodically On
LFR Decoder	Optionally On	Optionally On
RF Controller, Data Buffer, Encoder	Optionally On	Optionally On
RF Transmitter ⁽⁵⁾	Optionally On	Optionally On
ADC10	Off	Optionally On ⁽³⁾

Table 1. STOP Mode Behavior (continued)

Mode	STOP1	STOP4
Regulator	Off	On
I/O Pins	Hi-Z	States Held
Wakeup Methods	Interrupts, resets	Interrupts, resets

1. RTI can be used in STOP1 or STOP4 if the clock selected is the LFO. To use the HFO as the clock the MCU must be in the RUN mode.
2. MFO oscillator started if the LFR detectors are periodically sampled, the LFR detectors detect an input signal; a pressure or acceleration reading is in progress or the RF state machine is sending data.
3. Requires internal ADC10 clock to be enabled.
4. Period of sampling set by MCU.
5. RF data buffer may be set up to run while the CPU is in the STOP modes.

Specific to the tire pressure monitoring application the parameter registers and the LFO with wakeup timer are powered up at all times whenever voltage is applied to the supply pins. The LFR detector and MFO may be periodically powered up by the LFR decoder.

3.5.3 Active BDM Enabled in STOP Mode

Entry into the ACTIVE BACKGROUND DEBUG mode from RUN mode is enabled if the ENBDM bit in BDCSCR is set. The BDCSCR register is not memory mapped so it can only be accessed through the BDM interface by use of the BDM commands READ_STATUS and WRITE_CONTROL. If ENBDM is set when the CPU executes a STOP instruction, the system clocks to the BACKGROUND DEBUG logic remain active when the MCU enters STOP mode so BACKGROUND DEBUG communication is still possible. In addition, the voltage regulator does not enter its low-power standby state but maintains full internal regulation. If the user attempts to enter the STOP1 with ENBDM set, the MCU will instead enter this mode which is STOP4 with system clocks running.

Most BACKGROUND commands are not available in STOP mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in STOP mode. The BACKGROUND command can be used to wake the MCU from stop and enter ACTIVE BACKGROUND mode if the ENBDM bit is set. Once in BACKGROUND DEBUG mode, all BACKGROUND commands are available.

3.5.4 MCU On-Chip Peripheral Modules in STOP Modes

When the MCU enters any STOP mode, system clocks to the internal peripheral modules except the wakeup timer and LFR detectors/decoder are stopped. Even in the exception case (ENBDM = 1), where clocks are kept alive to the BACKGROUND debug logic, clocks to the peripheral systems are halted to reduce power consumption.

I/O Pins

If the MCU is configured to go into STOP1 mode, the I/O pins are forced to their default reset state (Hi-Z) upon entry into stop. This means that the I/O input and output buffers are turned off and the pullup is disconnected.

Memory

All module interface registers will be reset upon wakeup from STOP1 and the contents of RAM are not preserved. The MCU must be initialized as upon reset. The contents of the FLASH memory are non-volatile and are preserved in any of the STOP modes.

Parameter Registers

The 64 bytes of parameter registers are kept active in all modes of operation as long as power is applied to the supply pins. The contents of the parameter registers behave like RAM and are unaffected by any reset.

LFO

The LFO remains active regardless of any mode of operation.

MFO

The medium frequency oscillator (MFO) will remain powered up when the MCU enters the STOP mode only when the SMI has been initiated to make a pressure or acceleration measurement; or when the RF transmitter's state machine is processing data.

HFO

The HFO is halted in all STOP modes.

PWU

The PWU remains active regardless of any mode of operation.

ADC10

The internal asynchronous ADC10 clock is always used as the conversion clock. The ADC10 can continue operation during STOP4 mode. Conversions can be initiated while the MCU is in the STOP4 mode. All ADC10 module registers contain their reset values following exit from STOP1 mode.

LFR

When the MCU enters STOP mode the detectors in the LFR will remain powered up depending on the states of the bits selecting the periodic sampling. Refer to [Section 12](#) for more details.

Bandgap Reference

The bandgap reference is enabled whenever the sensor measurement interface requires sensor or voltage measurements.

TPM1

When the MCU enters STOP mode, the clock to the TPM1 module stops and the module halts operation. If the MCU is configured to go into STOP1 mode, the TPM1 module will be reset upon wakeup from STOP and must be re-initialized.

Voltage Regulator

The voltage regulator enters a low-power standby state when the MCU enters any of the STOP modes except STOP4 (LVDSE = 1 or ENBDM = 1).

Temperature Sensor

The temperature sensor is powered up on command from the MCU.

Temperature Restart

When the MCU enters a STOP mode the temperature restart will remain powered up if the TRE bit is set. If the temperature restart level is reached the MCU will restart from the reset vector.

3.5.5 RFM Module in STOP Modes

The RFM's external crystal oscillator (XCO), bit rate generator, PLL, VCO, RF data buffer, data encoder, and RF output stage will remain powered up in STOP modes during a transmission, or if the SEND bit has been set and DIRECT mode has been enabled.

RF Output

When the RFM finishes a transmission sequence the external crystal oscillator (XCO), bit rate generator, PLL, VCO, RF data buffer, data encoder, and RF output stage will remain powered up if the SEND bit is set.

3.5.6 P-cell in STOP Modes

The P-cell is powered up only during a measurement if scheduled by the sensor measurement interface. Otherwise it is powered down.

3.5.7 Optional g-Cell in STOP Modes

The g-cell is powered up only during a measurement if scheduled by the sensor measurement interface. Otherwise it is powered down.

4 Memory

The overall memory map of the FXTH870x6 resides on the MCU.

4.1 MCU Memory Map

As shown in [Figure 8](#), MCU on-chip memory in the FXTH870x6 consists of parameter registers, RAM, FLASH program memory for nonvolatile data storage, and I/O and control/status registers. The registers are divided into four groups:

- Direct-page registers (\$0000 through \$004F)
- Parameter registers (\$0050 through \$008F)
- RAM (\$0090 through \$028F)
- High-page registers (\$1800 through \$182B)

DIRECT PAGE REGISTERS	\$0000 \$004F
PARAMETER REGISTERS	\$0050 \$008F
RAM 512 BYTES	\$0090 \$028F
UNIMPLEMENTED 5488 BYTES	\$0290 \$17FF
HIGH PAGE REGISTERS	\$1800 \$182B
41964 BYTES	\$182C \$BFFF
USER FLASH 8128 BYTES	\$C000 \$DFBF
USER VECTORS	\$DFC0 \$DFFF
FIRMWARE JUMP TABLE	\$E000 \$E03F
FIRMWARE FLASH 8128 BYTES	\$E040 \$FFFF

Figure 8. FXTH870x6 MCU Memory Map

The total programmable FLASH memory map is 16K, but the upper 8K is used for firmware and test software. Upon power up the firmware will initialize the device and redirect all vectors to the user area from \$DFC0 through \$DFFF. Any calls to the firmware subroutines are accessed through a jump table starting at location \$E000 (see [Section 14](#)).

4.2 Reset and Interrupt Vectors

[Table 2](#) shows address assignments for jump table to the reset and interrupt vectors. The vector names shown in this table are the labels used in the equate file provided by Freescale in the CodeWarrior project file.

Table 2. Vector Summary

User Vector Addr	Vector Name	Module Source
\$DFE0:DFE1	Vkbi	KBI
\$DFE2:DFE3	Reserved	
\$DFE4:DFE5	Reserved	
\$DFE6:DFE7	Vrti	Sys Ctrl - RTI
\$DFE8:DFE9	Vlfrcvr	LFR
\$DFEA:DFEB	Vadc1	ADC10
\$DFEC:DFED	Vrf	RFM

Table 2. Vector Summary (continued)

User Vector Addr	Vector Name	Module Source
\$DFEE:DFF0	Vsm	SMI
\$DFF0:DFF1	Vtpm1ovf	TPM1
\$DFF2:DFF3	Vtpm1ch1	TPM1
\$DFF4:DFF5	Vtpm1ch0	TPM1
\$DFF6:DFF7	Vwuktmr	PWU
\$DFF8:DFF9	Vlvd	Sys Ctrl - LVD
\$DFFA:DFFB	Reserved	
\$DFFC:DFFD	Vswi	SWI opcode
\$DFFE:DFFF	Vreset	Sys Ctrl - POR, PRF, COP, LVD Temp Restart, Illegal opcode or address

4.3 MCU Register Addresses and Bit Assignments

The registers in the FXTH870x6 are divided into these four groups:

- Direct-page registers are located in the first 80 locations in the memory map; these are accessible with efficient direct addressing mode instructions.
- The parameter registers begin at address \$0050; these are also accessible with efficient direct addressing mode instructions.
- High-page registers are used less often, so they are located above \$1800 in the memory map. This leaves more room in the direct page for more frequently used registers and variables.
- The nonvolatile register area consists of a block of 16 locations in FLASH memory at \$FFB0:FFBF. Nonvolatile register locations include:
 - Three values that are loaded into working registers at reset
 - An 8-byte back door comparison key that optionally allows the user to gain controlled access to secure memory.

Because the nonvolatile register locations are FLASH memory, they must be erased and programmed like other FLASH memory locations.

Direct page registers are located within the first 256 locations in the memory map, so they are accessible with efficient direct addressing mode instructions, which requires only the lower byte of the address. Bit manipulation instructions can be used to access any bit in any direct-page register. Table 3 is a summary of all user-accessible direct-page registers and control bits. Those related to the TPMS application and modules are described in detail in this specification.

The register names in column two of the following tables are shown in bold to set them apart from the bit names to the right. Cells that are not associated with named bits are shaded. A shaded cell with a 0 indicates this unused bit always reads as a 0. Shaded cells with dashes indicate unused or reserved bit locations that could read as 1s or 0s.

Table 3. MCU Direct Page Register Summary

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$0000	PTAD				PTAD[4:0]				
\$0001	PTAPE					PTAPE[3:0]			
\$0002	Reserved								
\$0003	PTADD					PTADD[3:0]			
\$0004	PTBD							PTBD[1:0]	
\$0005	PTBPE							PTBPE[1:0]	
\$0006	Reserved								
\$0007	PTBDD							PTBDD[1:0]	
\$0008	Reserved								
\$0009	Reserved								
\$000A	Reserved								
\$000B	Reserved								
\$000C	KBISC	0	0	0	0	KBF	KBACK	KBIE	KBIMOD

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Table 3. MCU Direct Page Register Summary (continued)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$000D	KBIPE					KBIPE[3:0]			
\$000E	KBIES					KBEDG[3:0]			
\$000F	Reserved								
\$0010	TPM1SC	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
\$0011	TPM1CNTH	Bit [15:8]							
\$0012	TPM1CNTL	Bit [7:0]							
\$0013	TPM1MODH	Bit [15:8]							
\$0014	TPM1MODL	Bit [7:0]							
\$0015	TPM1C0SC	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	0	0
\$0016	TPM1C0VH	Bit [15:8]							
\$0017	TPM1C0VL	Bit [7:0]							
\$0018	TPM1C1SC	CH1F	CH1IE	MS1B	MS1A	ELS1B	ELS1A	0	0
\$0019	TPM1C1VH	Bit [15:8]							
\$001A	TPM1C1VL	Bit [7:0]							
\$001B	Reserved								
\$001C	PWUDIV			WDIV[5:0]					
\$001D	PWUCS0	WUF	WUFAK	WUT[5:0]					
\$001E	PWUCS1	PRF	PRFAK	PRST[5:0]					
\$001F	PWUS	PSEL	0	CSTAT[5:0]					
\$0020-27	LFR Registers	LFR Registers, see Table 4 and Table 5							
\$0028	ADSC1	COCO	AIEN	ADCO	ADCH[4:0]				
\$0029	ADSC2	ADACT	ADTRG	ACFE	ADCFG	0	0	0	0
\$002A	ADRH	0	0	0	0	ADR[11:8]			
\$002B	ADRL	ADR[7:0]							
\$002C	ADCVH	0	0	0	0	ADCV[11:8]			
\$002D	ADCVL	ADCV[7:0]							
\$002E	ADCFG	ADLPC	ADIV[1:0]		ADLSMP	MODE[1:0]		ADICLK[1:0]	
\$002F	ADPCTL1	ADPC[7:0]							
\$0030-4F	RFM Registers	RFM Registers, see Table 6 and Table 7							
\$0050-8F	Parameter Reg	PARAM[63:0]							

Note: Shaded bits are recommended to only be controlled by firmware or factory test.

Table 4. LFR Register Summary - LPAGE = 0

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$0020	LFCTL1	LFEN	SRES	CARMOD	LPAGE	IDSEL[1:0]		SENS[1:0]	
\$0021	LFCTL2	LFSTM[3:0]				LFONTM[3:0]			
\$0022	LFCTL3	LFDO	TOGMOD	SYNC[1:0]		LFCDTM[3:0]			
\$0023	LFCTL4	LFDRIE	LFERIE	LFCDIE	LFIDIE	DECEN	VALEN	TIMOUT[1:0]	
\$0024	LFS	LFDRF	LFERF	LFCDF	LFIDF	LFOVF	LFEOMF	LPSM	LFIK
\$0025	LFDATA	RXDATA[7:0]							
\$0026	LFIDL	ID[7:0]							
\$0027	LFIDH	ID[15:8]							

Table 5. LFR Register Summary - LPAGE = 1

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$0020	LFCTL1	LFEN	SRES	CARMOD	LPAGE	IDSEL[1:0]		SENS[1:0]	
\$0021	LFCTRLE					TRIMEE	AZSC[2:0]		
\$0022	LFCTRLD	AVFOF[1:0]		DEQS	AZDC[1:0]		ONMODE	CHK125[1:0]	
\$0023	LFCTRLC	AMPGAIN[1:0]		FINSEL[1:0]		AZEN	LOWQ[1:0]		DEQEN
\$0024	LFCTRLB	HYST[1:0]		LFFAF	LFCAF	LFPOL	LFCPTAZ[2:0]		
\$0025	LFCTRLA	TESTSEL[3:0]				LFCC[3:0]			
\$0026	Reserved								
\$0027	Reserved								

Note: Shaded bits are recommended to only be controlled by firmware or factory test.

Table 6. RFM Register Summary - RPAGE = 0

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$0030	RFCR0	BPS[7:0]								
\$0031	RFCR1	FRM[7:0]								
\$0032	RFCR2	SEND	RPAGE	EOM	PWR[4:0]					
\$0033	RFCR3	DATA	IFPD	ISPC	IFID	FNUM[3:0]				
\$0034	RFCR4	RFBT[7:0]								
\$0035	RFCR5	BOOST	LFSR[6:0]							
\$0036	RFCR6	VCO_GAIN[1:0]		RFFT[5:0]						
\$0037	RFCR7	RFIF	RFEF	RFVF	RFIAK	RFIEN	RFLVDEN	RCTS	RFMRST	
\$0038	PLLCR0	AFREQ[12:5]								
\$0039	PLLCR1	AFREQ[4:0]					POL	CODE[1:0]		
\$003A	PLLCR2	BFREQ[12:5]								
\$003B	PLLCR3	BFREQ[4:0]					CF	MOD	CKREF	
\$003C	RFD0	RFD[7:0]								
\$003D	RFD1	RFD[15:8]								
\$003E	RFD2	RFD[23:16]								
\$003F	RFD3	RFD[31:24]								
\$0040	RFD4	RFD[39:32]								
\$0041	RFD5	RFD[47:40]								
\$0042	RFD6	RFD[55:48]								
\$0043	RFD7	RFD[63:56]								
\$0044	RFD8	RFD[71:64]]								
\$0045	RFD9	RFD[79:72]								
\$0046	RFD10	RFD[87:80]								
\$0047	RFD11	RFD[95:88]								
\$0048	RFD12	RFD[103:96]								
\$0049	RFD13	RFD[111:104]								
\$004A	RFD14	RFD[119:112]								
\$004B	RFD15	RFD[127:120]								
\$004C	Reserved									
\$004D	Reserved									
\$004E	Reserved									
\$004F	Reserved									

Note: Shaded bits are recommended to only be controlled by firmware or factory test.

Table 7. RFM Register Summary - RPAGE = 1

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$0030	RFCR0	BPS[7:0]							
\$0031	RFCR1	FRM[7:0]							
\$0032	RFCR2	SEND	RPAGE	EOM	PWR[4:0]				
\$0033	RFCR3	DATA	IFPD	ISPC	IFID	FNUM[3:0]			
\$0034	RFCR4	RFBT[7:0]							
\$0035	RFCR5	BOOST	LFSR[6:0]						
\$0036	RFCR6	VCO_GAIN[1:0]		RFFT[5:0]					
\$0037	RFCR7	RFIF	RFEF	RFVF	RFAK	RFIEN	RFLVDEN	RCTS	RFMRST
\$0038	EPR	—/VCD3	PLL_LPF_[2:0]/VCD[2:0]					PA_SLOPE	VCD_EN
\$0039	Reserved								
\$003A	Reserved								
\$003B	Reserved								
\$003C	RFD0	RFD[135:128]							
\$003D	RFD1	RFD[143:136]							
\$003E	RFD2	RFD[151:144]							
\$003F	RFD3	RFD[159:152]							
\$0040	RFD4	RFD[167:160]							
\$0041	RFD5	RFD[175:168]							
\$0042	RFD6	RFD[183:176]							
\$0043	RFD7	RFD[191:184]							
\$0044	RFD8	RFD[199:192]							
\$0045	RFD9	RFD[207:200]							
\$0046	RFD10	RFD[215:208]							
\$0047	RFD11	RFD[223:216]							
\$0048	RFD12	RFD[231:224]							
\$0049	RFD13	RFD[239:232]							
\$004A	RFD14	RFD[247:240]							
\$004B	RFD15	RFD[255:248]							
\$004C	Reserved								
\$004D	Reserved								
\$004E	Reserved								
\$004F	Reserved								

Note: Shaded bits are recommended to only be controlled by firmware or factory test.

4.4 High Address Registers

High-page registers are used much less often, so they are located above \$1800 in the memory map. This leaves more room in the direct page for more frequently used registers and variables. The registers control system level features as given in [Table 8](#).

Table 8. MCU High Address Register Summary

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$1800	SRS	POR	PIN	COP	ILOP	ILAD	PWU	LVD	0
\$1801	SBDFR	0	0	0	0	0	0	0	BDFR
\$1802	SIMOPT1	COPE	COPCLKS	STOPE	RFEN	TRE	TRH	BKGDPE	1
\$1803	SIMOPT2	0	COPT[2:0]			LFOSEL	TCLKDIV	BUSCLKS[1:0]	
\$1804	Reserved								
\$1805	Reserved								
\$1806	SDIDH	REV[3:0]				ID[11:8]			
\$1807	SDIDL	ID[7:0]							
\$1808	SRTISC	RTIF	RTIACK	RTICLKS	RTIE	0	RTIS[2:0]		
\$1809	SPMSC1	LVDF	LVDACK	LVDIE	LVDRE	LVDSE	LVDE	0	BGBE
\$180A	SPMSC2	0	0	0	PDF	0	PPDACK	PDC	0
\$180B	Reserved								
\$180C	SPMSC3	LVWF	LVWACK	LVDV	LVWV	0	0	0	0
\$180D	SIMSES			KBF	IRQF	TRF	PWUF	LFF	RFF
\$180E	SOTRM	SOTRM[7:0]							
\$180F	SIMTST		TRH[2:0]						TRO
\$1810-1F	Reserved								
\$1820	FCDIV	DIVLD	PRDIV8	DIV[5:0]					
\$1821	FOPT	KEYEN	FNORED	0	0	0	0	SEC0[1:0]	
\$1822	Reserved								
\$1823	FCNFG	0	0	KEYACC	0	0	0	0	0
\$1824	FPROT	FPS[7:1]							FPDIS
\$1825	FSTAT	FCBEF	FCCF	FPVIOL	FACCERR	0	FBLANK	0	0
\$1826	FCMD	FERASE	FCMD[6:0]						
\$1827-3F	Reserved								

Note: Reserved bits shown as 0 must always be written to 0.

Reserved bits shown as 1 must always be written to 1.

Shaded bits are recommended to only be controlled by firmware or factory test.

4.5 MCU Parameter Registers

The 64 bytes of parameter registers are located at addresses \$0050 through \$008F. These registers are powered up at all times and may be used to store temporary or history data during the times that the MCU is in any of the STOP modes. The parameter register at \$008F is used by the firmware for interrupt flags.

4.6 MCU RAM

The FXTH870x6 includes static RAM. The locations in RAM below \$0100 can be accessed using the more efficient direct addressing mode, and any single bit in this area can be accessed with the bit-manipulation instructions (BCLR, BSET, BRCLR, and BRSET). Locating the most frequently accessed program variables in this area of RAM is preferred.

The RAM retains data when the MCU is in low-power WAIT, STOP3 or STOP4 modes. At power-on or after wakeup from STOP1, the contents of RAM are not initialized. RAM data is unaffected by any reset provided that the supply voltage does not drop below the minimum value for RAM retention (VRAM).

When security is enabled, the RAM is considered a secure memory resource and is not accessible through BDM or through code executing from non-secure memory. See [Section 4.8](#) for a detailed description of the security feature.

None of the RAM locations are used directly by the firmware provided by Freescale. The firmware routines utilize RAM only through stack operations; and the user needs to be aware of stack depth required by each routine as described in the CodeWarrior project files supplied by Freescale.

4.7 FLASH

The FLASH memory is intended primarily for program storage. The operating program can be loaded into the FLASH memory after final assembly of the application product using the single-wire BACKGROUND DEBUG interface. Because no special voltages are needed for FLASH erase and programming operations, in-application programming is also possible through other software-controlled communication paths. For a more detailed discussion of in-circuit and in-application programming, refer to the *HCS08 Family Reference Manual, Volume I*, Freescale document order number HCS08RMV1/D.

4.7.1 Features

Features of the FLASH memory include:

- User Program FLASH Size — 8192 bytes (16 pages of 512 bytes each)
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 100,000 program/erase cycles at typical voltage and temperature
- Flexible block protection
- Security feature for FLASH and RAM
- Auto power-down for low-frequency read accesses

4.7.2 Program and Erase Times

Before any program or erase command can be accepted, the FLASH clock divider register (FCDIV) must be written to set the internal clock for the FLASH module to a frequency (f_{FCLK}) between 150 kHz and 200 kHz. This register can be written only once, so normally this write is performed during reset initialization. FCDIV cannot be written if the access error flag, FACCERR in FSTAT, is set. The user must ensure that FACCERR is not set before writing to the FCDIV register. One period of the resulting clock ($1/f_{FCLK}$) is used by the command processor to time program and erase pulses. An integer number of these timing pulses are used by the command processor to complete a program or erase command.

Table 9 shows program and erase times. The bus clock frequency and FCDIV determine the frequency of FCLK (f_{FCLK}). The time for one cycle of FCLK is $t_{FCLK} = 1/f_{FCLK}$. The times are shown as a number of cycles of FCLK and as an absolute time for the case where $t_{FCLK} = 5 \mu s$. Program and erase times shown include overhead for the command state machine and enabling and disabling of program and erase voltages.

Table 9. Program and Erase Times

Parameter	Cycles of FCLK	Time if FCLK = 200 kHz
Byte program	9	45 μs
Byte program (burst)	4	20 $\mu s^{(1)}$
Page erase	4000	20 ms
Mass erase	20,000	100 ms

1. Excluding start/end overhead

4.7.3 Program and Erase Command Execution

The steps for executing any of the commands are listed below. The FCDIV register must be initialized and any error flags cleared before beginning command execution. The command execution steps are:

1. Write a data value to an address in the FLASH array. The address and data information from this write is latched into the FLASH interface. This write is a required first step in any command sequence. For erase and blank check commands, the value of the data is not important. For page erase commands, the address may be any address in the 512-byte page of FLASH to be erased. For mass erase and blank check commands, the address can be any address in the FLASH memory. Whole pages of 512 bytes are the smallest block of FLASH that may be erased. Do not program any byte in the FLASH more than once after a successful erase operation. Reprogramming bits to a byte which is already programmed is not allowed without first erasing the page in which the byte resides or mass erasing the entire FLASH memory. Programming without first erasing may disturb data stored in the FLASH.

2. Write the command code for the desired command to FCMD. The five valid commands are blank check (0x05), byte program (0x20), burst program (0x25), page erase (0x40), and mass erase (0x41). The command code is latched into the command buffer.
3. Write a 1 to the FCBEF bit in FSTAT to clear FCBEF and launch the command (including its address and data information).

A partial command sequence can be aborted manually by writing a 0 to FCBEF any time after the write to the memory array and before writing the 1 that clears FCBEF and launches the complete command. Aborting a command in this way sets the FACCERR access error flag which must be cleared before starting a new command.

A strictly monitored procedure must be obeyed or the command will not be accepted. This minimizes the possibility of any unintended changes to the FLASH memory contents. The command complete flag (FCCF) indicates when a command is complete. The command sequence must be completed by clearing FCBEF to launch the command. [Figure 9](#) is a flowchart for executing all of the commands except for burst programming. The FCDIV register must be initialized before using any FLASH commands. This must be done only once following a reset.

4.7.4 Burst Program Execution

The burst program command is used to program sequential bytes of data in less time than would be required using the standard program command. This is possible because the high voltage to the FLASH array does not need to be disabled between program operations. Ordinarily, when a program or erase command is issued, an internal charge pump associated with the FLASH memory must be enabled to supply high voltage to the array. Upon completion of the command, the charge pump is turned off. When a burst program command is issued, the charge pump is enabled and then remains enabled after completion of the burst program operation if these two conditions are met:

- The next burst program command has been queued before the current program operation has completed.
- The next sequential address selects a byte on the same physical row as the current byte being programmed. A row of FLASH memory consists of 64 bytes. A byte within a row is selected by addresses A5 through A0. A new row begins when addresses A5 through A0 are all zero.

The first byte of a series of sequential bytes being programmed in burst mode will take the same amount of time to program as a byte programmed in standard mode. Subsequent bytes will program in the burst program time provided that the conditions above are met. In the case the next sequential address is the beginning of a new row, the program time for that byte will be the standard time instead of the burst time. This is because the high voltage to the array must be disabled and then enabled again. If a new burst command has not been queued before the current command completes, then the charge pump will be disabled and high voltage removed from the array.

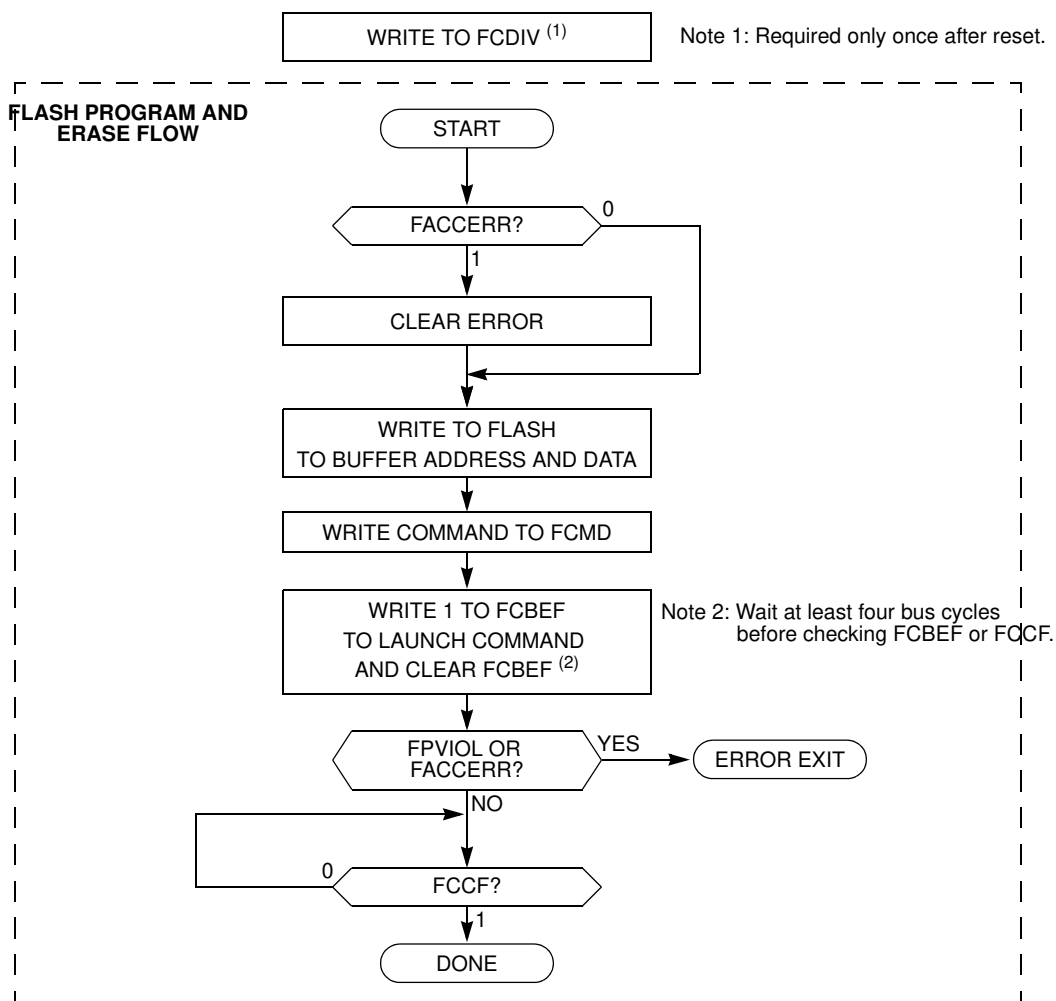


Figure 9. FLASH Program and Erase Flowchart

Programming time for the FLASH through the BDM function is dependent on the specific external BDM interface tool and software being used. Consult tool vendor for programming times.