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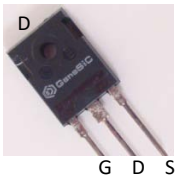
Silicon Carbide Junction Transistor/Schottky Diode Co-Pack

V_{DS}	=	1200 V
$R_{DS(ON)}$	=	50 mΩ
$I_{D\ (@\ 25°C)}$	=	45 A
$I_{D\ (@\ 145°C)}$	=	20 A
$h_{FE\ (@\ 25°C)}$	=	100

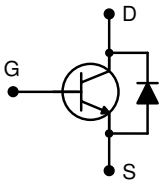
Features

- 175 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Integrated SiC Schottky Rectifier
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Package



TO-247AB



Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 µs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth
- Reduced cooling requirements
- Reduced system size

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Table of Contents

Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
SiC Junction Transistor					
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	1200	V	
Continuous Drain Current	I_D	T_C = 25°C	45	A	Fig. 11
Continuous Drain Current	I_D	T_C = 145°C	20	A	Fig. 11
Continuous Gate Current	I_G		1.3	A	
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 175 °C, Clamped Inductive Load	$I_{D,max}$ = 20 @ $V_{DS} \leq V_{DSmax}$	A	Fig. 13
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 175 °C, I_G = 1 A, V_{DS} = 800 V, Non Repetitive	>20	µs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Power Dissipation	P_{tot}	T_C = 25 °C / 145 °C, t_p > 100 ms	282 / 56	W	Fig. 10
Operating and storage temperature	T_{stg}		-55 to 175	°C	

Parameter	Symbol	Conditions	Value	Unit	Notes
Free-Wheeling SiC Diode					
Repetitive peak reverse voltage	V_{RRM}		1200	V	
Continuous forward current	I_F	$T_C \leq 150$ °C	10	A	
RMS forward current	$I_{F(RMS)}$	$T_C \leq 150$ °C	17	A	
Surge non-repetitive forward current, Half Sine Wave	I_{FSM}	T_C = 25 °C, t_P = 10 ms T_C = 150 °C, t_P = 10 ms	65 55	A	
Non-repetitive peak forward current	$I_{F,max}$	T_C = 25 °C, t_P = 10 µs	280	A	
I^2t value	$\int i^2\,dt$	T_C = 25 °C, t_P = 10 ms T_C = 115 °C, t_P = 10 ms	21 15	A^2s	

Thermal Characteristics					
Thermal resistance, junction - case	R_{thJC}	SiC Junction Transistor	0.53	°C/W	
Thermal resistance, junction - case	R_{thJC}	SiC Diode	0.8	°C/W	

Section II: Static Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
A: On State							
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 20 A, T_j = 25 °C I_D = 20 A, T_j = 150 °C I_D = 20 A, T_j = 175 °C		50 93 109		mΩ	Fig. 4
Gate – Source Saturation Voltage	$V_{GS,SAT}$	I_D = 20 A, I_D/I_G = 40, T_j = 25 °C I_D = 20 A, I_D/I_G = 30, T_j = 175 °C		3.44 3.24		V	Fig. 7
DC Current Gain	h_{FE}	V_{DS} = 8 V, I_D = 20 A, T_j = 25 °C V_{DS} = 8 V, I_D = 20 A, T_j = 125 °C V_{DS} = 8 V, I_D = 20 A, T_j = 175 °C		100 62 56		–	Fig. 5
FWD forward voltage	V_F	I_F = 10 A, T_j = 25 °C I_F = 10 A, T_j = 175 °C		1.5 2.6	1.8 3.0	V	
B: Off State							
Drain Leakage Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 25 °C V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 125 °C V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 175 °C		5 8 10	25 40 50	µA	Fig. 8
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA	

Section III: Dynamic Electrical Characteristics

Parameter	Symbol	Conditions		Value			Unit	Notes
				Min.	Typical	Max.		
A: Capacitance and Gate Charge								
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 800 V, f = 1 MHz			3091		pF	Fig. 9
Reverse Transfer Capacitance	C_{rss}	V_{DS} = 800 V, f = 1 MHz			53		pF	Fig. 9
Total FWD capacitance	C_{FWD}	V_R = 1 V, f = 1 MHz, T_j = 25 °C V_R = 400 V, f = 1 MHz, T_j = 25 °C V_R = 1000 V, f = 1 MHz, T_j = 25 °C			490 45 33		pF	
Gate-Source Charge	Q_{GS}	V_{GS} = -5…3 V			23		nC	
Gate-Drain Charge	Q_{GD}	V_{GS} = 0 V, V_{DS} = 0…800 V			77		nC	
Gate Charge - Total	Q_G				100		nC	
Total FWD capacitive charge	$Q_{C,FWD}$	$I_F \leq I_{F,MAX}$ dI_F/dt = 200 A/µs T_j = 175 °C	V_R = 400 V V_R = 960 V		31 52		nC	

B: Switching[1]

Internal Gate Resistance – zero bias	$R_{G(INT-ZERO)}$	f = 1 MHz, V_{AC} = 50 mV, V_{DS} = 0 V, V_{GS} = 0 V, T_j = 175 ºC	1.7	Ω
Internal Gate Resistance – ON	$R_{G(INT-ON)}$	V_{GS} > 2.5 V, V_{DS} = 0 V, T_j = 175 ºC	0.13	Ω
Turn On Delay Time	$t_{d(on)}$	T_j = 25 ºC, V_{DS} = 800 V, I_D = 20 A, Resistive Load Refer to Section V for additional driving information.	12	ns
Fall Time, V_{DS}	t_f		14	ns
Turn Off Delay Time	$t_{d(off)}$		24	ns
Rise Time, V_{DS}	t_r		12	ns
Turn On Delay Time	$t_{d(on)}$	T_j = 175 ºC, V_{DS} = 800 V, I_D = 20 A, Resistive Load	15	ns
Fall Time, V_{DS}	t_f		13	ns
Turn Off Delay Time	$t_{d(off)}$		30	ns
Rise Time, V_{DS}	t_r		10	ns
Turn-On Energy Per Pulse	E_{on}	T_j = 25 ºC, V_{DS} = 800 V, I_D = 20 A, Inductive Load Refer to Section V.	316	µJ
Turn-Off Energy Per Pulse	E_{off}		40	µJ
Total Switching Energy	E_{tot}		356	µJ
Turn-On Energy Per Pulse	E_{on}	T_j = 175 ºC, V_{DS} = 800 V, I_D = 20 A, Inductive Load	298	µJ
Turn-Off Energy Per Pulse	E_{off}		28	µJ
Total Switching Energy	E_{tot}		326	µJ

[1] – All times are relative to the Drain-Source Voltage V_{DS}

Section IV: Figures

A: Static Characteristics

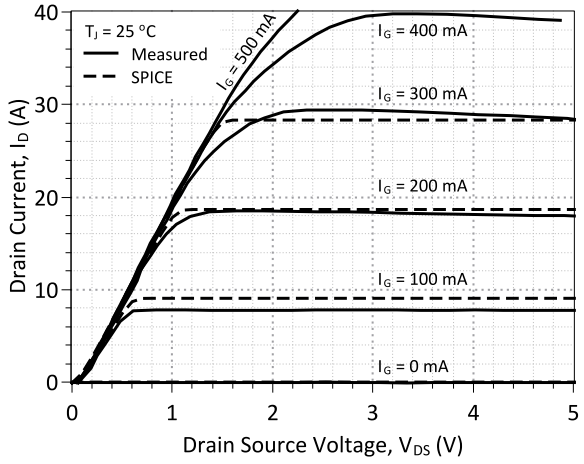


Figure 1: Typical Output Characteristics at 25 °C

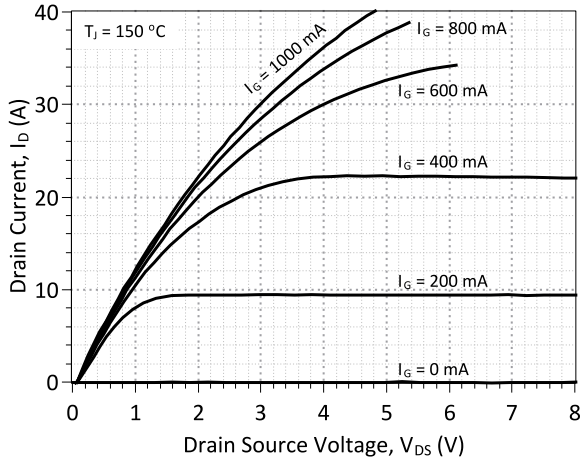


Figure 2: Typical Output Characteristics at 150 °C

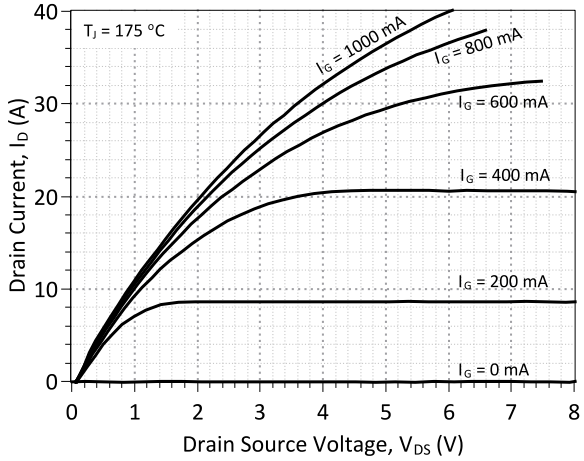


Figure 3: Typical Output Characteristics at 175 °C

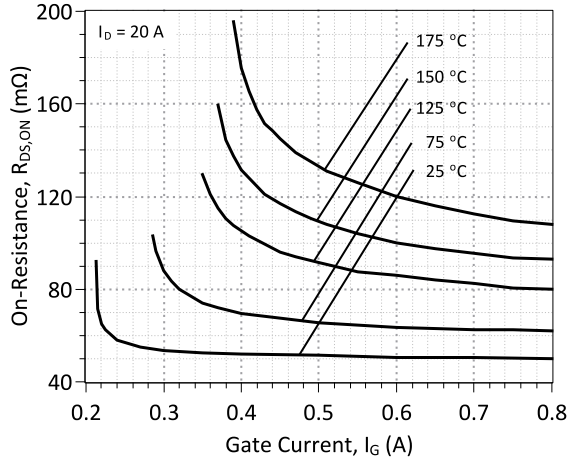


Figure 4: On-Resistance vs. Gate Current

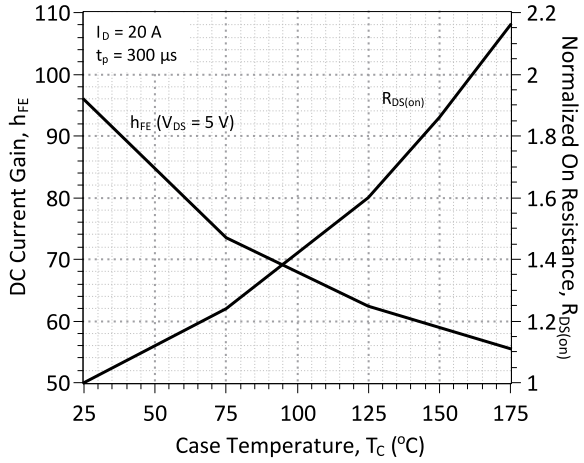


Figure 5: DC Current Gain and Normalized On-Resistance vs. Temperature

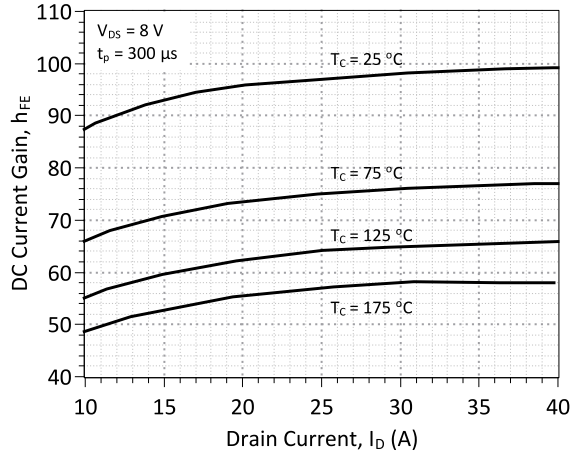


Figure 6: DC Current Gain vs. Drain Current

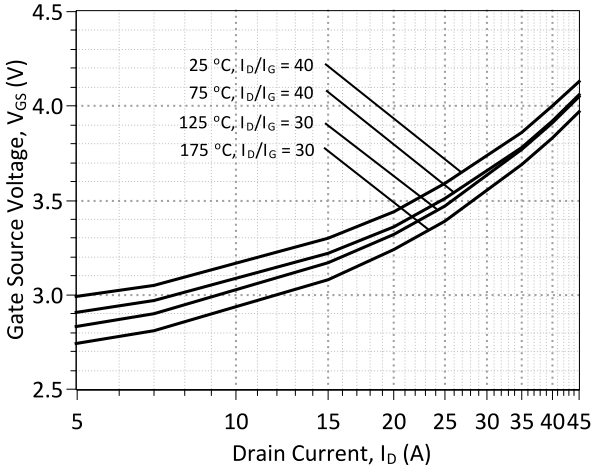


Figure 7: Typical Gate – Source Saturation Voltage

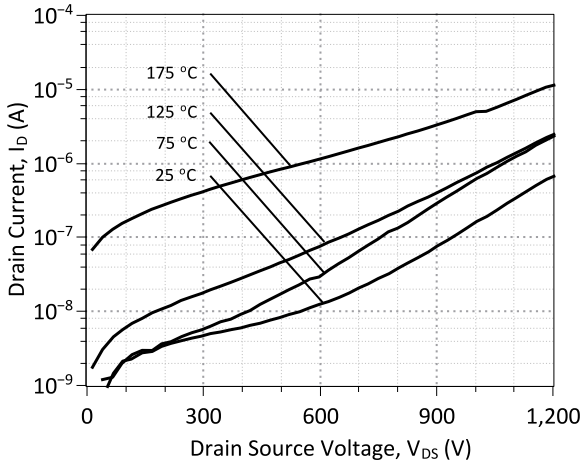


Figure 8: Typical Blocking Characteristics

B: Dynamic Characteristics

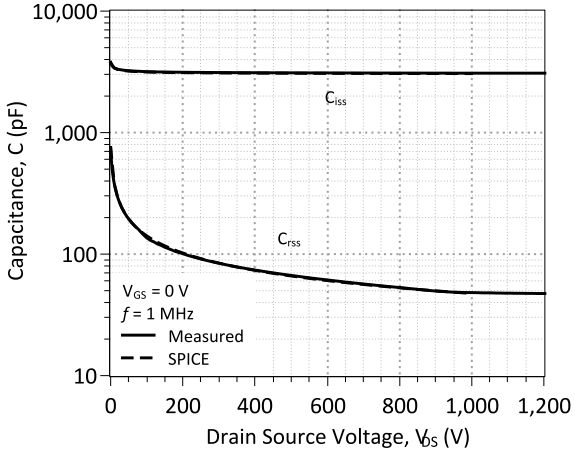


Figure 9: Input and Reverse Transfer Capacitance

C: Current and Power Derating

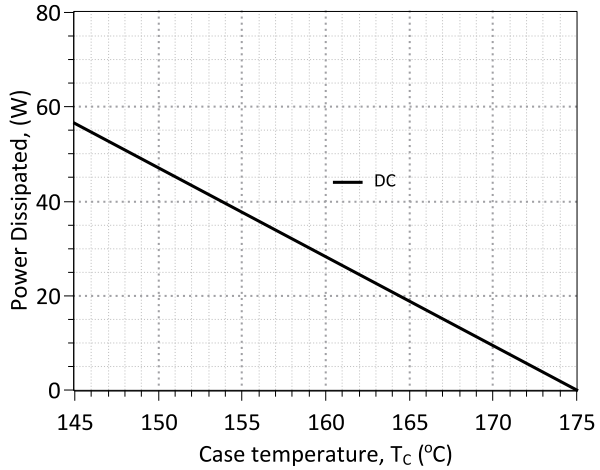


Figure 10: Power Derating Curve

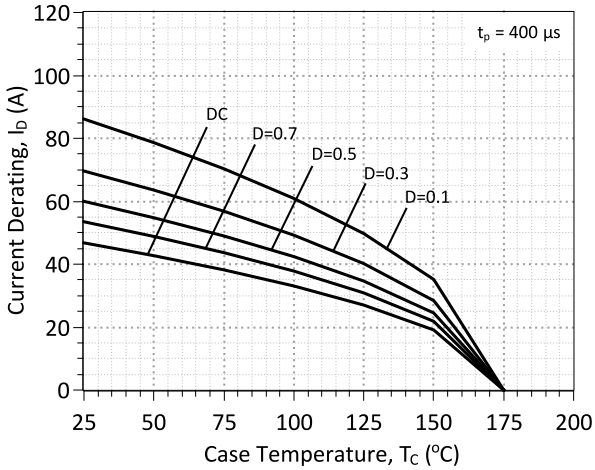


Figure 11: Drain Current Derating vs. Temperature

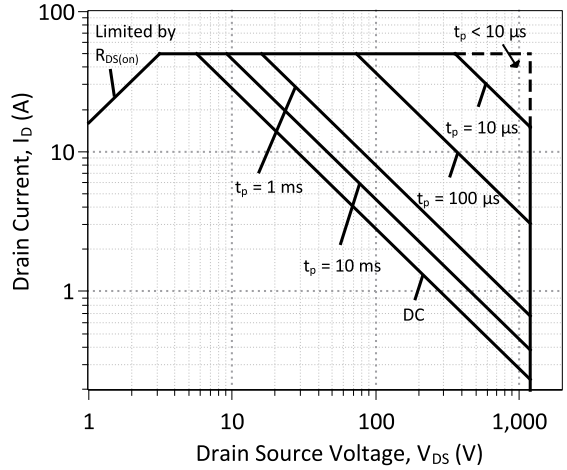


Figure 12: Forward Bias Safe Operating Area at T_c= 25 °C

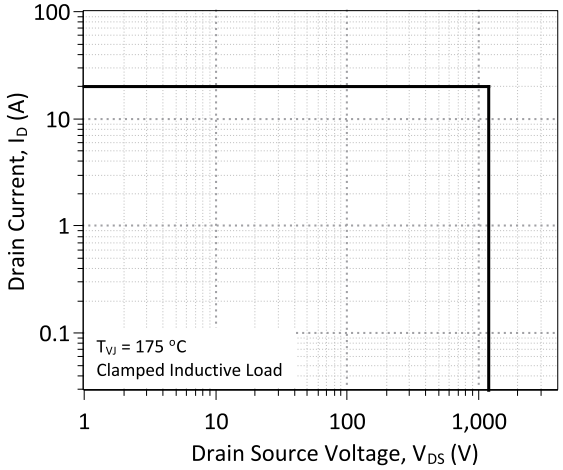


Figure 13: Turn-Off Safe Operating Area

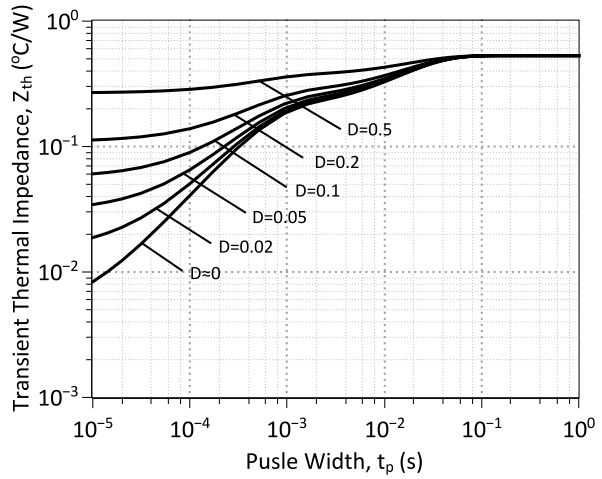


Figure 14: SJT Transient Thermal Impedance

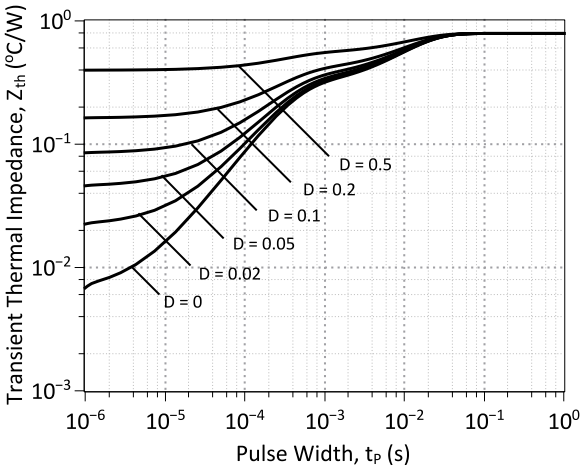


Figure 15: FWD Transient Thermal Impedance

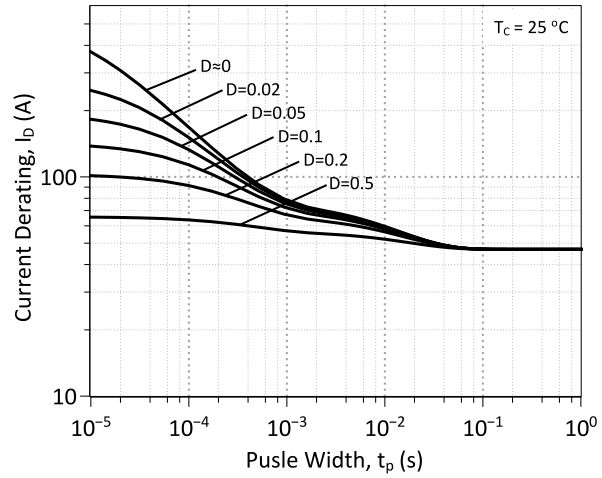


Figure 16: Drain Current Derating vs. Pulse Width

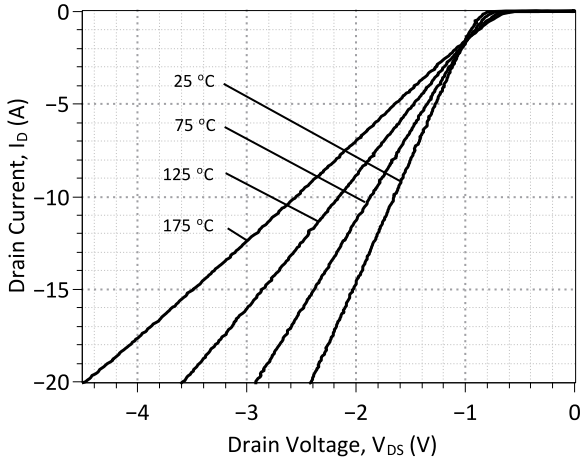


Figure 17: Typical FWD Forward Characteristics

Section V: Driving the GA20SICP12-247

Drive Topology	Gate Drive Power Consumption	Switching Frequency	Application Emphasis	Availability
TTL Logic	High	Low	Wide Temperature Range	Coming Soon
Constant Current	Medium	Medium	Wide Temperature Range	Coming Soon
High Speed – Boost Capacitor	Medium	High	Fast Switching	Production
High Speed – Boost Inductor	Low	High	Ultra Fast Switching	Coming Soon
Proportional	Lowest	High	Wide Drain Current Range	Coming Soon
Pulsed Power	Medium	N/A	Pulse Power	Coming Soon

A: Static TTL Logic Driving

The GA20SICP12-247 may be driven using direct (5 V) TTL logic after current amplification. The (amplified) current level of the supply must meet or exceed the steady state gate current ($I_{G,steady}$) required to operate the GA20SICP12-247. The power level of the supply can be estimated from the target duty cycle of the particular application. $I_{G,steady}$ is dependent on the anticipated drain current I_D through the SJT and the DC current gain h_{FE}, it may be calculated from the following equation. An accurate value of the h_{FE} may be read from Figure 6.

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

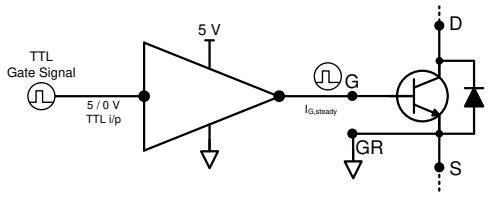


Figure 18: TTL Gate Drive Schematic

B: High Speed Driving

The SJT is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 19 which features a positive current peak during turn-on, a negative current peak during turn-off, and continuous gate current to remain on.

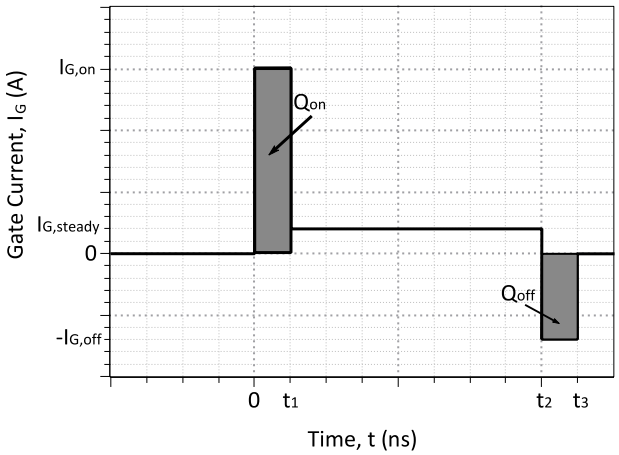


Figure 19: An idealized gate current waveform for fast switching of an SJT.

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$Q_{on} = I_{G,on} * t_1$$

$$Q_{on} \geq Q_{gs} + Q_{gd}$$

Ideally, $I_{G,on}$ should terminate when the drain voltage falls to its on-state value in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the device package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The voltage applied to the gate pin should be maintained high enough, above the $V_{GS,sat}$ (see Figure 7) level to counter these effects.

A high negative peak current, $-I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with V_{GS} = 0 V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

Two high-speed drive topologies for the SiC SJTs are presented below.

B:1: High Speed, Low Loss Drive with Boost Capacitor, GA03IDDJT30-FR4

The GA20SICP12-247 may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide fast switching current peaks at turn-on and turn-off and a continuous gate current while in on-state. A 3 kV isolated evaluation gate drive board (GA03IDDJT30-FR4) utilizing this topology is commercially available for high and low-side driving, its datasheet provides additional details about this drive topology.

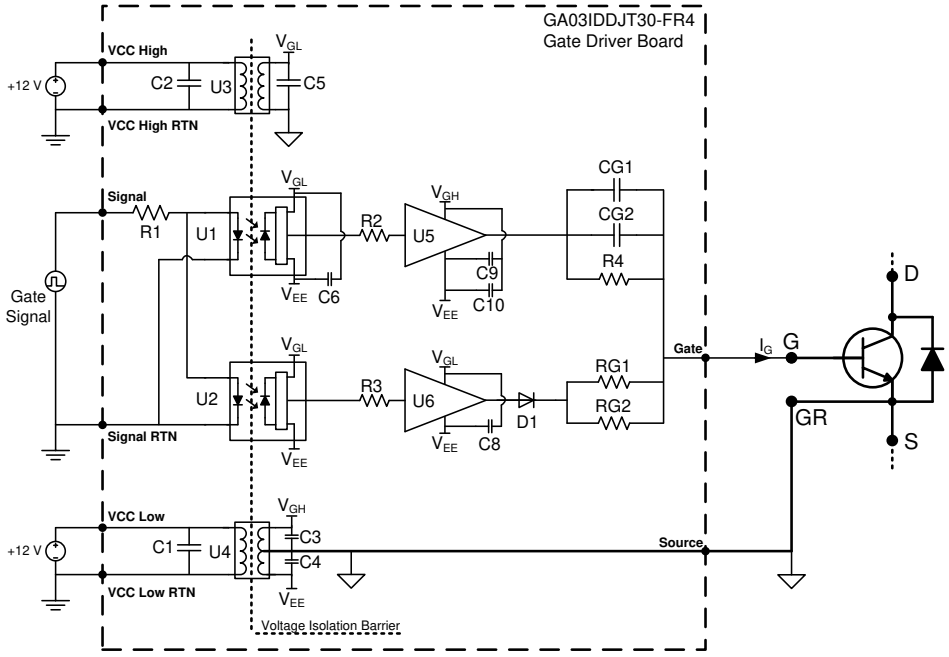


Figure 20: Topology of the GA03IDDJT30-FR4 Two Voltage Source gate driver.

The GA03IDDJT30-FR4 evaluation board comes equipped with two on board gate drive resistors (RG1, RG2) pre-installed for an effective gate resistance[3] of R_G = 3.75 Ω. It may be necessary for the user to reduce RG1 and RG2 under high drain current conditions for safe operation of the GA20SICP12-247. The steady state current supplied to the gate pin of the GA20SICP12-247 with on-board R_G = 3.75 Ω, is shown in Figure 21. The maximum allowable safe value of R_G for the user's required drain current can be read from Figure 22.

For the GA20SICP12-247, R_G must be reduced for I_D ≥ ~14 A for safe operation with the GA03IDDJT30-FR4.

For operation at I_D ≥ ~14 A, R_G may be calculated from the following equation, which contains the DC current gain h_{FE} (Figure 6) and the gate-source saturation voltage $V_{GS,sat}$ (Figure 7).

$$R_{G,max} = \frac{(4.7V - V_{GS,sat}) * h_{FE}(T, I_D)}{I_D * 1.5} - 0.6\Omega$$

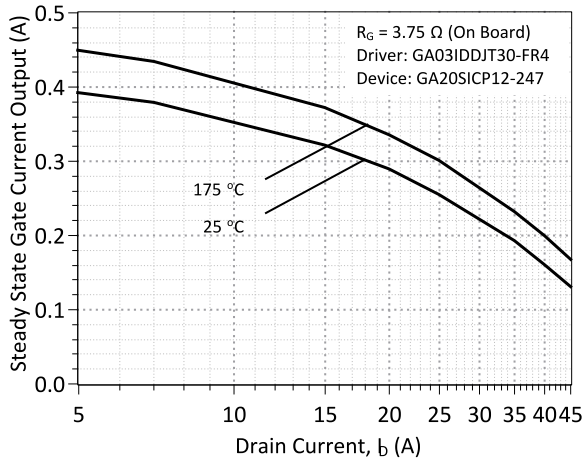


Figure 21: Typical steady state gate current supplied by the GA03IDDJT30-FR4 board for the GA20SICP12-247 with the on board resistance of 3.75 Ω

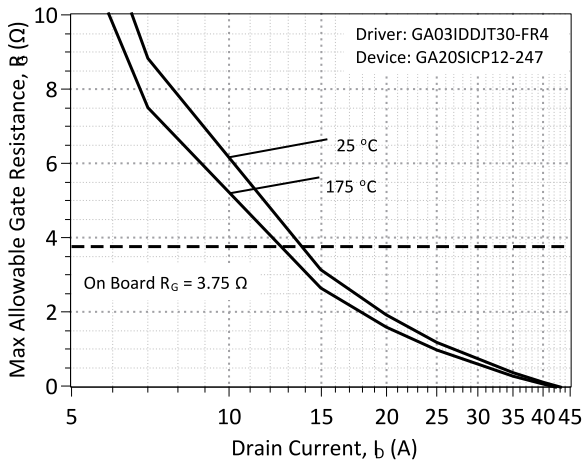


Figure 22: Maximum gate resistance for safe operation of the GA20SICP12-247 at different drain currents using the GA03IDDJT30-FR4 board.

B:2: High Speed, Low Loss Drive with Boost Inductor

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the GA20SICP12-247 at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses $I_{G,on}$ and $I_{G,off}$. During operation, inductor L is charged to a specified $I_{G,on}$ current value then made to discharge I_L into the SJT gate pin using logic control of S_1, S_2, S_3, and S_4, as shown in Figure 23. After turn on, while the device remains on the necessary steady state gate current $I_{G,steady}$ is supplied from source V_{CC} through R_G. Please refer to the article "A current-source concept for fast and efficient driving of silicon carbide transistors" by Dr. Jacek Rąbkowski for additional information on this driving topology.[4]

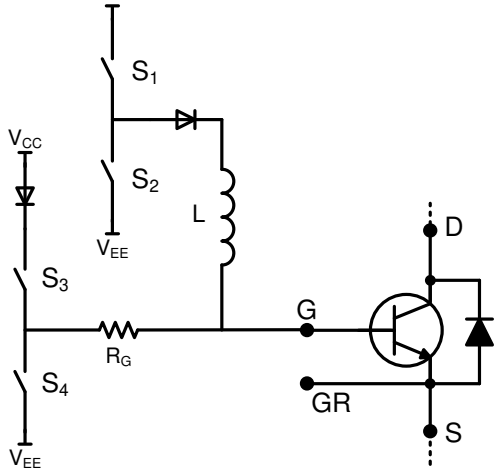


Figure 23: Simplified Inductive Pulsed Drive Topology

[3] – $R_G = (1/RG1 + 1/RG2)^{-1}$. Driver is pre-installed with RG1 = RG2 = 7.5 Ω

[4] – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/aee-2013-0026, June 2013

C: Proportional Gate Current Driving

For applications in which the GA20SICP12-247 will operate over a wide range of drain current conditions, it may be beneficial to drive the device using a proportional gate drive topology to optimize gate drive power consumption. A proportional gate driver relies on instantaneous drain current I_D feedback to vary the steady state gate current $I_{G,steady}$ supplied to the GA20SICP12-247

C:1: Voltage Controlled Proportional Driver

The voltage controlled proportional driver relies on a gate drive IC to detect the GA20SICP12-247 drain-source voltage V_{DS} during on-state to sense I_D. The gate drive IC will then increase or decrease $I_{G,steady}$ in response to I_D. This allows $I_{G,steady}$, and thus the gate drive power consumption, to be reduced while I_D is relatively low or for $I_{G,steady}$ to increase when is I_D higher. A high voltage diode connected between the drain and sense protects the IC from high-voltage when the driver and GA20SICP12-247 are in off-state. A simplified version of this topology is shown in Figure 24, additional information will be available in the future at http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/

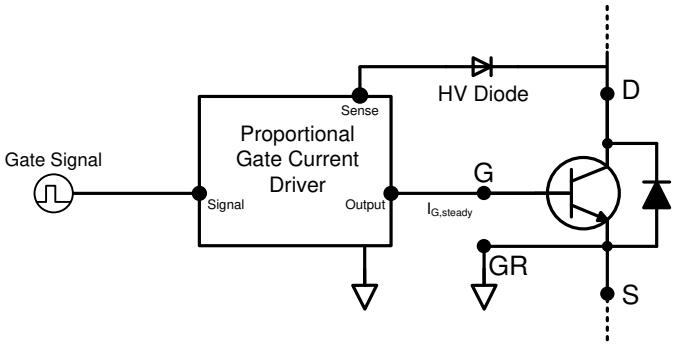


Figure 24: Simplified Voltage Controlled Proportional Driver

C:2: Current Controlled Proportional Driver

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback I_D of the GA20SICP12-247 during on-state to supply $I_{G,steady}$ into the device gate. $I_{G,steady}$ will then increase or decrease in response to I_D at a fixed forced current gain which is set be the turns ratio of the transformer, $h_{force} = I_D / I_G = N_2 / N_1$. GA20SICP12-247 is initially tuned-on using a gate current pulse supplied into an RC drive circuit to allow I_D current to begin flowing. This topology allows $I_{G,steady}$, and thus the gate drive power consumption, to be reduced while I_D is relatively low or for $I_{G,steady}$ to increase when is I_D higher. A simplified version of this topology is shown in Figure 25, additional information will be available in the future at http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/.

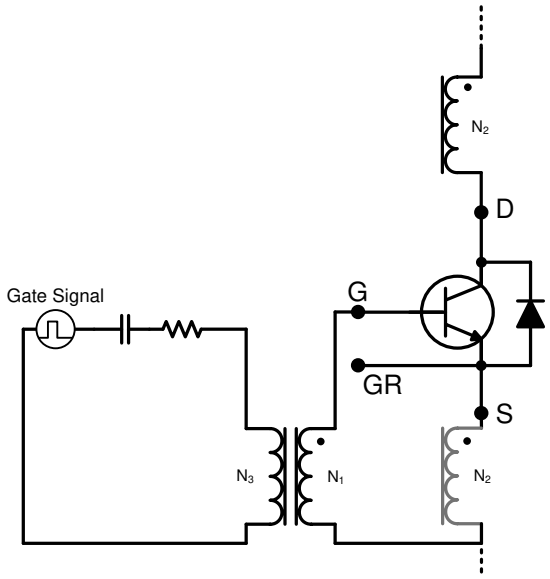
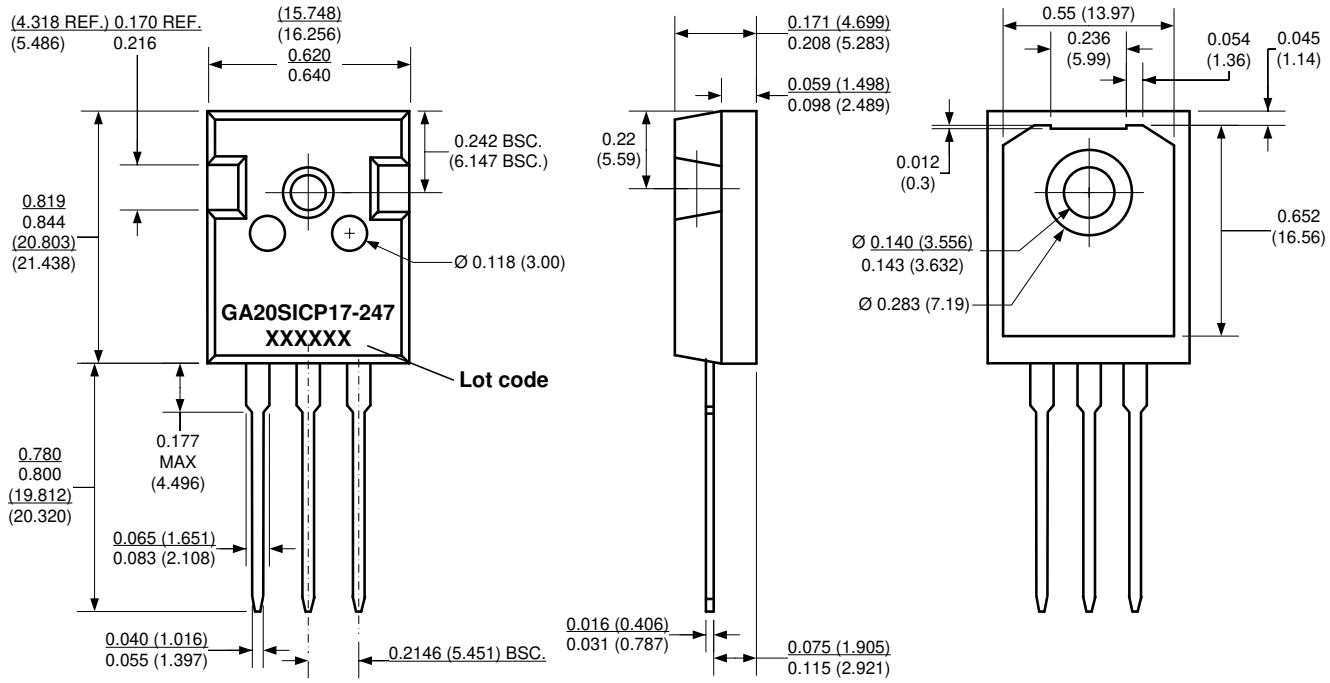


Figure 25: Simplified Current Controlled Proportional Driver

Section VI: Package Dimensions

TO-247AB **PACKAGE OUTLINE**



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2015/06/11	0	Initial release	

Published by
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Dulles, VA 20166

Section VII: SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/products_sic/igbt_copack/GA20SICP12-247_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA20SICP12-247.

```
*     MODEL OF GeneSiC Semiconductor Inc.
*     $Revision: 1.0             $
*     $Date:     29-MAY-2015     $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*
*     COPYRIGHT (C) 2015 GeneSiC Semiconductor Inc.
*     ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
* Start of GA20SICP12-247 SPICE Model
*
.SUBCKT GA20SICP12 DRAIN GATE SOURCE
Q1 DRAIN GATE SOURCE GA20SICP12_Q
D1 SOURCE DRAIN GA20SICP12_D1
D2 SOURCE DRAIN GA20SICP12_D2
*
.model GA20SICP12_Q NPN
+ IS       9.833E-48       ISE        1.073E-26       EG         3.23
+ BF       100             BR         0.55            IKF        9000
+ NF       1               NE         2               RB         3.09
+ RE       0.005           RC         0.040           CJC        752E-12
+ VJC      3.17            MJC        0.48            CJE        3.01E-09
+ VJE      3.568           MJE        0.538           XTI        3
+ XTB      -1.5            TRC1       8.50E-03        MFG   GeneSiC_Semi
+ IRB      0.006           RBM        0.101
.MODEL GA20SICP12_D1 D
+ IS       5.48E-17        RS         0.03214547      N          1
+ IKF      1000            EG         1.2             XTI        3
+ CJO      1.15E-09        VJ         0.44            M          1.5
+ FC       0.5             TT         1.00E-10        IBV        1.00E-03
.MODEL GA20SICP12_D2 D
+ IS       1.54E-13        RS         0.23            N          3.941
+ IKF      19              EG         3.23            XTI        0
+ FC       0.5             TT         0               IBV        1.00E-03
.ENDS
* End of GA20SICP12-247 SPICE Model
```