Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Never stop thinking

n-Channel Power MOSFET

OptiMOS™
BSF134N10NJ3 G

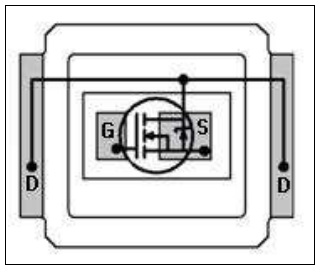
Data Sheet

2.5, 2011-05-31
Final

Industrial & Multimarket

1 Description

OptiMOS™100V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 100V the best choice for the demanding requirements of voltage regulator solutions in Solar, Drives, Datacom and Telecom applications. Super fast switching Control FETs together with low EMI Sync FETs provide solutions that are easy to design in. OptiMOS™ products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space, efficiency and cost.



Features

- Optimized for high switching frequency DC/DC converter
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Qualified according to JEDEC[1)] for target applications
- Superior thermal resistance
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Double.sided cooling
- Compatible with DirectFET® package MN footprint and outline
- Low profile (<0.7mm)
- Low parasitic inductance

Applications

- Synchronous rectification
- Primary side switches
- Power managment for high performance computing
- High power density point of load converters

Table 1 Key Performance Parameters

Parameter	Value	Unit		Related Links
V_{DS}	100	V		IFX OptiMOS webpage
$R_{DS(on),max}$	13.4	mΩ		IFX OptiMOS product brief
I_D	40	A		IFX OptiMOS spice models
Q_{OSS}	32	nC		IFX Design tools
$Q_{g\cdot typ}$	23			

Type	Package	Marking
BSF134N10NJ3 G	MG-WDSON-2	0210

1) J-STD20 and JESD22

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	40	A	V_{GS}=10 V, T_C=25 °C
				25		V_{GS}=10 V, T_C=100 °C
				9		V_{GS}=10 V, T_A=25 °C, R_{thJA}=45 K/W[1])
Pulsed drain current[2]	$I_{D,pulse}$	-	-	160		T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	70	mJ	I_D=30 A,R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	
Power dissipation	P_{tot}	-	-	43	W	T_C=25 °C
				2.2		T_A=25 °C, R_{thJA}=58 K/W[1]
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	
IEC climatic category; DIN IEC 68-1		55/150/56				

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical in still air

2) See figure 3 for more detailed information

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.9	K/W	top
		-	1	-		bottom
Device on PCB	R_{thJA}	-	-	58		6 cm^2 cooling area[1]

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical in still air

4 Electrical characteristics

Electrical characteristics, at Tj=25 °C, unless otherwise specified.

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2	2.7	3.5		V_{DS}=V_{GS}, I_D=40 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	10	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C
		-	10	100		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	12.2	13.4	mΩ	V_{GS}=10 V, I_D=30A
			15.4	20		V_{GS}=6 V, I_D=15A
Gate resistance	R_G	-	0.5	-	Ω	
Transconductance	g_{fs}	22	44		S	|V_{DS}|>2|$I_{D\|RDS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1700	2300	pF	V_{GS}=0 V, V_{DS}=50V, f=1 MHz
Output capacitance	C_{oss}	-	320	430		
Reverse transfer capacitance	C_{rss}	-	12	-		
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	V_{DD}=50V, V_{GS}=10 V, I_D=30 A, R_G= 1.6 Ω
Rise time	t_r	-	6	-		
Turn-off delay time	$t_{d(off)}$	-	15	-		
Fall time	t_f	-	5	-		

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8	-	nC	V_{DD}=50 V, I_D=30 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	4.1	-		
Switching charge	Q_{sw}	-	9	-		
Gate charge total	Q_g	-	23	30		
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	
Output charge	Q_{oss}		32	42		V_{DD}=50 V, V_{GS}=0 V

1) See figure 16 for gate charge parameter definition

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_s			36	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			160		
Diode forward voltage	V_{SD}	-	0.9	1.2	V	V_{GS}=0 V, I_F=I_S, T_j=25 °C
Reverse recovery charge	t_{rr}	-	59	-	nC	V_R=50V, I_F=I_s, di_F/dt=100 A/µs
Reverse recovery time	Q_{rr}	-	112	-	ns	

5 Electrical characteristics diagrams

Table 8

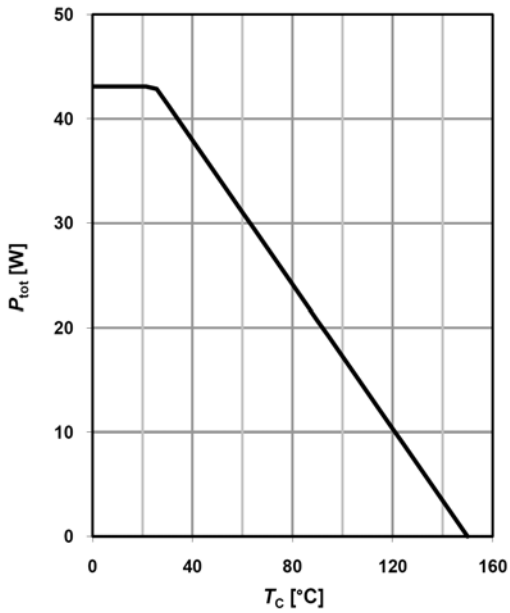
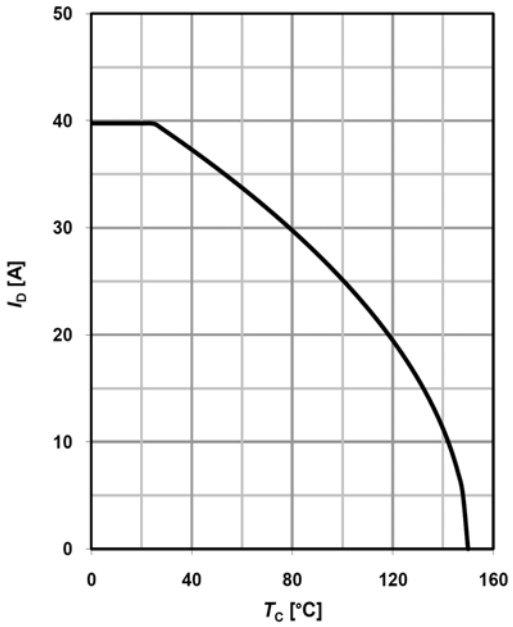
1 Power dissipation	2 Drain current
	
$P_{tot} = f(T_C)$	$I_D=f(T_C)$; parameter:V_{GS}

Table 9

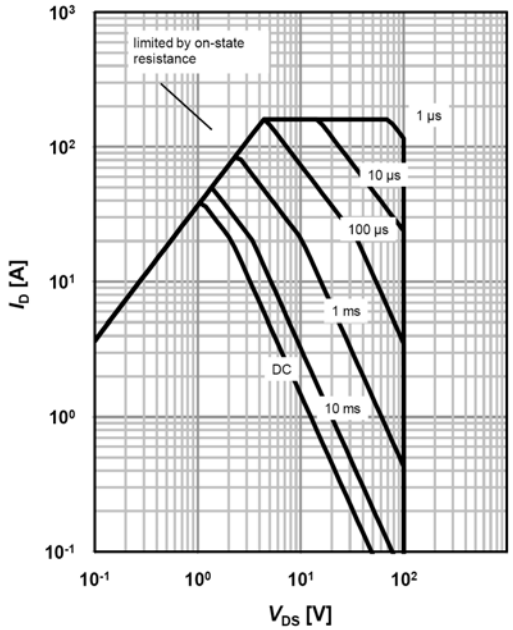
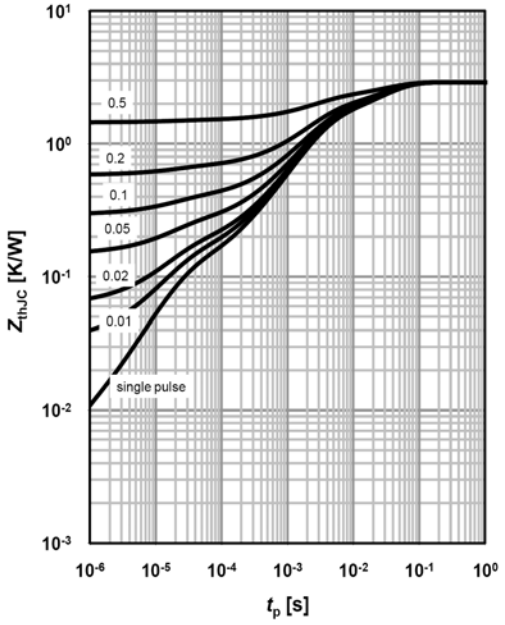
3 Safe operating area T_C=25 °C	4 Max. transient thermal impedance
	
$I_D=f(V_{DS})$; T_j=25 °C; D=0; parameter: T_p	$Z_{(thJC)}=f(t_p)$; parameter: D=t_p/T

Table 10

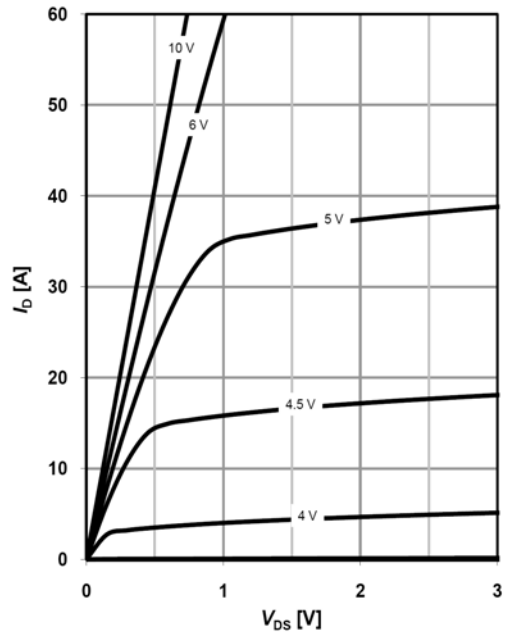
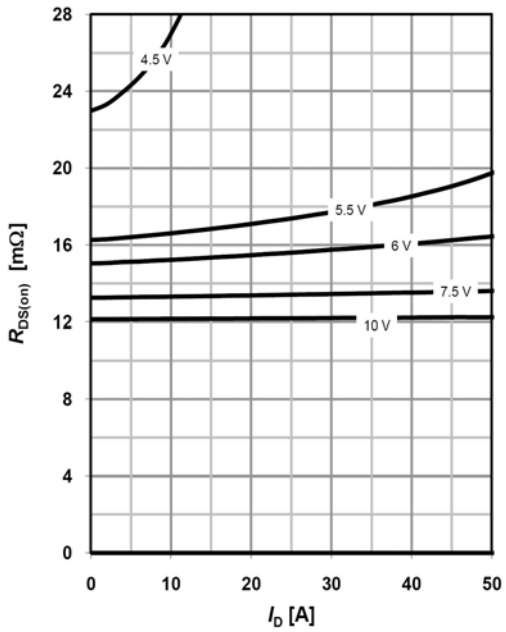
5 Typ. output characteristics T_C=25 °C	6 Typ. drain-source on-state resistance
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Table 11

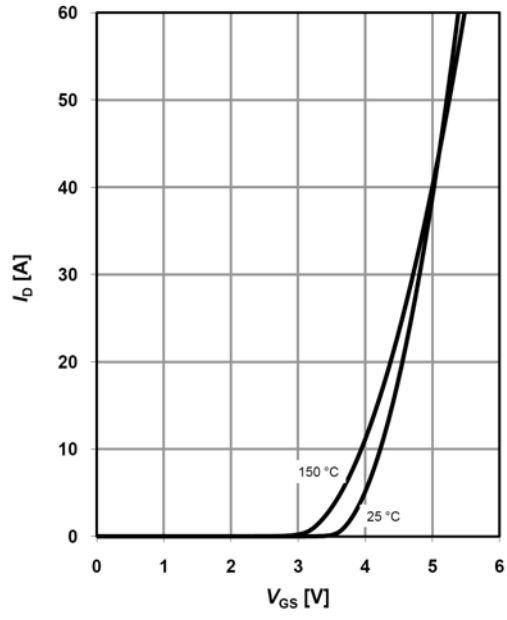
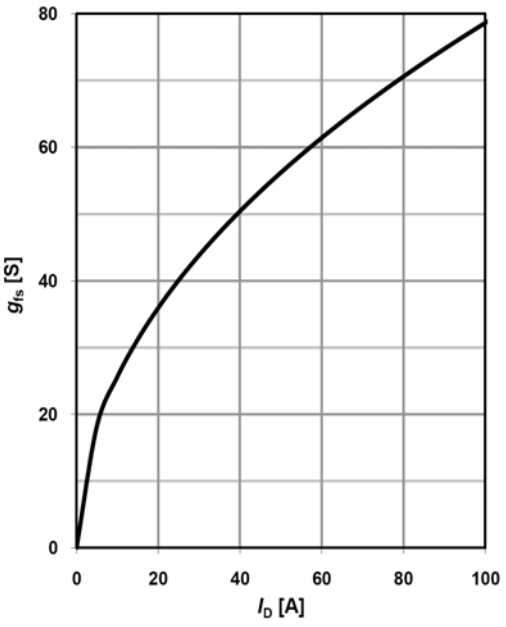
7 Typ. transfer characteristics	8 Typ. forward transconductance
	
I_D=f(VGS); |V_{DS}|>2|I_D|$R_{DS(on)max}$	g_{fs}=f(I_D); T_j=25 °C

Table 12

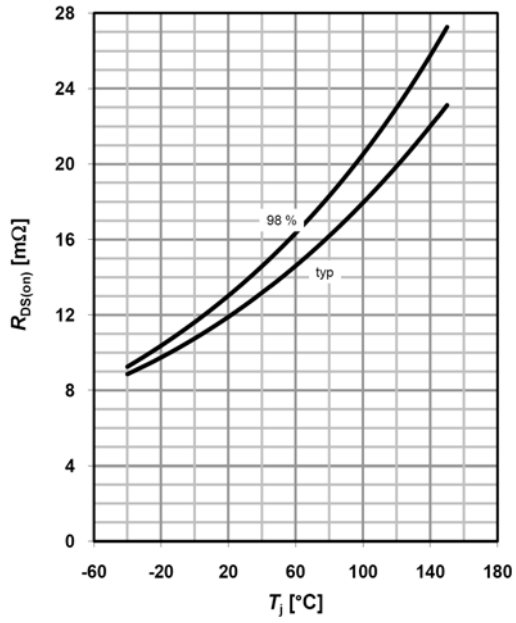
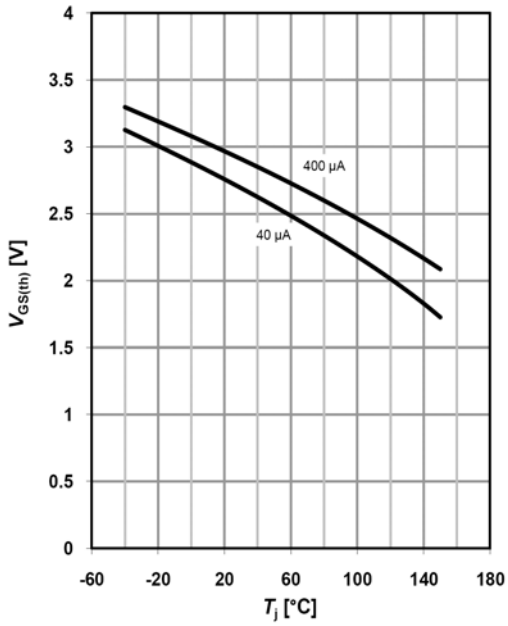
9 Drain-source on-state resistance	10 Typ. gate threshold voltage
	
$R_{DS(on)}=f(T_j)$; I_D=30 A; V_{GS}=10 V	$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Table 13

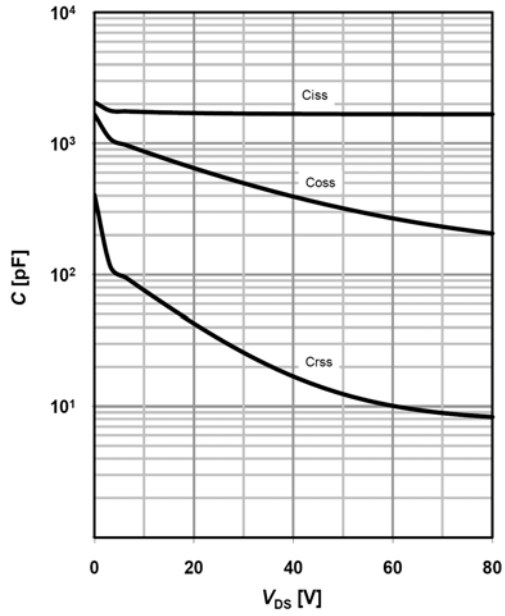
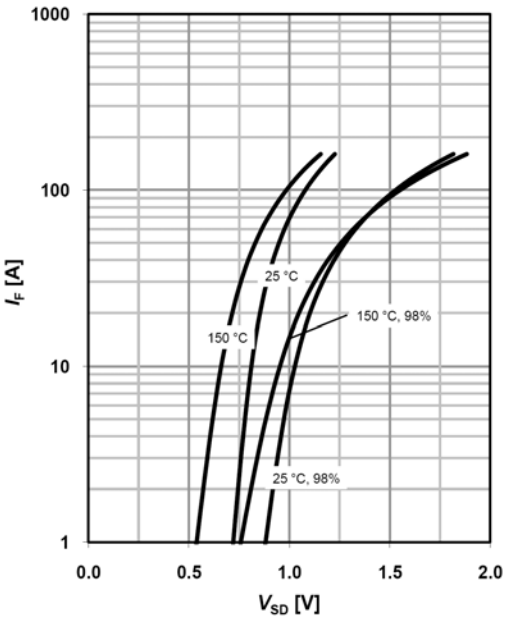
11 Typ. capacitances	12 Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	$I_F=f(V_{SD})$; parameter: T_j

Table 14

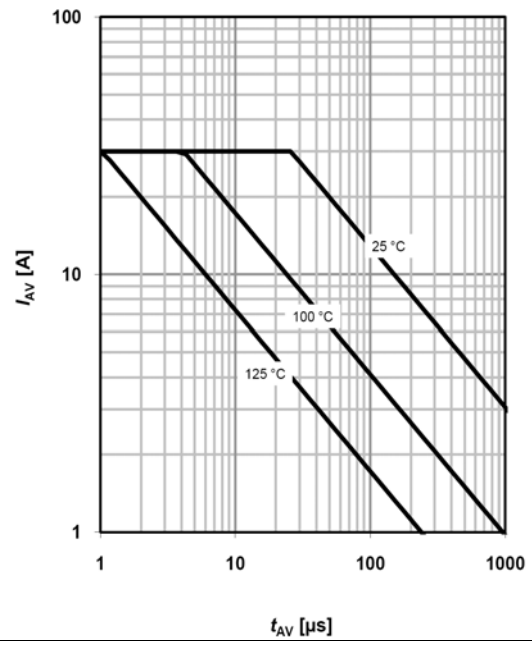
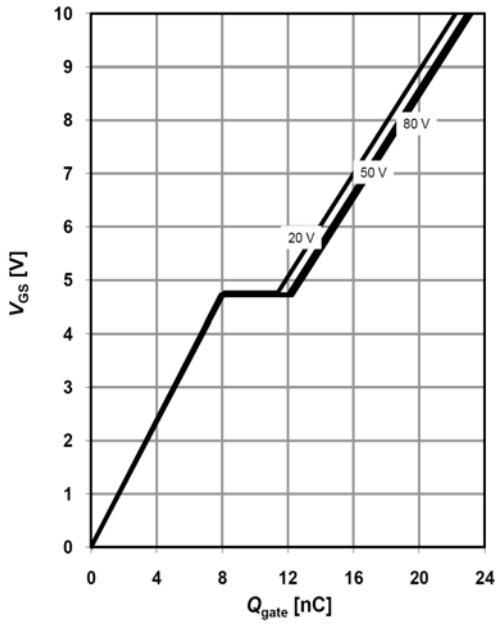
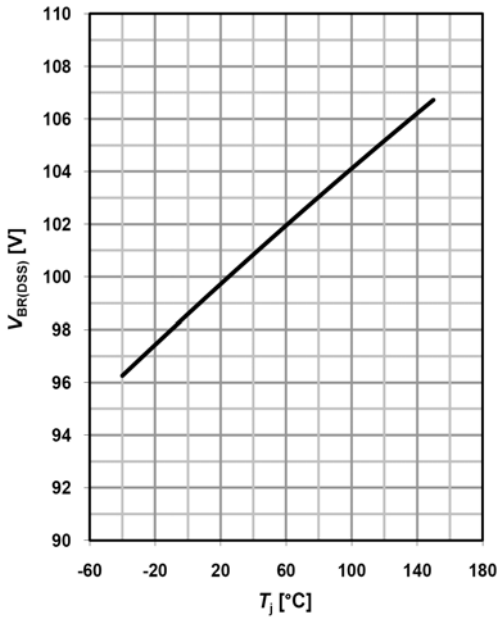
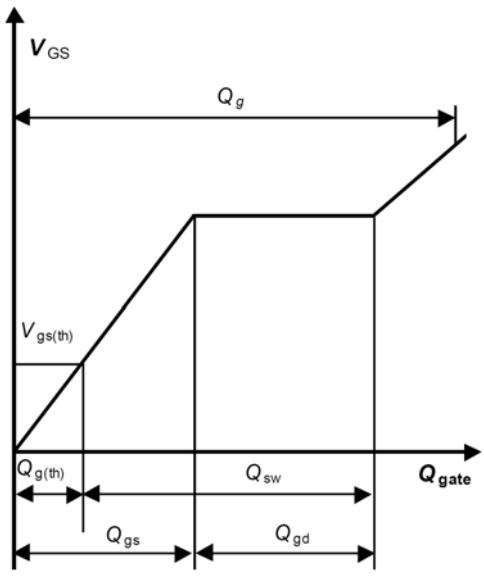
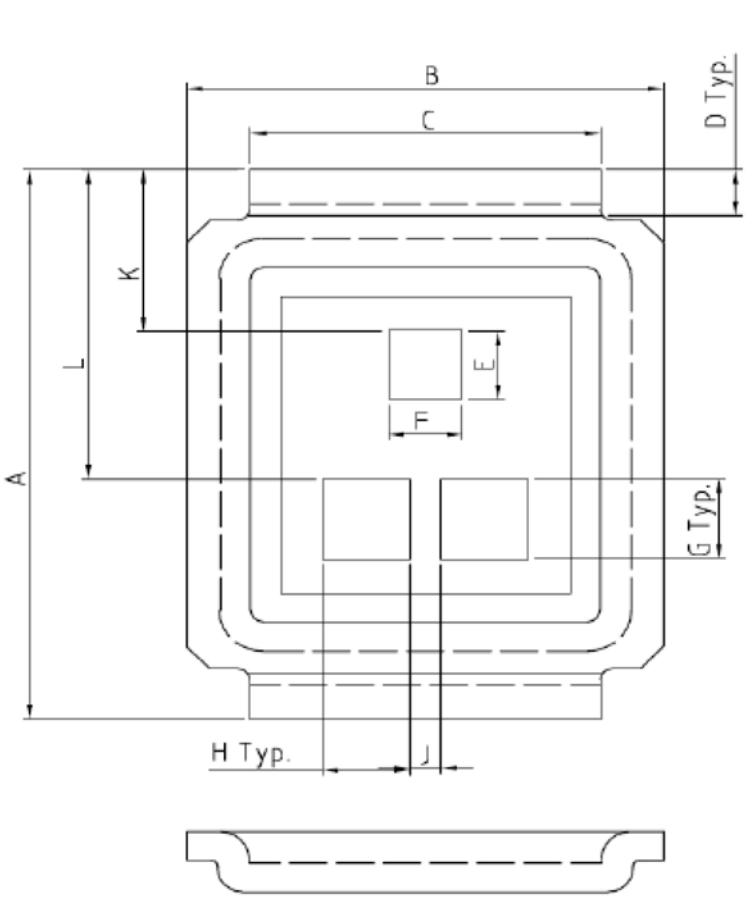
13 Avalanche characteristics	14 Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$	V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Table 15

15 Drain-source breakdown voltage	16 Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	

6 Package outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.75	4.88	0.187	0.192
B	3.70	3.95	0.146	0.156
C	2.75	2.85	0.108	0.112
D	0.35	0.45	0.014	0.018
E	0.58	0.62	0.023	0.024
F	0.58	0.62	0.023	0.024
G	0.68	0.72	0.027	0.028
H	0.68	0.72	0.027	0.028
J	0.23	0.27	0.009	0.011
K	1.30	1.5	0.051	0.055
L	2.60	2.70	0.102	0.106
M	0.60	0.70	0.024	0.028
R	0.00	0.10	0.000	0.004
P	0.08	0.17	0.003	0.007

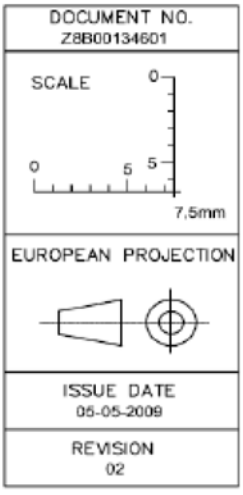


Figure 1 Outlines MG-WDSON-2, dimensions in mm/inches

7 Package outlines

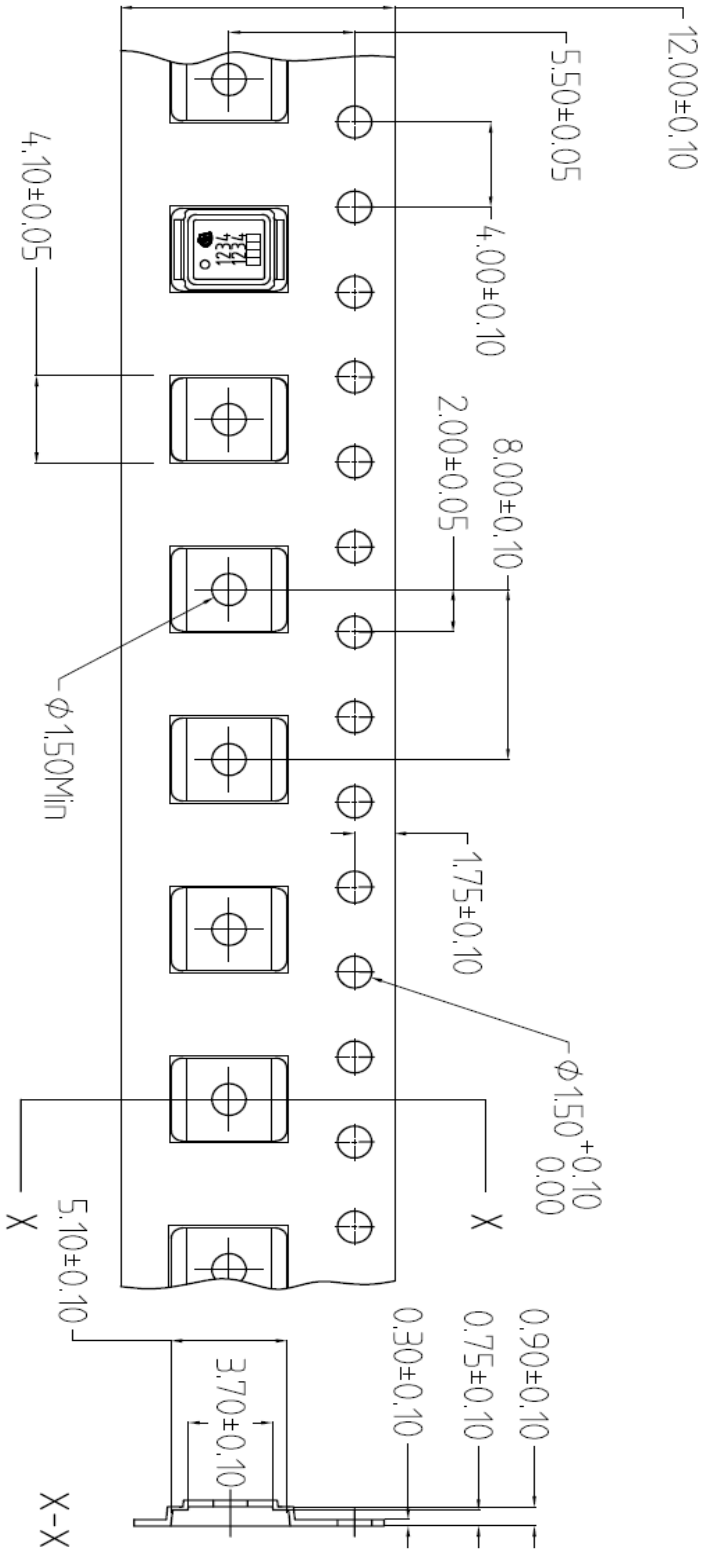
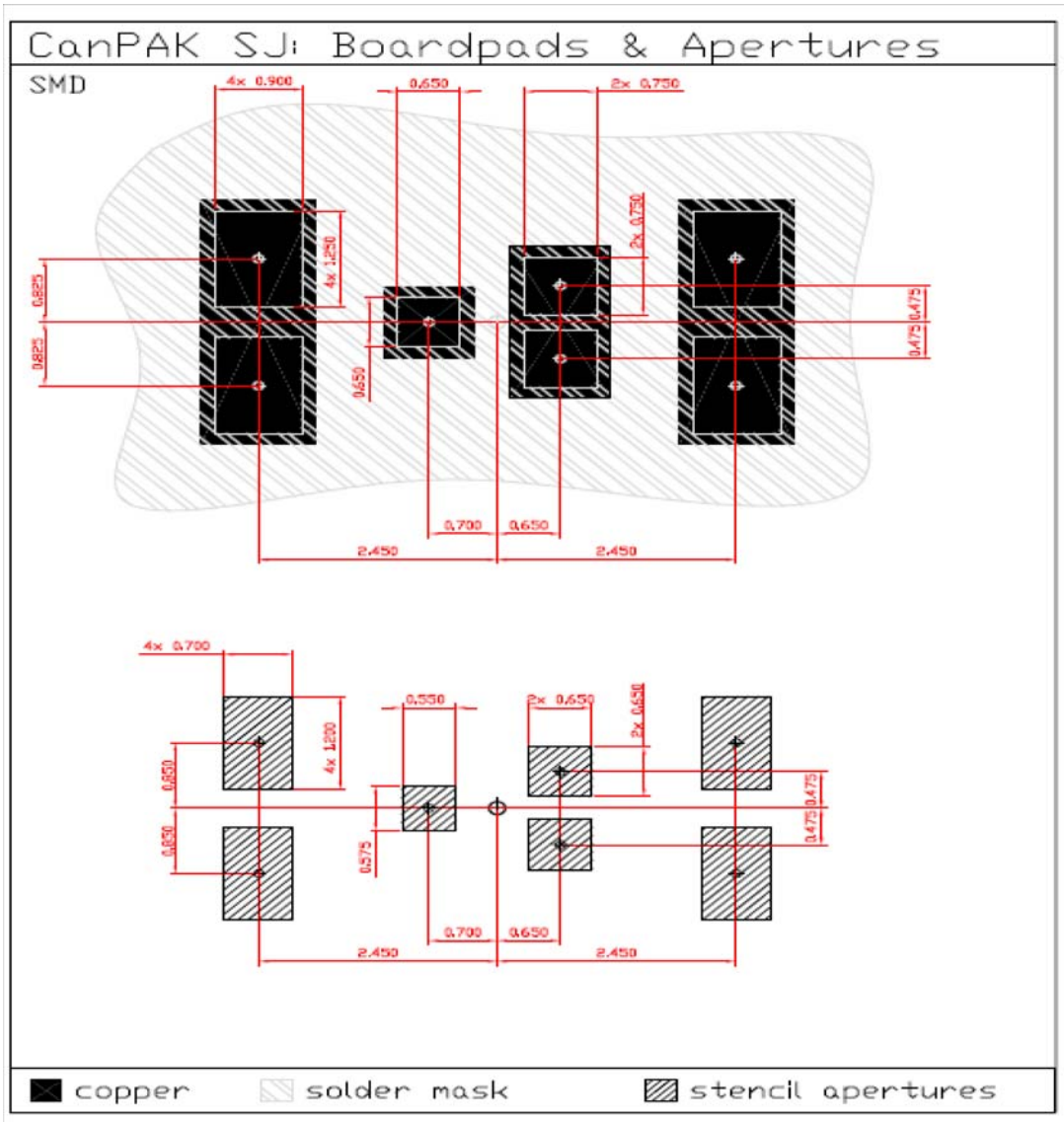
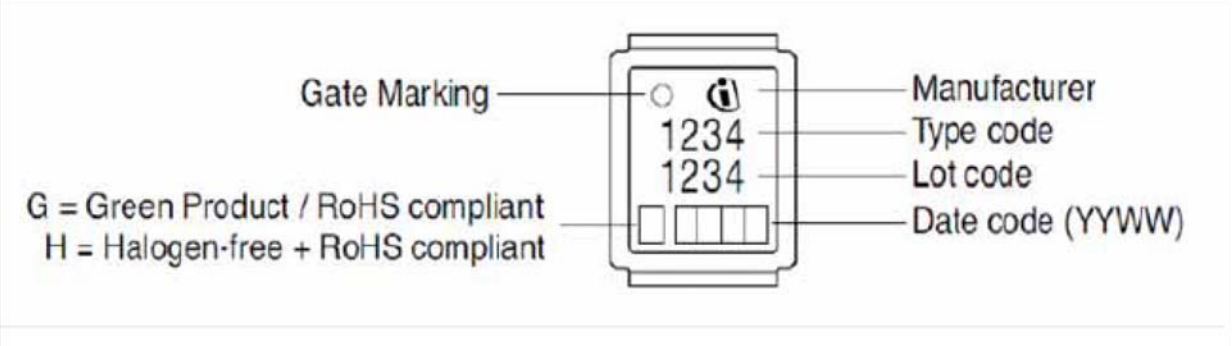


Figure 2 Outlines MG-WDSON-2, dimensions in mm/inches

8 Package outlines



9 Marking layout



9 Revision History

Revision History: 2011-05-31, 2.4

Previous Revision:

Revision	Subjects (major changes since last revision)
0.1	Release of target data sheet
1.0	Release Preliminary data sheet
2.2	Release Final data sheet
2.4	DirectFET Disclaimer expired

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?
Your feedback will help us to continuously improve the quality of this document.
Please send your proposal (including a reference to this document) to: **erratum@infineon.com**

Edition 2011-05-31

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.