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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ADVANTECH

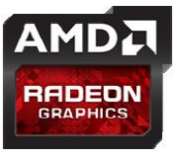
Enabling an Intelligent Planet

GFX-AE9260L16-5J

1A1-E000350ADP

Embedded PCIe Graphics

4 x Mini DP with cable locking



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1. Specification

Model Name	GFX-AE9260L16-5J
Graphics Engine	AMD Embedded Radeon E9260
Process Node	Fin FET 14 nm
Engine Clock (max)	Up to 1200 MHz
Graphics Memory	128-bit, 4 GB GDDR5
Memory Clock (max)	1750 MHz / 7.0 Gbps
Bus Interface	PCI Express® 3.0 (x8) PCI Express x16 Length
Shader Processing Units	896 Shaders
Floating Point Performance	2.2 TFLOPs
DirectX® Capability	DirectX® 12
Shader Model	Shader Model 5.0
OpenGL™	OpenGL™ 4.5
OpenCL™	OpenCL™ 2.0
VULKAN™	VULKAN™ Support
Unified Video Decoder (UVD)	UVD 6.3 for H.265/HEVC, 4K H.264, VC-1, MPEG-2 MPEG-4 part 2 decode
Display Interface	4 x Mini DP with cable locking
Maximum Resolution	DisplayPort: 3840x2160
Power Consumption	75 W
Operating Temperature	0°C ~ 50°C
Dimension	173 x 69 mm

2. Functional Overview

2.1. Memory Interface

AMD Radeon E9260 has four (128-bit) DRAM sequencers. Each DRAM channel is 32-bit wide. All DRAM devices must be of the same type, have the same size on each channel, and must run at the same voltage.

2.2. Acceleration Features

- Support for DirectX® 12 (Feature Level 12_0) features, including the full-speed 32-bit floating point per component operation:
  - Shader Model 5.0 geometry and pixel support in a unified shader architecture.
  - Support for OpenGL 4.5.
  - Support for OpenCL™ 2.0
  - Support for Mantle
  - Support for AMD LiquidVR™
  - Anti-aliasing filtering:
    - 2×/4×/8× MSAA (multi-sample anti-aliasing) modes are supported.
    - A multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
    - Custom filter anti-aliasing with up to 12-samples per pixel.
    - An adaptive anti-aliasing mode.
    - Lossless color compression (up to 16:1).
  - Anisotropic filtering:
    - Continuous anisotropic with 1× through 16× taps.
    - Up to 128-tap texture filtering.
    - Anisotropic biasing to allow trading quality for performance.
    - Improved anisotropic filtering with unified non-power of two-tap distribution and higher precision filter computations.
    - Advanced texture compression (3Dc+™).
    - High quality 4:1 compression for normal and luminance maps.
    - Angle-invariant algorithm for improved quality.
    - Single- or two-channel data format compatibility.
  - 3D resources virtualized to a 40-bit virtual addressing space, for support of large numbers of render targets and textures.

- Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.
- Lossless z-buffer compression for both z and stencil.
- Fast z-buffer clear.
- Fast color-buffer clear.
- Z-cache optimized for real-time shadow rendering.
- Z- and color-compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

2.3. Display System

The display system supports accelerated display modes on multiple independent display controllers.

The full features of the display system are outlined in the following sections.

- Up to four independent display controllers that support up to true 36-bpp (bits per pixel) throughout the display pipe.
- Support for each display output type up to the following display timings:
  - DisplayPort 1.3 up to two 5120 × 2880 pixel resolution display @ 60 Hz refresh rates on two single stream (SST) DisplayPort 1.3 outputs, and up to four 3840 × 2160 @ 60 Hz or 4096 × 2160 @ 60 Hz displays
  - HDMI™ 2.0b (6 Gbit/s) up to four 3840 × 2160 @ 60 Hz or four 4096 ×2160 @ 60 Hz outputs
  - Dual-link DVI up to two 2560 × 1600 @ 60 Hz or 1920 × 1200 @ 60 Hz
  - Single-link DVI up to four 1920 × 1200 @ 60 Hz
- Support for up to four independent display timings on DisplayPort, HDMI, or DVI interfaces
- Advanced video capabilities, including high-fidelity gamma, color correction, and scaling for High Dynamic Range (HDR) or Standard Dynamic Range (SDR)
- HDCP supported independently and simultaneously on all HDMI, DVI, and DisplayPort outputs

  Note: HDCP is available only to licensed HDCP licensees and can only be enabled when connected to an HDCP-capable receiver
  - Supports HDCP version 1.4/2.2 protection for the HDMI interface
  - Supports HDCP version 1.1/2.2 protection for the DisplayPort interface
  - Supports HDCP version 1.4 protection for the DVI interface

- Support for Stereo 3D displays through HDMI, DisplayPort, and DVI. Includes frame-sequential and frame-packed full Stereo 3D modes. Also 2D frame- compatible modes including side-by-side, top-and-bottom, line interleaved, and pixel interleaved
- Line or pixel interleave Stereo 3D mixing supported without the use of graphics shaders by using two display pipes for left and right and blending together immediately before the display output; this improves the Stereo 3D performance.

2.4. DVI/HDMI Features

- Advanced DVI capability supporting 10-bit output when using dual-Link DVI up to 1920 × 1200 @ 60 Hz
- Supports industry-standard CEA-861-E video modes including 480p, 720p,1080i, and 1080p, and 2160p.
- Supports AMD FreeSync™ technology on HDMI using AMD's vendor specific extension:
  - Fully HDMI compliant
  - Requires at least one display that is capabale of AMD HDMI FreeSync™technology
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—165 MP/s (megapixels per second) for single-link DVI
  - DVI—330 MP/s for dual-link DVI
  - HDMI—594 MP/s

2.5. DisplayPort (DP) Features

- Supports all the mandatory features of the DisplayPort Standard Version 1.3 and the following optional features on all links:
  - HBR3 (8.1 Gbps) support
  - ACM packet-type support
  - ISRC packet-type support
  - Y-only colormetry
- DisplayPort Multi-streaming Transport (MST) allowing up to four display pipelines to drive a single DisplayPort interface (provided the DisplayPort link bandwidth is not exceeded)
- Supports AMD FreeSync™ technology, which dynamically synchronizes the refresh rate of a display with the frame rate of the GPU:
  - Based on DisplayPort™ Adaptive-Sync technology
  - Requires at least one display that is capable of DisplayPort Adaptive-Sync technology

- Each DisplayPort link can support three options for the number of lanes and three options for link-data rate as follows:
  - Four, two, or one lane(s)
  - 8.1-, 5.4-,2.7-, or 1.62-Gbps link-data rate per lane
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth
- The following table shows the maximum pixel rates for four, two, or one lane(s) at 8.1-Gbps link rate.

	18 bpp	24 bpp	30 bpp	36 bpp
One Lane	360 MP/s	270 MP/s	216 MP/s	180 MP/s
Two Lanes	720 MP/s	540 MP/s	432 MP/s	360 MP/s
Four Lanes	1080 MP/s	1080 MP/s	864 MP/s	720 MP/s

2.6. Integrated HD-Audio Controller (Azalia) and Codec

- Each HDMI, DisplayPort, and wireless display output supports HD audio stream independently, up to a maximum of four output streams
- Maximum output bandwidth of 73.728 Mbit/s.
- Low power ECN support.
- Hardware silent stream for power optimization during no audio periods
- Function level reset.
- Compatible Microsoft® UAA driver support for basic audio.
- For advanced functionality (as follows), an AMD or a third party driver is required.
- LPCM:
  - Speaker formats: 2.0, 2.1, 3.0, 4.0, 5.1, 6.1, and 7.1
  - Sample rates: 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
  - Bits per sample: 16, 20, and 24
- Non-HBR Compressed audio pass-through up to 6.144 Mbps:
  - Supports AC-3, MPEG1, MP3 (MPEG1 layer 3), MPEG2, AAC, DTS, ATRAC, Dolby Digital+, WMA Pro, and DTS-HD.
- HBR compressed audio pass-through up to 24.576 Mbps:
  - Supports DTS-HD Master Audio and Dolby True HD.

- Plug-and-Play:
  - Sink audio format capabilities declaration.
  - Sink information.
  - AV association.
- Lip sync information.
- HDCP content protection
- DisplayPort supports Global TimeCode using the regular AUX channel—GTC master mode only

2.7. Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 3.0, up to 8.0 GT/s.
- Supports ×1, ×2, ×4, ×8 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×8 lane reversal where the receivers on lanes 0 to 7 on the graphics endpoint are mapped to the transmitters on lanes 7 down to 0 on the root complex.
- Supports ×8 lane reversal where the transmitters on lanes 0 to 7 on the graphics endpoint are mapped to the receivers on lanes 7 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

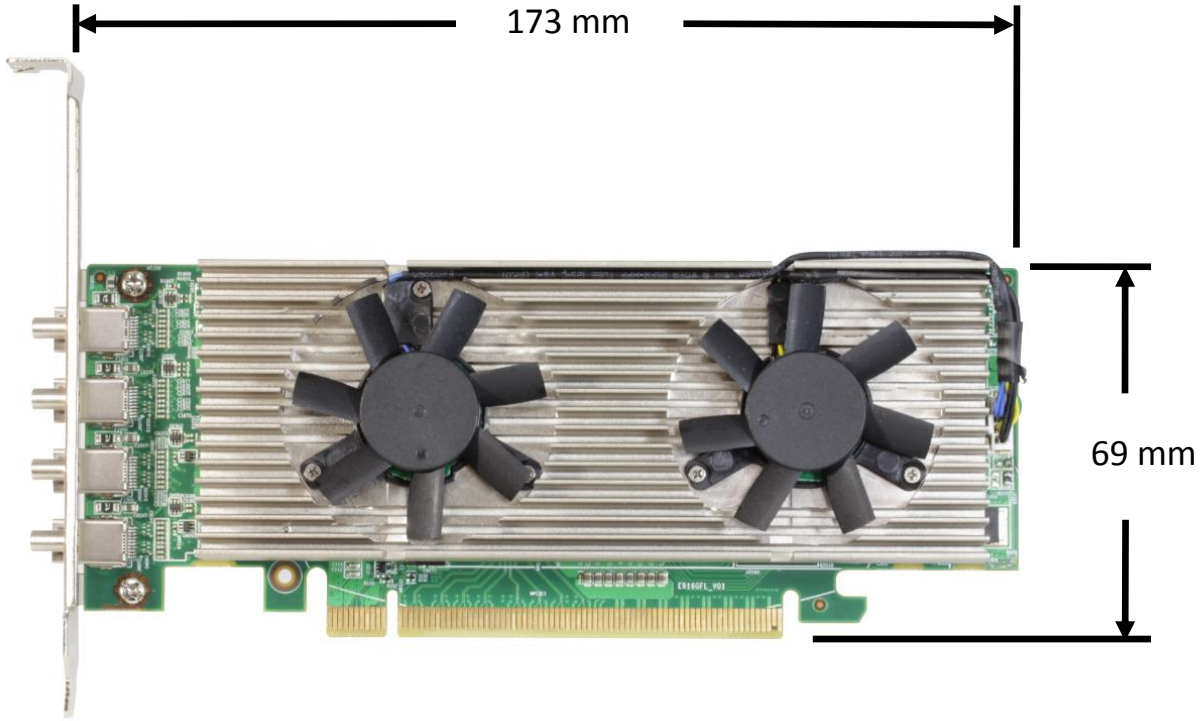
3. PIN Assignment and Description

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1, Differential pair	RSVD	Reserved
20	HSOn(1)		GND	Ground
21	GND	Ground	HSIp(1)	Receiver Lane 1, Differential pair
22	GND	Ground	HSIn(1)	
23	HSOp(2)	Transmitter Lane 2,	GND	Ground

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
24	HSOn(2)	Differential pair	GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2, Differential pair
26	GND	Ground	HSIn(2)	
27	HSOp(3)	Transmitter Lane 3, Differential pair	GND	Ground
28	HSOn(3)		GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3, Differential pair
30	RSVD	Reserved	HSIn(3)	
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	HSOp(4)	Transmitter Lane 4, Differential pair	RSVD	Reserved
34	HSOn(4)		GND	Ground
35	GND	Ground	HSIp(4)	Receiver Lane 4, Differential pair
36	GND	Ground	HSIn(4)	
37	HSOp(5)	Transmitter Lane 5, Differential pair	GND	Ground
38	HSOn(5)		GND	Ground
39	GND	Ground	HSIp(5)	Receiver Lane 5, Differential pair
40	GND	Ground	HSIn(5)	
41	HSOp(6)	Transmitter Lane 6, Differential pair	GND	Ground
42	HSOn(6)		GND	Ground
43	GND	Ground	HSIp(6)	Receiver Lane 6, Differential pair
44	GND	Ground	HSIn(6)	
45	HSOp(7)	Transmitter Lane 7, Differential pair	GND	Ground
46	HSOn(7)		GND	Ground
47	GND	Ground	HSIp(7)	Receiver Lane 7, Differential pair
48	PRSNT#2	Hot plug detect	HSIn(7)	
49	GND	Ground	GND	Ground

4. Board Configuration

4.1 Board Dimension

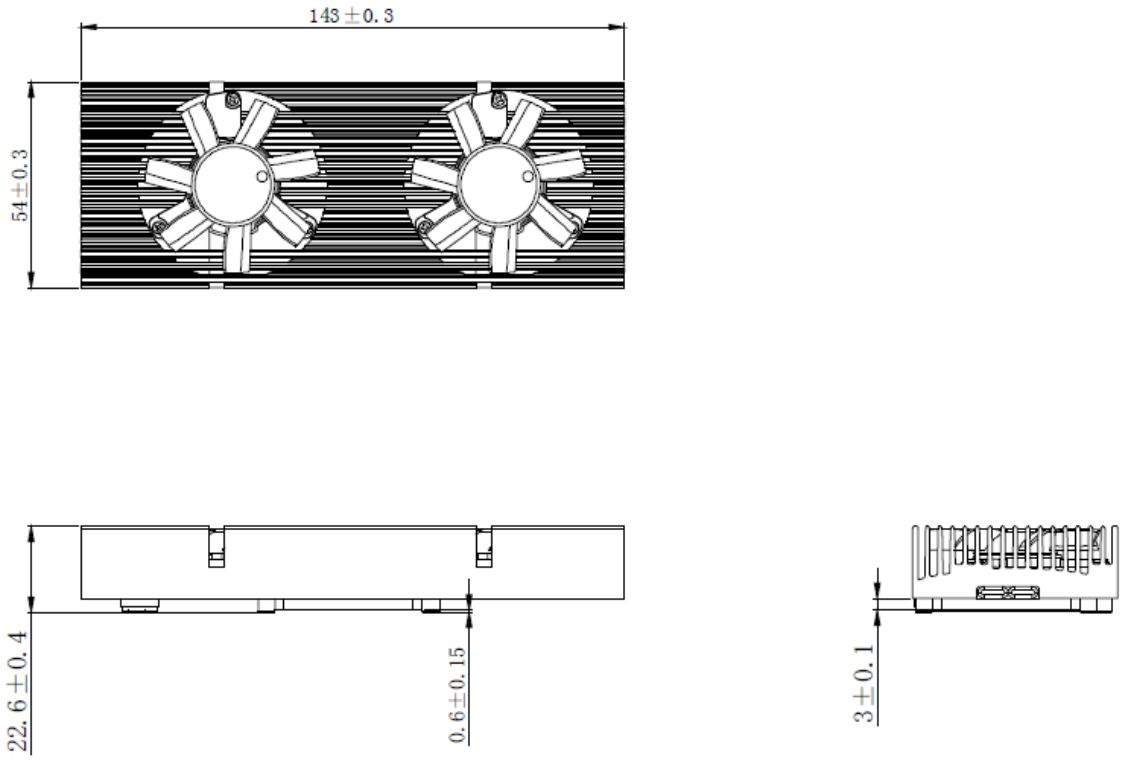


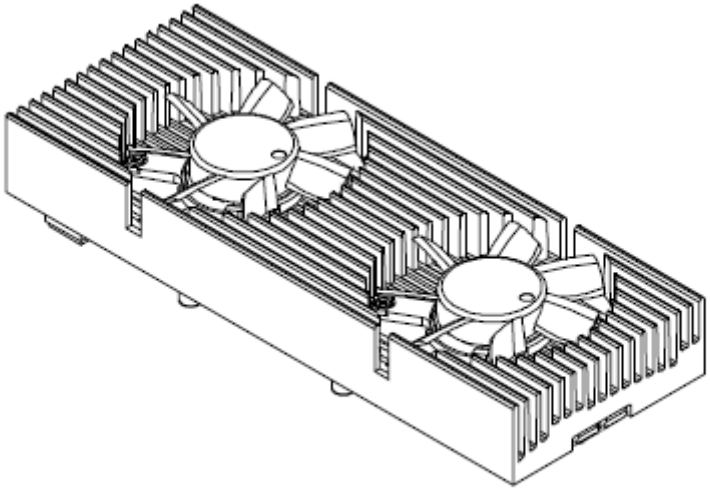
4.2 Display Interface

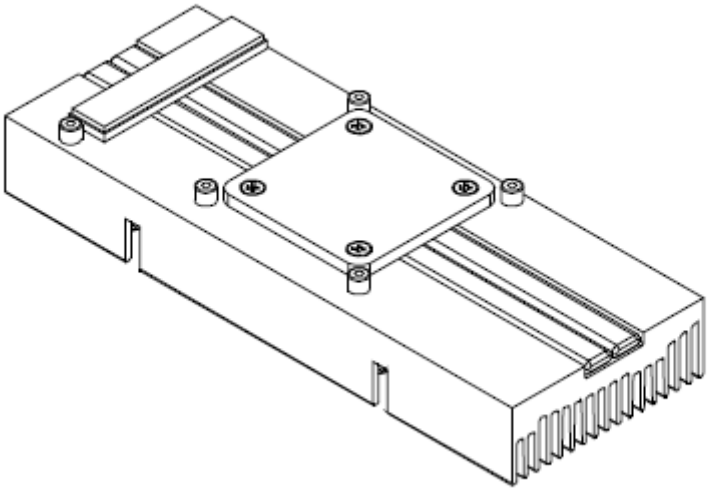
5. Thermal Mechanism

5.1 Fan Thermal Module

(Unit : mm)







Change log list

Rev.	Data	History
1.0	2017/03/06	ER16GFL-CK4 datasheet