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Key Features

- Dual non-inverted 75Ω cable interface with on-chip termination
- SMPTE ST 2082-1, ST 2081-1, ST 424, ST 292-1 and ST 259 compliant input/output
- Multi-standard operation from 1Mb/s to 11.88Gb/s
- Cable driver features:
  - Wide swing control
  - Pre-emphasis to compensate for significant insertion loss between device output and BNC
  - Manual output slew rate control
  - Manual or automatic Mute or disable on LOS
- Trace equalizer features:
  - Integrated 100Ω, differential input termination
  - Automatic power down on loss of signal
  - Adjustable carrier detect threshold
  - DC-coupling from 1.2V to 2.5V CML logic
  - Trace equalization to compensate for up to 15" FR4 at 11.88Gb/s
  - Input offset compensation

Additional Features

- Single 1.8V power supply for analog and digital core
- 2.5V or 3.3V for cable driver output supply
- GSPI serial control and monitoring interface
- Four configurable GPIO pins for control or status monitoring
- Wide operating temperature range: -40°C to +85°C
- Small 6mm x 4mm 40-pin QFN
- Pb-free/Halogen-free/RoHS and WEEE compliant package
- Pin compatible with the GS12181, GS12182, GS12281, and GS3281

Applications

Next Generation 12G UHD-SDI infrastructures designed to support UHDTV1, UHDTV2, 4K D-Cinema and 3D HFR and HDR production image formats. Typical applications: Cameras, Switchers, Distribution Amplifiers and Routers.

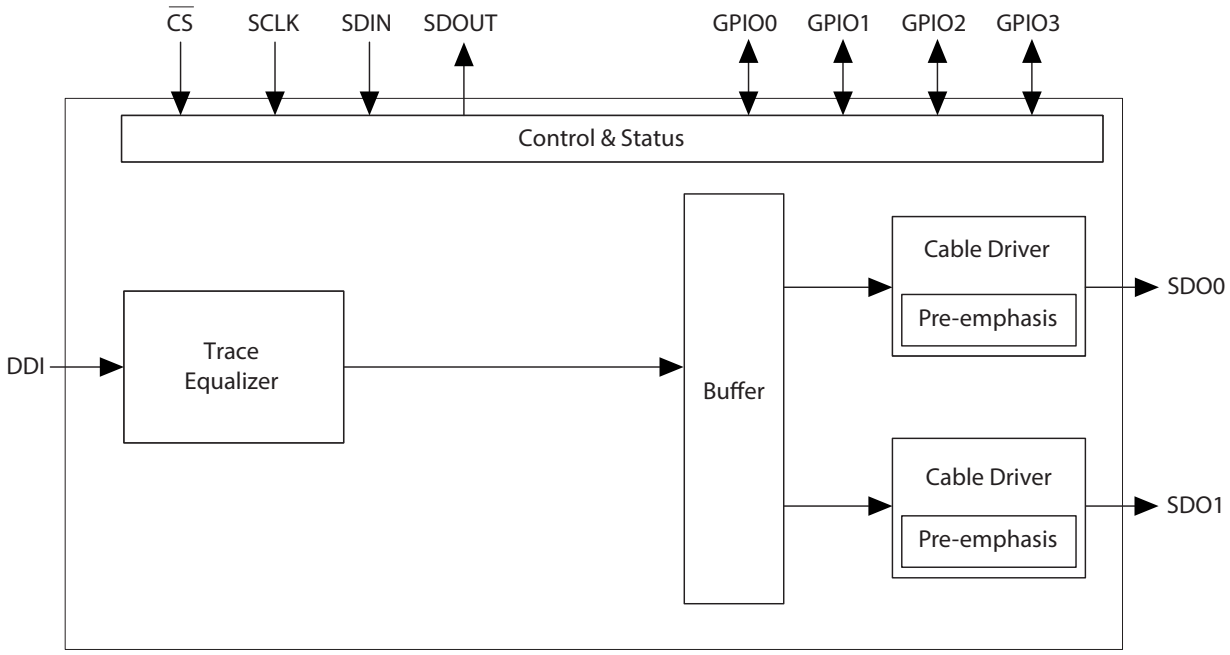
Description

The GS12081 is a low-power, multi-rate, cable driver supporting rates up to 12G UHD-SDI. It is designed to receive 100Ω differential input signals, and transmit the signal over 75Ω coaxial cables. The 100Ω trace input supports up to 17dB of insertion loss.

The two cable drivers have highly configurable pre-emphasis and swing controls to compensate for long trace and connector losses. Additionally, user selectable output slew rate control is provided for each cable driver output.

The GS12081 is pin compatible with the GS12181 and GS12281 single input, and the GS12182 dual input 12G UHD-SDI Multi-rate Re-timing Cable Drivers, as well as the GS3281 3G SDI Multi-rate Re-timing Cable Driver.

Note: For the GS12081 to be pin compatible with the GS12182, careful design considerations are required. Contact for your local Semtech FAE for details.



GS12081 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
3	038689	—	September 2017	Updated values in Table 2-2 and Table 2-3.
2	037841	—	August 2017	Added Section 4.5.12, and Section 4.3.2. Updated Section 4.5.13.
1	034026	—	November 2016	Figure 4-1, Section 4.4 updated. Added Section 4.5.11. Updates made to register map, Section 5.
0	031406	—	July 2016	New Document.

Contents

1. Pin Out

1.1 GS12081 Pin Assignment

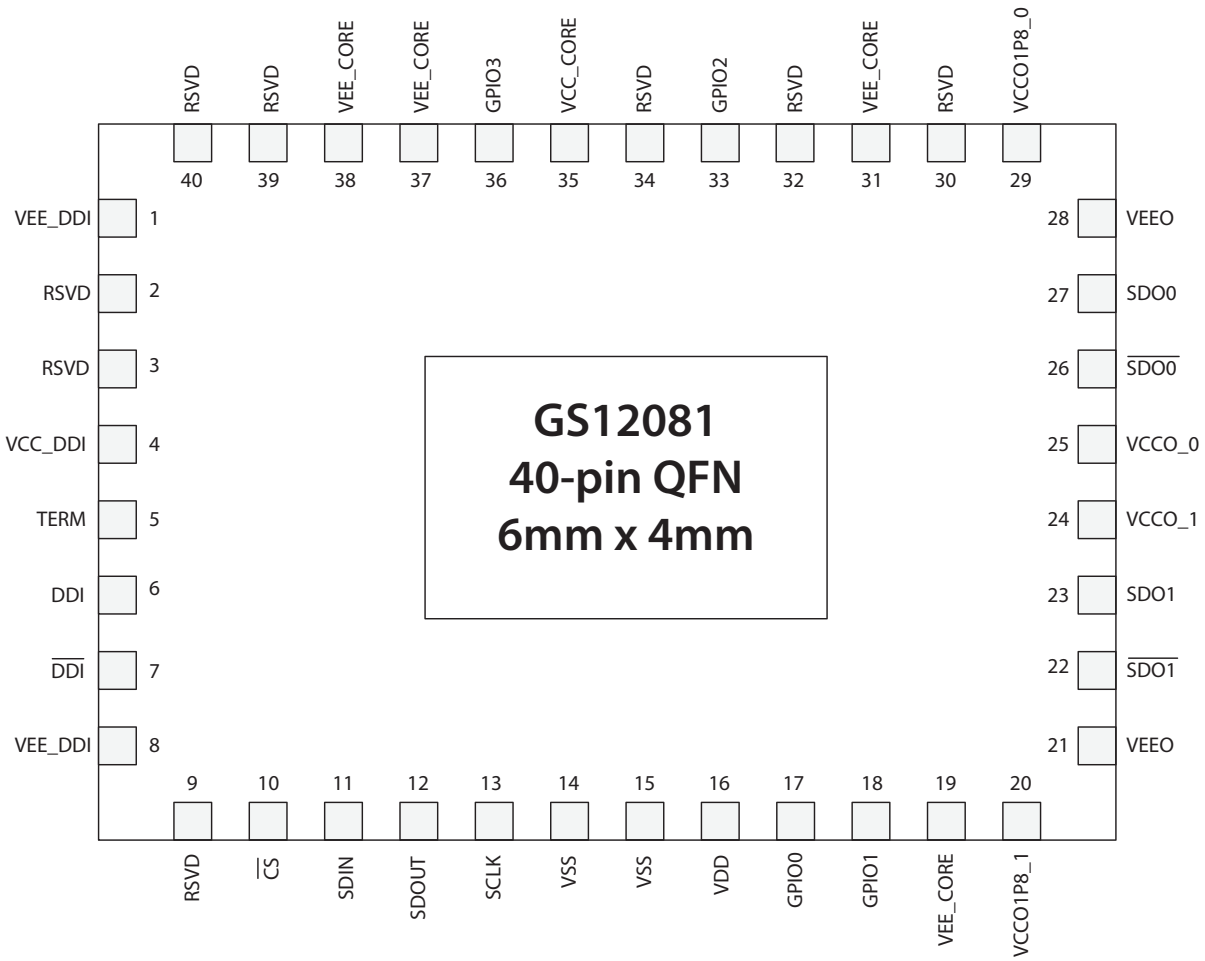


Figure 1-1: GS12081 Pin Assignment

1.2 GS12081 Pin Descriptions

Table 1-1: GS12081 Pin Descriptions

Pin Number	Name	Type	Description
1, 8	VEE_DDI	Power	Most negative power supply connection for the Trace Equalizer. Connect to ground.
2, 3, 9, 30, 32, 34, 39, 40	RSVD	—	These pins may be left floating. Please contact your Semtech FAE for additional information on circuit compatibility with the GS12241.
4	VCC_DDI	Power	Most positive power supply connection for the Trace Equalizer. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
5	TERM	—	Input Common Mode termination. Decouple to ground. See Section 6.1 Typical Application Circuit for values.
6, 7	DDI, $\overline{\text{DDI}}$	Input	Serial digital differential input. Differential CML input with internal 100Ω termination.
10	$\overline{\text{CS}}$	Digital Input	Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-up. Active-LOW input. Refer to Section 4.5.1 for more details.
11	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.5.2 for more details.
12	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS output. Refer to Section 4.5.3 for more details.
13	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.5.4 for more details.
14, 15	VSS	Power	Most negative power supply for digital core logic. Connect to ground.
16	VDD	Power	Most positive power supply connection for digital core logic. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
17	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Default function: Direction = Output Signal = High indicates LOS (Loss of Signal, inverse of Carrier Detect) Pin is 1.8V CMOS I/O, please refer to GPIO0_CFG for more information on how to configure GPIO0.

Table 1-1: GS12081 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
18	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Default function: Direction = Output Signal = Unassigned. Configure to the most appropriate GPIO function for the intended application. Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1.
19, 31, 37, 38	VEE_CORE	Power	Most negative power supply connection for the analog core. Connect to ground.
20	VCCO1P8_1	Power	Most positive power supply connection for cable driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
21, 28	VEEO	Power	Most negative power supply connection for the output drivers. Connect to ground.
22, 23	$\overline{\text{SDO1}}$,SDO1	Output	Differential CML output with two internal 75Ω pull-ups. **Note:** If one of the two outputs is not used by the application, ensure that it is connected to ground through a capacitor and resistor. See Section 6.1 Typical Application Circuit for values.
24	VCCO_1	Power	Most positive power supply connection for the SDO1/ $\overline{\text{SDO1}}$ output driver. Connect to 2.5V or 3.3V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
25	VCCO_0	Power	Most positive power supply connection for the SDO/$\overline{\text{SDO0}}$ output driver. Connect to 2.5V or 3.3V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
26, 27	$\overline{\text{SDO0}}$, SDO0	Output	Differential CML output with two internal 75Ω pull-ups. **Note:** If one of the two outputs is not used by the application, ensure that it is connected to ground through a capacitor and resistor. See Section 6.1 Typical Application Circuit for values.
29	VCCO1P8_0	Power	Most positive power supply connection for cable driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
33	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. Default function: Direction = Input Signal = Set high to put device in sleep Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2.
35	VCC_CORE	Power	Most positive power supply connection for the analog core. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.

Table 1-1: GS12081 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
36	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Default function: Direction = Input Signal = Set high to disable SDO1/$\overline{\text{SDO1}}$ Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3.
Tab	—	—	Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation. It is not commended to connect device ground pins to the central paddle.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage—Core (VCC_DDI, VCC_CORE, VDD)	-0.5V to +2.2V
Supply Voltage—Output Driver (VCCO_0, VCCO_1)	-0.5V to +3.65V
Input ESD Voltage (any pin)	2kV HBM
Storage Temperature Range (T_S)	-50°C to +125°C
Input Voltage Range (DDI, $\overline{DDI}$)	-0.3 to (VCC_DDI +0.3)V
Input Voltage Range (GPIO2, GPIO3 REF_CLK)	-0.3 to (VCC_CORE +0.3)V
Input Voltage Range ($\overline{CS}$, SDIN, SCLK, VSS, VDD, GPIO0, GPIO1)	-0.3 to (VDD +0.3)V
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	VCC_DDI, VCC_CORE, VDD		1.71	1.8	1.89	V	—
Supply Voltage - Output Driver	VCCO_0, VCCO_1		2.38	2.5	2.63	V	—
			3.14	3.3	3.47	V	—
Power - Mission Mode (SDO0/$\overline{\text{SDO0}}$ enabled SDO1/$\overline{\text{SDO1}}$ disabled)	P_D	VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$	—	170	—	mW	1
		VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$ with pre-emphasis set to setting of 15	—	185	—	mW	—
		VCCO_0 = 3.3V, Output Swing = 800mV$_{pp}$	—	190	—	mW	1
		VCCO_0 = 3.3V, Output Swing = 800mV$_{pp}$ with pre-emphasis set to setting of 15	—	210	—	mW	—
Power - Mission Mode (SDO0/$\overline{\text{SDO0}}$ disabled SDO1/$\overline{\text{SDO1}}$ disabled)	P_D		—	75	—	mW	1
Power - Sleep Mode	P_D	Sleep	—	40	—	mW	—
Supply Current - Cable Driver	I_{CCO_0}, I_{CCO_1}	VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$	—	23	34	mA	1,4
		VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$, with pre-emphasis set to setting of 15	—	29	38	mA	4
		VCCO_0 = 3.3V, Output Swing = 800mV$_{pp}$	—	24	35	mA	1,4
		VCCO_0 = 3.3V, Output Swing = 800mV$_{pp}$, with pre-emphasis set to a setting of 15	—	30	39	mA	4
	I_{CCO1P8_0}, I_{CCO1P8_1}	Output Swing = 800mV$_{pp}$	—	20	28	mA	4
Supply Current – Analog Core	I_{CC_CORE}	SDO0/$\overline{\text{SDO0}}$ disabled, SDO1/$\overline{\text{SDO1}}$ disabled	—	6	12	mA	—

Table 2-2: DC Electrical Characteristics (Continued)

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Current - Trace Equalizer	I_{CC_DDI}		—	21	32	mA	—
Supply Current - Digital Logic	I_{DD}		—	15	18	mA	—
DDI Input Common Mode Voltage	V_{CMIN}		0.94	—	2.525	V	2
SDO Output Common Mode Voltage	V_{CMOUT}		—	$V_{CMOUT} = V_{CCO} - \Delta V_{SDO}/2$	—		—
DDI Input Termination		Differential	—	100	—	Ω	—
SDO Output Termination		Between SDO and GND	—	75	—	Ω	3
Input Voltage - Digital Pins ($\overline{CS}$, SDIN, SCLK, GPIO[0:3])	V_{IH}		0.65* VDD	—	VDD	V	—
	V_{IL}		0	—	0.35* VDD	V	—
Output Voltage - Digital Pins (SDOUT, GPIO[0:3])	V_{OH}	I_{OH} = -5mA	VDD - 0.45	—	—	V	—
	V_{OL}	I_{OL} = +5mA	—	—	0.45	V	—

Notes:

1. Pre-emphasis is disabled.
2. 0.94V is when trace EQ is DC coupled to upstream driver running from 1.2V supply, and 2.525V is when trace EQ is DC coupled to upstream driver running from 2.5V supply.
3. Applies to both SDO0 and SDO1.
4. The specifications provided are per symbol, not a combined value.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VCC_DDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +2.5/3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR_{DDI}	—	0.001	—	11.88	Gb/s	—
Serial Output Voltage Swing	V_{SDO}	—	720	800	880	mV_{pp}	3
Differential Input Voltage Swing	ΔV_{DDI}	—	200	—	800	mV_{ppd}	—
Input Trace Equalization	—	12G	—	15	—	Inches	14dB, 5,7
		6G	—	20	—	Inches	12dB, 5
		3G	—	40	—	Inches	13dB, 5
		HD	—	40	—	Inches	6dB, 5
		SD	—	40	—	Inches	3dB, 5
		MADI	—	40	—	Inches	3dB, 5
Intrinsic Input Jitter Tolerance Square Wave Modulation	IIJT	12G	0.7	0.85	—	UI	—
		MADI/SD/HD/3G/6G	0.8	0.95	—	UI	—
SDO/$\overline{SDO}$ Rise/Fall Time	$t_{riseSDO}$, $t_{fallSDO}$	SD	400	—	1000	ps	4
		HD/3G	—	—	70	ps	4
		6G/12G	—	—	40	ps	4
SDO/$\overline{SDO}$ Mismatch in Rise/Fall Time	—	SD	—	—	100	ps	4
		HD/3G	—	—	20	ps	4
		6G/12G	—	—	10	ps	4
SDO/$\overline{SDO}$ Eye Cross Shift	—	SD	—	—	5	%	4
		HD/3G	—	—	8	%	4
		6G/12G	—	—	9	%	4
SDO/$\overline{SDO}$ Overshoot	—	—	—	—	10	%	4
Output Return Loss	—	5MHz to 1.485GHz	—	—	-17	dB	1
		1.485GHz to 2.97GHz	—	—	-12	dB	1
		2.97GHz to 5.94GHz	—	—	-8	dB	1
		5.94GHz to 11.88GHz	—	—	-5	dB	1

Table 2-3: AC Electrical Characteristics (Continued)

VCC_DDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +2.5/3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Data Output Jitter (SDO/$\overline{SDO}$)	$t_{OJ(11.88Gb/s)}$	Pattern = PRBS	—	0.06	0.2	UI_{pp}	2, 4, 6
	$t_{OJ(5.94Gb/s)}$		—	0.03	0.15	UI_{pp}	2, 4, 6
	$t_{OJ(2.97Gb/s)}$		—	0.03	0.15	UI_{pp}	2, 4, 6
	$t_{OJ(1.485Gb/s)}$		—	0.03	0.15	UI_{pp}	2, 4, 6
	$t_{OJ(270Mb/s)}$		—	0.04	0.15	UI_{pp}	2, 4, 6
	$t_{OJ(125Mb/s)}$		—	0.02	0.1	UI_{pp}	2, 4, 6

Notes:

1. Values achieved with Semtech evaluation board and connector.
2. Measured using a clean input source.
3. Default driver swing Setting.
4. This specification applies to SDO0/$\overline{SDO0}$ and SDO1/$\overline{SDO1}$.
5. Trace insertion loss was measured with FR4 material using 7 mil stripline traces using a PRBS23 signal.
6. Measured under minimal trace loss conditions.
7. Measured with an input launch swing of 800mVpp and trace equalizer set to 8.

Note: For GSPI Timing see Table 4-4: GSPI Timing Parameters.

3. Input/Output Circuits

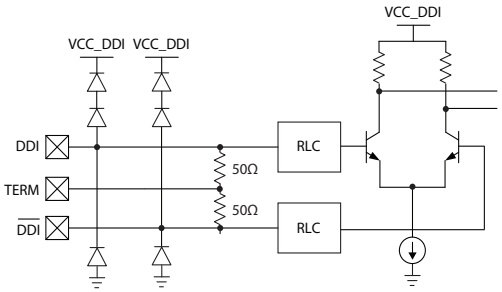


Figure 3-1: DDI, $\overline{\text{DDI}}$

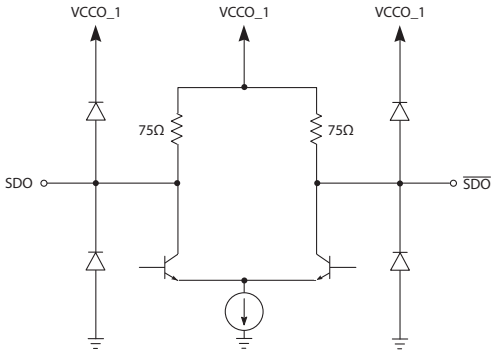


Figure 3-2: SDO0/$\overline{\text{SDO0}}$ and SDO1/$\overline{\text{SDO1}}$

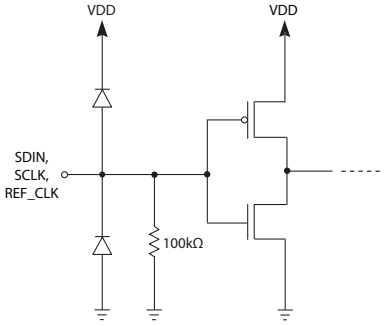


Figure 3-3: SDIN, SCLK

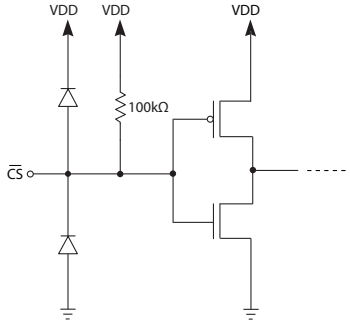


Figure 3-4: $\overline{\text{CS}}$

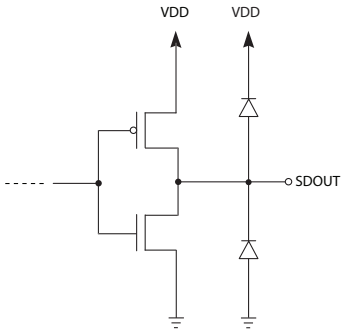


Figure 3-5: SDOUT

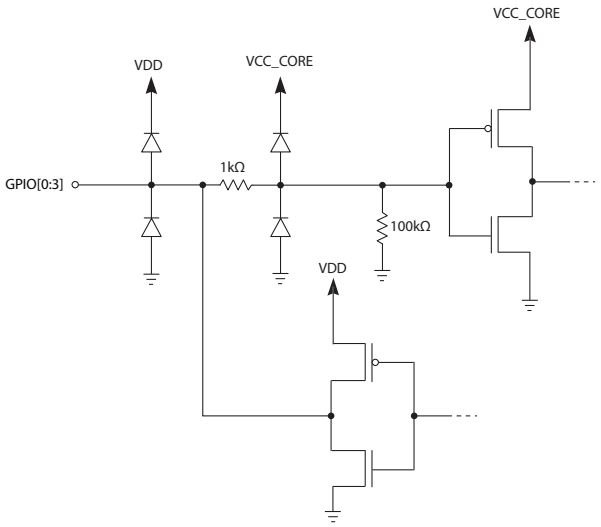


Figure 3-6: GPIO[0:3]

4. Detailed Description

4.1 Device Description

The GS12081 is a dual output SMPTE compliant cable driver with integrated 75Ω internal terminations. It includes a 100Ω differential trace equalizer to receive the outgoing signal from the system. The Trace Equalizer has manual offset correction and boost control, which can compensate for 17dB of insertion loss at 5.94GHz. The Cable Driver has amplitude and pre-emphasis control to compensate for significant insertion loss between device output and BNC. The pre-emphasis control is two dimensional, where both pre-emphasis pulse amplitude and width adjustments can be made to help optimize for interconnect mismatches such as vias and connectors.

Note: The parameters referred to within Section 4.2.1 to Section 4.2.2 are linked to their respective registers in Table 4-1. For a complete list of registers and functions, please see Section 5.

4.1.1 Sleep Mode

To enable low power operation, the GS12081 has manual and automatic sleep mode control.

The default mode is automatic sleep mode on LOS (Loss of signal). The device can also be manually put into sleep mode. When the device is in sleep mode, all the core blocks are powered-down, except the host interface and carrier detect circuits. The cable driver can be configured to be disabled or muted during sleep.

The **CTRL_AUTO_SLEEP** and **CTRL_MANUAL_SLEEP** parameters in register 0x3, control the sleep mode of the device. The default value of the **CTRL_AUTO_SLEEP** parameter is 1_b (auto sleep). While in auto sleep mode, the **CTRL_MANUAL_SLEEP** parameter has no effect. To enable host control of the sleep mode, set the **CTRL_AUTO_SLEEP** parameter to 0_b manual sleep control. To prevent the device from entering sleep, set the **CTRL_MANUAL_SLEEP** parameter to 0_b (not sleep). To manually configure the device to sleep, set the **CTRL_MANUAL_SLEEP** parameter to 1_b (sleep).

The device can also be manually made to sleep through the *GPIO* pins. The default GPIO pin to control sleep is *GPIO2* (pin 33). Drive this pin HIGH to make the device sleep.

4.2 Trace Equalizer

The GS12081 features a differential input buffer with 100Ω differential input termination, which includes a trace equalizer that can be configured to compensate for up to 15" of 7-mil stripline of FR4 at 11.88Gb/s and up to 40" at 3Gb/s.

The differential input signal can be either DC-coupled or AC-coupled and is capable of operation with any binary coded signal that between 1Mb/s and 11.88Gb/s.

The input circuit is compatible with industry standard CML differential transmitters when DC coupled using industry standard 100Ω differential termination circuitry.

The trace equalizer includes a manual input offset compensation circuit. This reduces offset-induced data jitter in the link due to asymmetric performance of DC-coupled upstream differential drivers. The input offset compensation circuit also improves the input sensitivity of the trace equalizer.

Note: The parameters referred to within Section 4.2.1 to Section 4.2.2 are linked to their respective registers in Table 4-1. For a complete list of registers and functions, please see Section 5.

4.2.1 Input Trace Equalization

The trace equalizer can compensate for up to 17dB of insertion loss at 5.94GHz in 8 increments, which can be adjusted through the **CFG_TREQ0_BOOST** parameter in control register 0x1E. The default value of **CFG_TREQ0_BOOST** is (2_h). Please refer to Figure 4-1 for recommended boost setting.

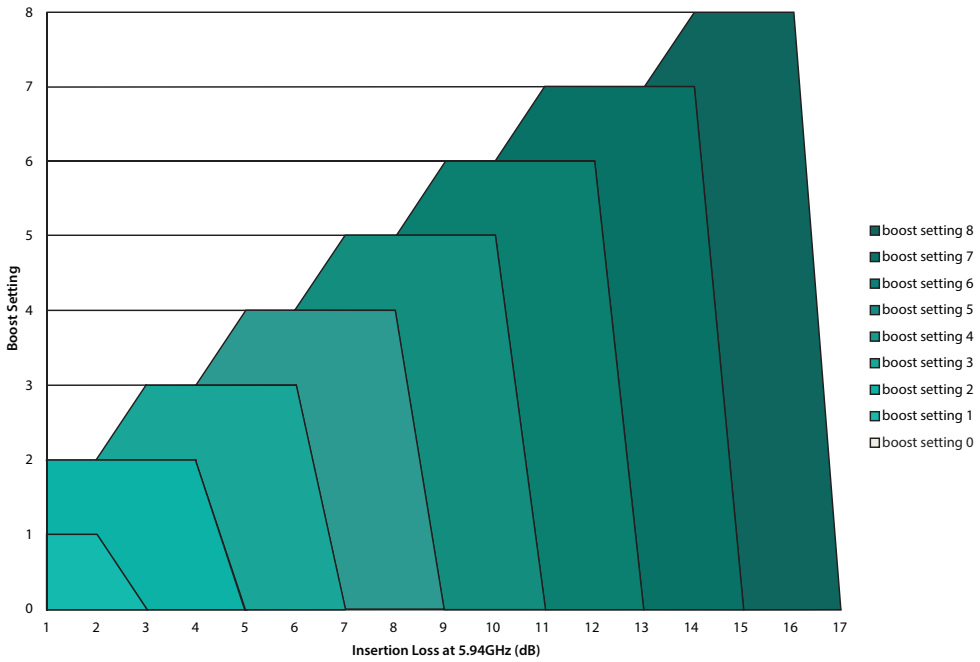


Figure 4-1: GS12081 Trace EQ Boost Setting Recommendation

By default at power up or after system reset, the trace equalizer is configured to compensate for up to 3" of 7-mil stripline in FR4 material at high frequencies.

Note: Although not a requirement, launch swing of 800mV_{ppd} is recommended for trace lengths longer than 5".

4.2.2 CD (Carrier Detect) and LOS (Loss of Signal)

LOS is the complement of CD and is used by various automatic control modes including mute on LOS, which will be covered in the output section of this document.

The default settings of the trace equalizer Carrier Detection sub-block should satisfy most applications; however the Carrier Detection mechanism in the trace equalizer is highly configurable and allows the system designer to optimize the sensitivity and hysteresis of the Carrier Detection mechanism to meet specific system requirements.

The trace equalizer Carrier Detect is reported by status parameter **STAT_PRI_CD** in register 0x87.

The first CD control parameter is **CFG_TREQ0_CD_BOOST** in register 0x1E. This parameter determines the method and therefore the level of equalization to be used on the input signal routed to the Carrier Detection sub-block. The default value is 0_b, which maximizes the level of equalization. Alternatively, the designer can choose to have this signal equalized at the same level as the main input signal, controlled by **CFG_TREQ0_BOOST**, by setting **CFG_TREQ0_CD_BOOST** to 1_b. The setting of this parameter has no impact on the main signal routed to the output.

The last two CD control parameters can be found in register 0x1F. Parameters **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TRE0Q_CD_DEASSERT_THRESH** set the Carrier Detect assert and de-assert thresholds to the input signal, which also defines the hysteresis of CD signal.

The default values of **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TREQ0_CD_DEASSERT_THRESH** are is 4_d and 3_d respectively. With the default settings, the minimum launch swing needed to assert the carrier detect is 200mV and it will be de-asserted when the signal level falls below 150mV.

The **STAT_PRI_CD** (Carrier Detect) parameter will be set to 0_b and the LOS will be set to 1_b whenever a new signal at the input does not exceed the assert threshold, or an existing signal falls below the de-assert threshold. The result is that the outputs will mute (assuming Mute on LOS is left to its default value in the **CONTROL_OUTPUT_MUTE** register 0x49). See Section 4.3.4 for more details.

Given a differential input trace with 17dB of insertion loss at 5.94GHz and **CFG_TREQ0_CD_BOOST** = 0_b, Figure 4-2 illustrates the relationship between launch swing voltage, and minimum threshold setting to assert or de-asset Carrier Detect at all rates up to threshold setting at 11.88Gb/s.

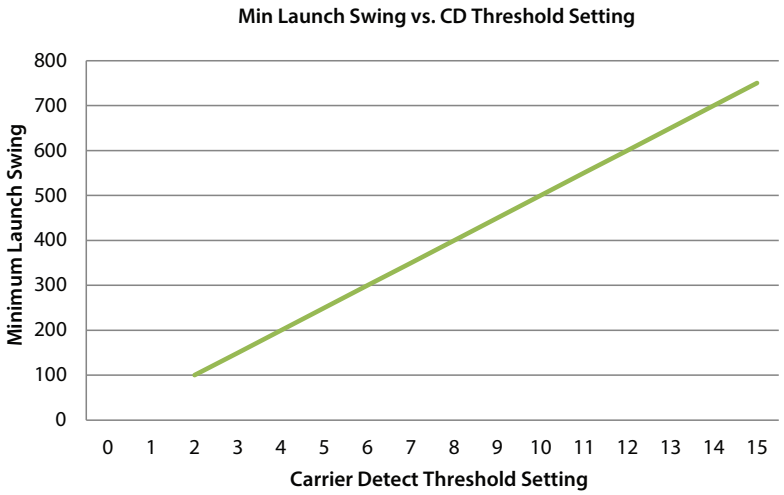


Figure 4-2: Input Voltage Vs. Carrier Detect Threshold Setting

Table 4-1: Trace Equalizer Configuration and Status Parameters

Register Address$_h$ and Name	Parameter Name	Description
1F, TREQ0_CD_ HYSTERESIS	CFG_TREQ0_CD_DEASSERT_THRESH	Sets the Carrier Detect de-assert threshold.
	CFG_TREQ0_CD_ASSERT_THRESH	Sets the Carrier Detect assert threshold.
1E, TREQ0_ INPUT_BOOST	CFG_TREQ0_CD_BOOST	Selects the boost method of the CD signal.
	CFG_TREQ0_BOOST	Sets the Trace Equalizer boost level.
84, STICKY_ COUNTS_0	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.
87, CURRENT_ STATUS_1	STAT_PRI_CD	Primary carrier detection status.

4.3 Output Drivers

The GS12081 features two independently configurable output drivers (see Figure 3-3). The two drivers provide highly configurable amplitude and pre-emphasis control. The signal on the outputs can be inverted to help with signal polarity when layout requires trace inversion. The LOS (Loss of Signal) status from the equalizer stage can be used to automatically mute or disable the outputs on their assertion. The cable drivers can be configured to mute or disable during sleep. The sleep control modes take precedence over the manual or automatic LOS output control modes.

Note: The <n> in the control parameter names refers to the output number. Output 0 is the cable driver output *SDO0/$\overline{SDO0}$*, and output 1 is the cable driver output *SDO1/$\overline{SDO1}$*.

4.3.1 Output Driver Polarity Inversion

The signal polarity may be inverted at the outputs through the **CTRL_OUTPUT<n>_ DATA_ INVERT** parameters in register 0x48. This may be useful to compensate for an inverted upstream signal or to facilitate board signal routing. To invert the polarity of either of the two output drivers, write 1_b to control parameter **CTRL_OUTPUT<n>_DATA_ INVERT**.

4.3.2 Output Driver Data Rate Selection

By default the GS12081 will use the 6G/12G output driver and slew rate group settings for all data rates.

If the application will be using data rates other than 6G/12G, it is recommended that specific data rate group settings are used at all times for optimal performance.

To use specific data rate group settings, the host will need to set **CTRL_OUTPUT<n>_MANUAL_SLEW** to the required rate group. The slew rate options are as follows:

0 = SD/MADI
1 = HD/3G
2 = 6G/12G (default)

Note: It is recommended to enable offset correction for rates HD through 12G to minimize output jitter. This is done by setting **CFG_OFFSET_MANUAL_ENA** = 1 in register 0x1B.

4.3.3 Amplitude and Pre-Emphasis Control

The two output drivers offer very granular amplitude and pre-emphasis control. For optimal loss compensation, both the pre-emphasis pulse amplitude and the pre-emphasis pulse width can be independently configured on both output drivers. This extra flexibility provides a mechanism to better shape the pre-emphasis gain to match the frequency loss response of interconnect composed of trace, connector and via losses. The swing and pre-emphasis can be independently configured for specific data rates.

Note: The following are important points regarding this section.

- The parameters referred to within this section are linked to their respective registers in Table 4-2. For a complete list of registers and functions, see Section 5.
- To configure the GS12081 for specific rate group settings, see Section 4.3.2.

The output swing can be configured for the following three rate groups:

CFG_OUTPUT<n>_CD_SD_DRIVER_SWING (MADI and SD)
CFG_OUTPUT<n>_CD_HD_DRIVER_SWING (HD and 3G)
CFG_OUTPUT<n>_CD_UHD_DRIVER_SWING (6G and 12G)

The output pre-emphasis can be configured for the following two rate groups:

CFG_OUTPUT<n>_CD_HD_PREEMPH_WIDTH (HD and 3G)
CFG_OUTPUT<n>_CD_HD_PREEMPH_AMPL (HD and 3G)
CFG_OUTPUT<n>_CD_UHD_PREEMPH_WIDTH (6G and 12G)
CFG_OUTPUT<n>_CD_UHD_PREEMPH_AMPL (6G and 12G)

The default swing setting is 800mVpp single ended into an external 75Ω load. The swing can be adjusted in ~20mV increments. Applications where maximum output swing and pre-emphasis range are desired, it is recommended that the output supplies *VCCO_0* and *VCCO_1* be connected to a 3.3V supply. For most applications with short trace between GS12081 and output BNC, 2.5V power supply can be used.

4.3.3.1 Pre-Emphasis Optimization

The goal of pre-emphasis is to open the eye at the downstream receiver as much as possible. This means minimizing ISI jitter while meeting sufficient inner eye amplitude to meet a receiver's input sensitivity. The cable driver has the additional requirement to meet the SMPTE output specification.

The GS12081 has a high level of precision for pre-emphasis control, which allows for fine optimization of any loss channel. The default cable driver settings should meet SMPTE output specification for most applications with short (1 to 2 inch) trace between the GS12081 and the output BNC. However, the pre-emphasis values may be adjusted to produce a better-looking eye. It is difficult to provide guidance regarding dB, as a 12G eye diagram looks different depending on the video test equipment used. The designer must optimize for their targets.

Table 4-2: Output Swing and Pre-Emphasis Control Parameters

Register Name and Address$_h$	Parameter Name	Description
0x2B/0x29, OUTPUT_ PARAM_CD_ SD_3/ OUTPUT_ PARAM_CD_ SD_1	CFG_OUTPUT<n>_CD_ SD_DRIVER_SWING	Output amplitude configuration parameter. <n> = 0: For SD and MADI rates on SDO0. <n> = 1: For SD and MADI rates on SDO1.
0x2D/0x2F OUTPUT_ PARAM_ CD_HD_1/ OUTPUT_ PARAM_ CD_HD_3	CFG_OUTPUT<n>_CD_ HD_DRIVER_SWING	Output amplitude configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
0x2C/0x2E OUTPUT_ PARAM_ CD_HD_0/ OUTPUT_ PARAM_ CD_HD_2	CFG_OUTPUT<n>_CD_HD_ PREEMPH_WIDTH	Output pre-emphasis pulse width configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
	CFG_OUTPUT<n>_CD_HD_ PREEMPH_PWRDWN	Output pre-emphasis power down configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
	CFG_OUTPUT<n>_CD_HD_ PREEMPH_AMPL	Output pre-emphasis pulse amplitude configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
0x31/0x33 OUTPUT_ PARAM_ CD_UHD_1/ OUTPUT_ PARAM_ CD_UHD_3	CFG_OUTPUT<n>_CD_UHD_ DRIVER_SWING	Output amplitude configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
0x30/0x32 OUTPUT_ PARAM_ CD_UHD_0/ OUTPUT_ PARAM_ CD_UHD_2	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_WIDTH	Output pre-emphasis pulse width configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_PWRDWN	Output pre-emphasis power down configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_AMPL	Output pre-emphasis pulse amplitude configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
4B CONTROL_ OUTPUT_ SLEW	CTRL_OUTPUT0_MANUAL_SLEW	Manually set the slew rate and output driver rate group to be used for SDO0/$\overline{\text{SDO0}}$ when CTRL_OUTPUT0_SLEW_SEL= 0.
	CTRL_OUTPUT1_MANUAL_SLEW	Manually set the slew rate and output driver rate group to be used for SDO1/$\overline{\text{SDO1}}$ when CTRL_OUTPUT1_SLEW_SEL = 0.

4.3.4 Output State Control Modes

The GS12081 provides several output state control modes to meet specific application requirements. The cable driver has the following three output modes: operational, muted, disabled, or balanced. During non-sleep, if the control modes are configured such that multiple output modes are enabled, the priorities of the control modes from highest to lowest are the following: balanced, disabled, and then muted.Section 4.3.4.1 through Section 4.3.4.3 describe how to configure the output control modes that are enabled during non-sleep. If the device enters sleep, either manually or automatically, the sleep output control modes take precedence over the non-sleep control modes. The default cable driver configuration is for it to be disabled during sleep; however the cable driver can be configured to mute during sleep by setting the **CFG_SLEEP_OUTPUT<n>_MUTE** parameter in register 0x5 to 1_b.

4.3.4.1 Output Mute Control Mode

Each of the outputs on the GS12081 have independent mute control modes, which can be configured through the host interface.

The following are the three output mute control modes:

1. The outputs automatically mute on LOS (default).
2. The outputs never mute.
3. The outputs are always muted.

The first mute control mode listed above is the default power-up configuration for both output drivers (the **CTRL_OUTPUT<n>_AUTO_MUTE** control parameter in register 0x49 is set to 1_b). In this mode, the outputs will automatically mute on the assertion of LOS.

The outputs can be manually configured to never mute by setting both the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_MANUAL_MUTE** control parameters in register 0x49 to 0_b. Alternatively, the outputs can be manually configured to always be muted by setting the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_ MANUAL_MUTE** control parameters to 0_b and 1_b respectively.

4.3.4.2 Output Disable Control Mode

Each of the outputs on the GS12081 also have independent disable control modes, which can be configured through the host interface.

The following are the three output disable control modes:

1. The outputs are never disabled (default).
2. The outputs are automatically disabled on LOS.
3. The outputs are always disabled.

The first disable control mode is the default power-up configuration for both output drivers (the **CTRL_OUTPUT<n>_AUTO_DISABLE** and **CTRL_OUTPUT<n>_MANUAL_DISABLE** control parameters in register 0x49 are both set to 0_b). In this mode, the outputs will never disable. By setting the **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter in register 0x49 to 1_b, the outputs will automatically disable on the assertion of LOS.

The output can be manually disabled by leaving the **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter set to 0_b and setting the **CTRL_OUTPUT<n>_MANUAL_DISABLE** control parameter to 1_b.

The disable control mode takes precedence over the output mute control mode.

4.3.4.3 Output Balanced Control Mode

The GS12081 has a feature designed to facilitate reliable Output Return Loss (ORL) measurement while the device is still powered. The device can be put into a BALANCE mode which prevents the outputs from toggling while ORL is being measured. BALANCE mode can be enabled through the host interface, by setting control parameter **CTRL_OUTPUT<n>_ BALANCED** in register 4D to 1_b. This control mode takes precedence over both the output mute and output disable control modes.

4.3.5 Output Waveform Specifications

The Duty Cycle Distortion (DCD) of the serial digital differential outputs is less than 12ps. DCD is defined as the difference in the width of an output logic "1" versus that of output logic "0" as measured at the 50% point of the output waveform.

The DCD of the serial digital single ended outputs is less than 30ps.

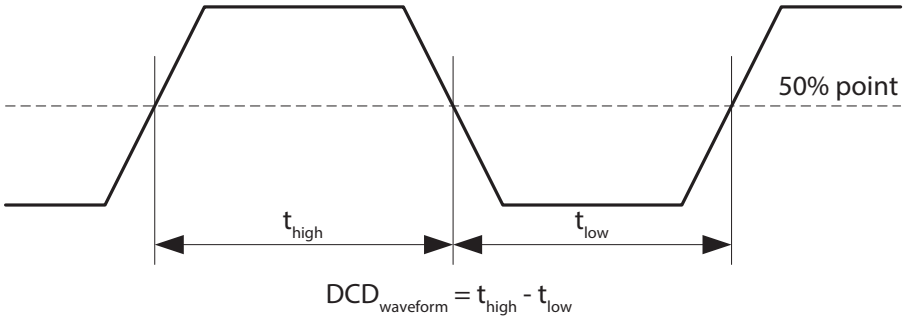


Figure 4-3: Traditional Waveform Definition of DCD

4.4 GPIO Controls

There are four configurable *GPIO* pins which can independently be configured as inputs or outputs. Each GPIO has a default function which can be re-configured through the host interface.

If there is a conflict between the internal register configuration of a given device function and the logic-level applied to a *GPIO* pin that is configured to control that same device function, the GPIO logic-level takes precedence over the internal register configuration. The logic HIGH and LOW levels of the *GPIO[3:0]* pin to which LOS is connected are specified by the EIA/JESD8-5A standard for 1.8V operation.

For a list of available functions and configuration details of *GPIO[3:0]*, please refer to the GPIO Configuration registers in Section 5.

4.5 GSPI Host Interface

The GS12081 is configured via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (*SDIN* pin), serial data output signal (*SDOUT* pin), an active-LOW chip select ($\overline{CS}$ pin) and a burst clock (*SCLK* pin).

The GS12081 is a slave device, so the SCLK, SDIN and $\overline{CS}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

4.5.1 $\overline{CS}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-LOW signal provided by the host processor to the GS12081.

The HIGH-to-LOW transition of this pin marks the start of serial communication to the GS12081.

The LOW-to-HIGH transition of this pin marks the end of serial communication to the GS12081.

Each device may use its own separate Chip Select signal from the host processor or up to 32 devices may be connected to a single Chip Select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the UNIT ADDRESS in GSPI Command Word 1 will respond to communication from the host processor (unless the B'CAST ALL bit in GSPI Command Word 1 is set to 1).

4.5.2 SDIN Pin

The *SDIN* pin is the GSPI serial data input pin of the GS12081.

The 32-bit Command and 16-bit Data Words from the host processor or from the SDOUT pin of other devices are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is LOW.

4.5.3 SDOUT Pin

The *SDOUT* pin is the GSPI serial data output of the GS12081.

All data transfers out of the GS12081 to the host processor or to the SDIN pin of other connected devices occur from this pin.

By default at power up or after system reset, the *SDOUT* pin provides a non-clocked path directly from the SDIN pin, regardless of the $\overline{CS}$ pin state, except during the GSPI Data Word portion for read operations from the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the *SDOUT* pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor or other downstream connected device on the subsequent SCLK rising edge.

4.5.3.1 GSPI Link Disable Operation

It is possible to disable the direct SDIN to SDOUT (Loop-Through) connection by writing a value of 1 to the **GSPI_LINK_DISABLE** bit in **CONTROL_REG**. When disabled, any data appearing at the *SDIN* pin will not appear at the *SDOUT* pin and the *SDOUT* pin is HIGH.

Note: Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.