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Bidirectional 12G UHD-SDI Re-timing Adaptive Cable Equalizer/Cable Driver

Key Features

- Single bidirectional 75 Ω cable interface with on-chip termination
- SMPTE ST 2082-1, ST 2081-1, ST 424, ST 292-1 and ST 259 compliant input/output
- Multi-standard operation from 1Mb/s to 11.88Gb/s
- Supports re-timing for DVB-ASI at 270Mb/s and MADI at 125Mb/s
- 3D Input Signal Eye Monitor
- PRBS Generator and Checker
- Automatic cable equalization. Typical equalized cable lengths of Belden 1694A cable:
 - 60m at 11.88Gb/s
 - 65m at 5.94Gb/s
 - 160m at 2.97Gb/s
 - 240m at 1.485Gb/s
 - 400m at 270Mb/s

Cable Equalizer Mode Features:

- Manual or automatic power-down on loss of signal
- Programmable carrier detect with squelch threshold adjustment
- Manual and automatic Cable Equalizer bypass

Cable Driver Mode Features:

- Wide swing control
- Pre-emphasis to compensate for significant insertion loss between device output and BNC
- Manual or automatic power-down on loss of signal
- Manual or automatic Mute or Disable on LOS

Trace Equalizer Features:

- Integrated 100Ω , differential input termination
- Manual or automatic power-down on loss of signal
- Adjustable carrier detect threshold
- DC-coupling from 1.2V to 2.5V CML logic
- Trace Equalization to compensate for up to 20" FR4 at 11.88Gb/s
- Automatic input offset compensation

Trace Driver Features:

- Integrated 100Ω , differential output termination
- DC-coupling from 1.2V to 2.5V CML logic
- Trace Driver data output pre-emphasis to compensate for up to 20" FR4 at 11.88Gb/s
- Manual or automatic Mute or Disable on LOS

CDR features:

- Manual or automatic rate modes
- Manual or automatic Re-timer Bypass
- Wide-range Loop Bandwidth control
- Re-timing at the following data rates: 125Mb/s, 270Mb/s, 1.485Gb/s, 2.97Gb/s, 5.94Gb/s, and 11.88Gb/s. This includes the f/1.001 rates.

Additional Features:

- Single 1.8V power supply for analogue and digital core
- 2.5V for Cable Driver output supply
- 1.2V, 1.8V, or 2.5V for Trace Driver output supply
- GSPI serial control and monitoring interface
- Four configurable GPIO pins for control or status monitoring
- Wide operating temperature range: -40°C to +85°C
- Small 6mm x 4mm 40-pin QFN
- Pb-free/Halogen-free/RoHS & WEEE compliant package
- Pin compatible with the GS3590

Applications

Next-generation 12G UHD-SDI infrastructures designed to support UHDTV1, UHDTV2, 4K D-Cinema and 3D HFR and HDR production image formats. Typical applications: Cameras, Switchers, Distribution Amplifiers and Routers.

Description

The GS12090 is a low-power, configurable multi-rate re-timing Cable Equalizer/Cable Driver supporting rates up to 12G UHD-SDI. It can be configured to equalize or drive signals over 75Ω coaxial cable. It includes DC restoration to compensate for the DC content of SMPTE pathological test patterns. Since the GS12090 is a re-timing device, extremely low output jitter is achievable even at extended cable/trace lengths.

The integrated Eye Monitor provides non-disruptive mission mode analysis of the post-equalized input signal. The 256x128 resolution scan matrix allows accurate signal analysis to speed-up prototyping and enable field analysis.

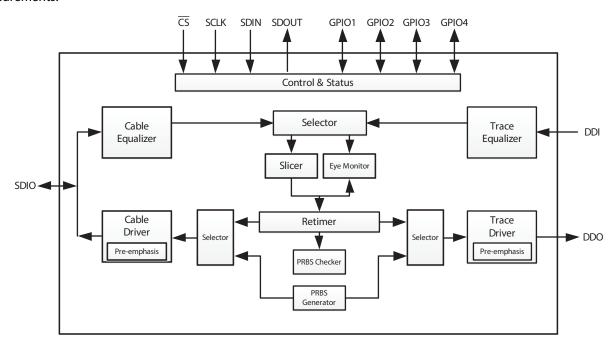
Built-in macros enable customizable cross section analysis and quick horizontal and vertical eye opening measurements.

With high phase consistency between scans and configurable space and time thresholds, algorithms can be deployed in the field to analyse long-term signal quality variation (Bathtub Plot) to reduce costly system installation debug time for intermittent errors.

Each output has highly configurable pre-emphasis and swing controls to compensate for long trace and connector losses.

Additionally, automatic and user selectable output slew rate control is provided for the Cable Equalizer output.

The GS12090 is pin compatible with the GS3590 Bidirectional 3G-SDI Re-timing Adaptive Cable Equalizer/Cable Driver.



GS12090 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
6	038491	_	September 2017	Updated values in Table 2-2 and Table 2-3
5	037880	_	July 2017	Added Section 4.8.4.
4	037328	_	June 2017	Updated Section 4.10.13, and added Section 4.10.12.
3	036215	_	April 2017	Updated Functional Block Diagram, Table 2-2, Table 2-3, Section 4.6, Section 4.8.5.1, Section 5.1, Section 5.2, Section 5.3, Section 7. Added Section 4.2.3.1, Section 4.2.3.2
2	034023	_	December 2016	Updates as described in the GS12090 Errata (PDS-061439, ECO-034371)
1	031348	_	October 2016	Changes throughout entire document.
0	029599	_	March 2016	New Document.

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1. Pin Out

1.1 GS12090 Pin Assignment

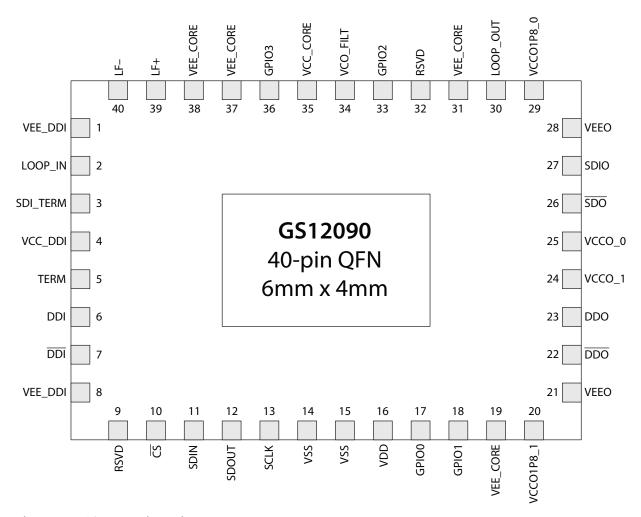


Figure 1-1: GS12090 Pin Assignment

1.2 GS12090 Pin Descriptions

Table 1-1: GS12090 Pin Descriptions

Pin Number	Name	Туре	Description
1,8	VEE_DDI	Power	Most negative power supply connection for the Cable Equalizer and Trace Equalizer. Connect to ground.
2	LOOP_IN	Input	Single-ended CML input with internal 75 Ω termination. Connect to LOOP_OUT (pin 30) through a capacitor (see Section 6.1 Typical Application Circuit for recommended values).
3	SDI_TERM	_	Input Common Mode termination. Decouple to ground (see Section 6.1 Typical Application Circuit for recommended values).
4	VCC_DDI	Power	Most positive power supply connection for the Trace and Cable Equalizer. Connect to 1.8V.
5	TERM	_	Input Common Mode termination. Decouple to ground (see Section 6.1 Typical Application Circuit for recommended values).
6, 7	DDI, DDI	Input	Serial digital differential input. Differential CML input with internal 100Ω termination.
9, 32	RSVD	_	These pins may be left floating. Please contact your Semtech FAE fo additional information on circuit compatibility with the GS12090.
10	टड	Digital Input	Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. $1.8V\ CMOS\ input\ with\ 100k\Omega\ pull-up.$ Active-low input. $Refer\ to\ Section\ 4.10.1\ for\ more\ details.$
11	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with $100k\Omega$ pull-down. Refer to Section 4.10.2 for more details.
12	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS output. Refer to Section 4.10.3 for more details.
13	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with $100k\Omega$ pull-down. Refer to Section 4.10.4 for more details.
14, 15	VSS	Power	Most negative power supply for digital core logic. Connect to ground.
16	VDD	Power	Most positive power supply connection for digital core logic. Connect to 1.8V.

Table 1-1: GS12090 Pin Descriptions (Continued)

Pin Number	Name	Туре	Description
17	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Default function: Direction = Output Signal = High indicates LOS (Loss of Signal, inverse of Carrier Detect) Pin is 1.8V CMOS I/O, please refer to GPIOO_CFG for more information on how to configure GPIOO.
18	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Default function: Direction = Output Signal = High indicates PLL is locked Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1.
19, 31, 37, 38	VEE_CORE	Power	Most negative power supply connection for the analogue core. Connect to ground.
20	VCCO1P8_1	Power	Most positive power supply connection for Trace Driver pre-driver. Connect to 1.8V.
21, 28	VEEO	Power	Most negative power supply connection for the output drivers. Connect to ground.
22, 23	DDO, DDO	Output	Differential CML output with two internal 50Ω pull-ups. In cable equalizer mode, the data signal or PRBS Generator can be selected for this output.
24	VCCO_1	Power	Most positive power supply connection for the DDO/ $\overline{\text{DDO}}$ output driver. Connect to 1.2V – 2.5V.
25	VCCO_0	Power	Most positive power supply connection for the SDIO/SDO output driver. Connect to 2.5V.
26	SDO	Output	Single-ended CML output buffer with internal 75 Ω pull-up. Decouple to ground (see Section 6.1 Typical Application Circuit for recommended values).
27	SDIO	Output	Single-ended bidirectional CML buffer with internal 75 Ω pull-up. In cable driver mode, the data signal or PRBS Generator can be selected for this output.
29	VCCO1P8_0	Power	Most positive power supply connection for Cable Driver pre-driver. Connect to 1.8V.
30	LOOP_OUT	Output	Single-ended CML output. Connect to LOOP_IN (pin 2) through a capacitor (see Section 6.1 Typical Application Circuit for recommended values).

Table 1-1: GS12090 Pin Descriptions (Continued)

Pin Number	Name	Туре	Description
33	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. Default function: Direction = Input Signal = Set HIGH to put device in sleep Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2.
34	VCO_FILT	Passive	VCO filter capacitor connection. Decouple to ground. See Section 6.1 Typical Application Circuit for recommended values.
35	VCC_CORE	Power	Most positive power supply connection for the analogue core. Connect to 1.8V.
36	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Default function: Direction = Input Signal = Set HIGH to put device in cable driver mode Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3.
39	LF+	Passive	Loop filter capacitor connection. Connect to pin 40 through a capacitor (see Section 6.1 Typical Application Circuit for recommended values).
40	LF-	Passive	Loop filter capacitor connection. Connect to pin 39 through a capacitor (see Section 6.1 Typical Application Circuit for recommended values).
Tab	_	_	Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation. It is not recommended to connect the device ground pins to the central paddle.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter		Value
Supply Voltage—Core (V _{CC_DDI} , V _{CC_CORE} , V _{DD})		-0.5V to +2.2V
Supply Voltage—Output Driver	V _{CCO_0}	-0.5V to +2.8V
Supply voltage—Output Driver	V _{CCO_1}	-0.5V to +2.8V
Input ESD Voltage (any pin)		3kV HBM
Storage Temperature Range (T _S)		-50°C to +125°C
Input Voltage Range (SDIO)		-0.3 to (V _{CCO_0} + 0.3)V
Input Voltage Range (GPIO2, GPIO3)		-0.3 to (V _{CC_CORE} + 0.3)V
Input Voltage Range (CS, SDIN, SCLK, VSS, VDD, GPIO0, GPIO1)		-0.3 to (V _{DD} +0.3)V
Solder Reflow Temperature		260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

 $T_A = -40$ °C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Тур	Max	Units	Notes
	Bi-Directio	nal Characteristics (Applicable	to Both Mo	des)			
Supply Voltage	V_{CC_DDI} , V_{CC_CORE} , V_{DD}	_	1.71	1.8	1.89	٧	_
DDI Input and DDO Output Termination		Differential	_	100	_	Ω	_
SDIO Bi-directional Termination		Between SDIO and GND	_	75	_	Ω	_
SDO Output Termination		Between SDO and GND	_	75	_	Ω	_
		CDR Unlocked During Rate Search	_	182	_	mA	_
Supply Current—	I _{CC_CORE}	PRBS Generator Enabled	_	119	es) 1.8 1.89 V 100 — Ω 75 — Ω 75 — Ω 182 — mA	2, 3	
Analogue Core		PRBS Checker Enabled	_	60	_	mA	2
		Eye Monitor Enabled	_	54	_	mA	2
Supply Current— Digital Logic	I _{DD}	_	_	16	20	mA	_
Input Voltage—Digital Pins	V _{IH}	_	0.65* V _{DD}	_	V_{DD}	V	_
$(\overline{CS}, SDIN, SCLK, GPIO[0:3])$	V_{IL}	_	0	_		٧	
Output Voltage—Digital Pins	V _{OH}	I _{OH} = -5mA	VDD - 0.45	- 16 20 mA 55*	_		
(SDOUT, GPIO[0:3])	V _{OL}	$I_{OL} = +5mA$	_	_	0.45	V	_
	(Cable Equalizer Mode Characte	ristics				
			1.14	1.2	1.26	V	
Supply Voltage—Trace Driver	—Trace V _{CCO_1}		1.71	1.8	1.89	V	_
			2.38	2.5	2.63	V	_

Table 2-2: DC Electrical Characteristics (Continued)

 $T_A = -40$ °C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Тур	Max	Units	Notes
		$V_{CCO_{1}} = 1.2V$, Output Swing = 400mV_{ppd} , DDO/ \overline{DDO} enabled	_	430	_	mW	1
		$V_{CCO_1} = 1.8V$, Output Swing = 400mV_{ppd} , DDO/ \overline{DDO} enabled	_	440	_	mW	1
Power	P_{D}	$V_{CCO_{1}} = 1.8V$, Output Swing = 800mV_{ppd} , DDO/ \overline{DDO} enabled	_	455	_	mW	1
		$V_{CCO_{1}} = 2.5V$, Output Swing = 400mV_{ppd} , DDO/ \overline{DDO} enabled	_	445	_	mW	1
		$V_{CCO_{1}} = 2.5V$, Output Swing = 800mV_{ppd} , DDO/ \overline{DDO} enabled	_	470	_	mW	1
		$V_{CCO_1} = 1.2V$, Output Swing = 400mV_{ppd}	_	10	17	mA	1
		$V_{CCO_{1}} = 1.8V$, Output Swing = 400mV_{ppd}	_	10	17	mA	1
Supply Current—Trace Driver	I _{CCO_1}	$V_{CCO_1} = 1.8V$, Output Swing = 800mV_{ppd}	_	20	30	mW mW mW mA mA mA mA mA mA mA	1
		$V_{CCO_1} = 2.5V$, Output Swing = 400mV_{ppd}	_	10	17	mA	1
		$V_{CCO_1} = 2.5V$, Output Swing = 800mV_{ppd}	_	20	30	mA	1
Supply Current — Trace Driver Pre Driver	I _{CCO_1P8_1}	Output Swing = 800mV _{pp}	_	25	32	mA	_
Supply Current — V _{CCO_0}	I _{CCO_0}	$V_{CCO_0} = 2.5V$, Output Swing = 800mV_{ppd}	_	13	18	mA	_
Supply Current— Cable Equalizer	I _{CC_SDI}	_	_	55	75	mA	_
Supply Current— Analogue Core	I _{CC_CORE}	CDR Locked to Rate	_	125	161	mA	_
DDO Output Common Mode Voltage	V _{CMOUT}	-	_	$V_{CMOUT} = V_{CCO_1} - \Delta V_{DDO} / 2$	_	V	_

Table 2-2: DC Electrical Characteristics (Continued)

 $T_A = -40$ °C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Тур	Max	Units	Notes
		Cable Driver Mode Characteris	stics				
Supply Voltage — Cable Driver	V_{CCO_0}	_	2.38	2.5	2.63	V	_
		$V_{CCO_0} = 2.5V$, Output Swing = 800mV_{pp} , DDO/ \overline{DDO} disabled	_	375	_	mW	1
Power	P _D	$V_{CCO_0} = 2.5V$, Output Swing = 800mV_{pp} with max pre-emphasis, DDO/ \overline{DDO} disabled	_	390	_	mW	_
		$V_{CCO_0} = 2.5V$, Output Swing = 800mV_{pp}	_	25	36	mA	1
Supply Current— Cable Driver	I _{CCO_0}	$V_{CCO_0} = 2.5V$, Output Swing = 800mV_{pp} , with max pre-emphasis	_	30	38	V mW	_
Supply Current — Cable Driver Pre Driver	I _{CCO1P8_0}	Output Swing = 800mV _{pp}	_	20	30	mA	_
Supply Current— Analogue Core	I _{CC_CORE}	CDR Locked to Rate	_	120	164	mA	_
Supply Current — Trace Equalizer	I _{CC_DDI}	_	_	20	32	mA	_
DDI Input Common Mode Voltage	V _{CMIN}	_	0.94	V _{CC_DDI} - 0.1V	2.525	٧	4
		Sleep Mode					
Sleep		Cable Equalizer mode		80		mW	
Sleep		Cable Driver mode	_	45	_	mW	_

Notes:

- 1. Pre-emphasis is disabled.
- 2. Current listed is an increase to $I_{\mbox{\footnotesize CC_CORE}}$ when stated condition is true.
- 3. Selected clock source = VCO free running.
- 4. When the Trace Equalizer is AC-coupled, the input common mode is V_{CC_DDI} 0.1V. 0.94V is the worst case when the Trace Equalizer is DC-coupled to upstream driver running from 1.2V supply. 2.525V is the worst case when the Trace Equalizer is DC-coupled to upstream driver running from 2.5V supply.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

 $V_{CC_DDI}, V_{CC_CORE}, V_{DD} = +1.8V \pm 5\% \ and \ V_{CCO_0}, V_{CCO_1} = +2.5V \pm 5\%, T_A = -40^{\circ}C \ to \ +85^{\circ}C, unless \ otherwise \ shown.$

Parameter	Symbol	Conditions	Min	Тур	Max	Units	Notes
	Bi-Directional (Characteristics (Applicable	to Both Mod	es)			
Serial Input Data Rate	DR _{DDI} , DR _{SDIO}	_	0.001	_	11.88	Gb/s	12
erial Input Data Rate eturn Loss LL Loop Bandwidth (for 0.2UI		5MHz to 1.485GHz	_	_	-17	dB	1
		1.485GHz to 2.97GHz	_	_	-12	dB	1
Return Loss		2.97GHz to 5.94GHz	_	_	-8	dB	1
		5.94GHz to 11.88GHz	_	_	-5	dB	1
		Setting 0.0625x	_	5	_	kHz	5
		Setting 0.125x	_	10	_	kHz	5
	BW _{LOOP(125Mb/s)}	Setting 0.25x	_	19	_	kHz	5
		Setting 0.5x (Default)	_	38	_	kHz	5
		Setting 1.0x	_	75	_	B Gb/s dB dB dB dB kHz kHz	5
-		Setting 0.0625x	_	10	_	kHz	5
		Setting 0.125x	_	20	_	kHz	5
	BW _{LOOP(270Mb/s)}	Setting 0.25x	_	40	_	kHz	5
		Setting 0.5x	_	80	_	kHz	5
		Setting 1.0x (Default)	_	158	_	kHz	5
-	BW _{LOOP(1.485Gb/s)}	Setting 0.0625x	_	55	_	kHz	5
		Setting 0.125x	_	110	_	kHz	5
		Setting 0.25x	_	220	_	kHz	5
		Setting 0.5x (Default)	_	438	_	kHz	5
PLL Loop Bandwidth (for 0.2UI		Setting 1.0x	_	875	_	B Gb/s dB dB dB kHz	5
jitter and 50% edge density)		Setting 0.0625x	_	110	_		5
		Setting 0.125x	_	220	_		5
	BW _{LOOP(2.97Gb/s)}	Setting 0.25x	_	440	_	kHz	5
		Setting 0.5x (Default)	_	0.88	_	MHz	5
		Setting 1.0x	_	1.75	_	Gb/s dB dB dB kHz kHz kHz kHz kHz kHz kHz kH	5
-		Setting 0.0625x	_	220	_	kHz	5
		Setting 0.125x	_	440	_	kHz	5
	BW _{LOOP(5.94Gb/s)}	Setting 0.25x	_	0.88	_	MHz	5
		Setting 0.5x (Default)	_	1.75	_	MHz	5
		Setting 1.0x	_	3.5	_	MHz	5
·		Setting 0.0625x		440		kHz	5
		Setting 0.125x	_	0.88	_	MHz	5
	BW _{LOOP(11.88Gb/s)}	Setting 0.25x	_	1.75	_	MHz	5
		Setting 0.5x (Default)	_	3.5	_	MHz	5
		Setting 1.0x	_	7.0	_	MHz	5

Table 2-3: AC Electrical Characteristics (Continued)

 $V_{CC_DDI}, V_{CC_CORE}, V_{DD} = +1.8V \pm 5\% \text{ and } V_{CCO_0}, V_{CCO_1} = +2.5V \pm 5\%, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise shown.}$

Parameter	Symbol	Conditions	Min	Тур	Max	Units	Notes
	Cabl	le Equalizer Mode Characteris	tics				
BNC Input Voltage Swing	V_{SDIO}	_	720	800	880	mV _{pp}	3
Differential Output	41/	200mV	150	200	250	mV _{ppd}	7
Voltage Swing	$\Delta V_{ m DDO}$	800mV	600	800	1000	mV _{ppd}	8
DDO, DDO, Rise/Fall Time	t _{riseDDO} , t _{fallDDO}	All rates	_	_	40	ps	11
DDO Mismatch in Rise/Fall Time		_	_	_	8	ps	11
DDO Duty Cycle Distortion DDO, DDO		_	_	_	10	ps	_
PLL Lock Time— Asynchronous	t _{ALOCK}	_	_	75	_	ms	6
	t _{OJ(125Mb/s)}	Belden 1694A: 400m	_	0.02	0.1	UI	2
_	t _{OJ(270Mb/s)}	Belden 1694A: 400m	_	0.02	0.1	0 mV _{pp} 0 mV _{ppd} 0 mV _{ppd} 0 ps 0 ps 0 ps 0 ps 1 UI 1 UI 1 UI 1 UI 5 UI 5 UI 5 UI 6 mV _{ppd} 0 mV _{ppd} 0 mV _{ppd} 0 Inches 1 Inc	2
Serial Data Output Jitter (DDO) –	t _{OJ(1.485Gb/s)}	Belden 1694A: 240m	_	0.02	0.1		2
	t _{OJ(2.97Gb/s)}	Belden 1694A: 160m	_	0.04	0.1		2
	t _{OJ(5.94Gb/s)}	Belden 1694A: 65m	_	0.07	0.15	UI	2
	t _{OJ(11.88Gb/s)}	Belden 1694A: 60m	_	0.07	0.15	UI	2
	Cal	ble Driver Mode Characteristi	CS				
Differential Input Voltage Swing	ΔV_{DDI}	_	200	_	800	${\rm mV_{ppd}}$	_
BNC Output Voltage Swing	$V_{SDIO}, V_{\overline{SDO}}$	_	720	800	880	mV _{pp}	4
		12G	_	20	_	Inches	14dB, 9
		6G	_	30	_	Inches	12dB, 9
Input Trace Equalization		3G	_	60	_	mV _{pp} mV _{ppd} mV _{ppd} ps ps ps ps UI	13dB, 9
input fruce Equalization		HD	_	60	_	Inches	6dB, 9
		SD		60		Inches	3dB, 9
		MADI	_	60		mV _{pp} d mV _{ppd} mV _{ppd} ps ps ps ps UI	3dB, 9
Intrinsic Input Jitter Tolerance	IIJT	12G	0.7	0.85	_		_
		MADI/SD/HD/3G/6G	8.0	0.95	_	UI	_
PLL Lock Time—	t _{ALOCK}	Referenceless with MADI rate detection disabled	_	_	16.7	ms	6
Asynchronous	ALOCK	Referenceless with MADI rate detection enabled	_	_	32	ms	6
PLL Lock Time—Synchronous	t _{SLOCK}	SD	_	_	10	μs	6
	SLUCK	HD/3G/6G/12G	_	_	5	μs	6
		SD/MADI	400		1000	ps	_
SDIO, SDO Rise/Fall Time	$t_{riseSDIO}$, $t_{fallSDIO}$	HD/3G	_		70	ps	_
		6G/12G	_	_	40	ps	_

Table 2-3: AC Electrical Characteristics (Continued)

 $V_{CC_DDI}, V_{CC_CORE}, V_{DD} = +1.8V \pm 5\% \text{ and } V_{CCO_0}, V_{CCO_1} = +2.5V \pm 5\%, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise shown.}$

Parameter	Symbol	Conditions	Min	Тур	Max	Units	Notes
SDIO MI I		SD/MADI	_	_	100	ps	
SDIO Mismatch in Rise/Fall Time		HD/3G	_	_	20	ps	
		6G/12G	_	_	10	ps	
5DIO 5		SD/MADI	_	_	5	%	
SDIO Eye Cross Shift (SDIO, SDO)		HD/3G	_	_	8	%	_
(02.0) 02.0)		6G/12G	_	_	9	%	_
SDIO Overshoot		_	_	_	10	%	_
Serial Data Output Jitter (SDIO)	t _{OJ(125Mb/s)}	— BW = default, Pattern = PRBS	_	0.015	0.08	UI	2, 10
	t _{OJ(270Mb/s)}			0.035	0.08	UI	2, 10
	t _{OJ(1.485Gb/s)}			0.025	0.08	UI	2, 10
	t _{OJ(2.97Gb/s)}			0.04	0.08	UI	2, 10
	t _{OJ(5.94Gb/s)}			0.04	0.1	UI	2, 10
	t _{OJ(11.88Gb/s)}			0.1	0.16	UI	2, 10
	t _{OJ(Bypass)}			0.1	0.2	UI	2, 10

Notes:

- 1. Values achieved with Semtech evaluation board and connector.
- 2. Measured using a clean input source.
- 3. Default value for CFG_EQ_INPUT_LAUNCH_SWING_COMP parameter in control register 0x18. The default parameter value is 80_d (50_h).
- 4. Default Cable Driver swing Setting.
- 5. Please see PLL_LOOP_BANDWIDTH_0 for the full range of loop bandwidth settings.
- 6. Please see Section 4.4.3.1 for the further definition on Synchronous and Asynchronous Lock Time.
- 7. Output driver setting of 8.
- 8. Output driver setting of 36.
- 9. Trace insertion loss was measured with FR4 material using 7 mil strip-line traces using a PRBS23 signal.
- 10. Measured under minimal trace loss conditions.
- 11. Rise/fall time was measured between 80% and 20%.
- 12. When in Cable Equalizer Mode, the rise/fall time of signals at the source should not be more than 62ns.

Note: For GSPI Timing see Table 4-12: GSPI Timing Parameters.

3. Input/Output Circuits

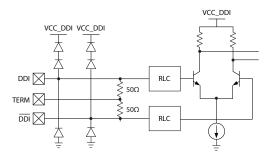


Figure 3-1: DDI, DDI

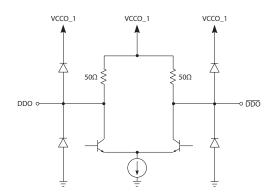


Figure 3-2: DDO/DDO

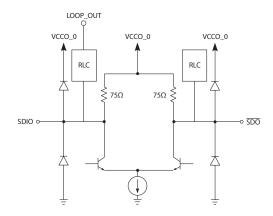


Figure 3-3: SDIO, SDO

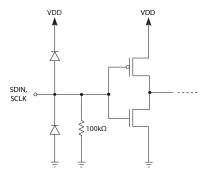


Figure 3-4: SDIN, SCLK

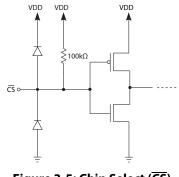


Figure 3-5: Chip Select (CS)

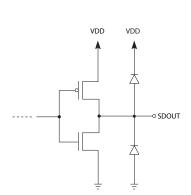


Figure 3-6: SDOUT

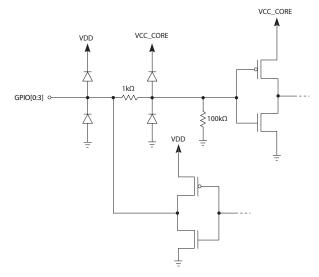


Figure 3-7: GPIO[0:3]

4. Detailed Description

4.1 Device Description

The GS12090 features a 75Ω internally-terminated bidirectional SDIO port, which can be set as SMPTE-compliant Cable Driver, or Cable Equalizer. In addition to the SDIO port, there is a 100Ω differential Trace Driver to transmit the incoming SDI signal to the system and a 100Ω differential Trace Equalizer to receive the outgoing signal from the system. The bidirectional mode can be controlled through the host interface, or the *GPIO* pin. The Cable Driver has amplitude and pre-emphasis control to compensate for significant insertion loss between device output and BNC. The Trace Driver also has amplitude and pre-emphasis control which can compensate for 15dB of insertion loss at 5.94GHz. The pre-emphasis control is two-dimensional in both the Cable Driver and Trace Driver, where both pre-emphasis pulse amplitude and width adjustments can be made to help optimize for interconnect mismatches such as vias and connectors. The Trace Equalizer has boost control, which can compensate for 17dB of insertion loss at 5.94GHz.

4.1.1 Bidirectional Mode Control

The bidirectional mode of the GS12090 can be controlled through the GPIO or the host interface.

By default the device is in pin control mode and *GPIO3* is the control input pin. To put the device in Cable Equalizer Mode drive this pin LOW. To put the device in Cable Driver Mode drive this pin HIGH.

In addition to GPIO control, the host can set the direction mode through the host interface using the **CTRL_DIRECTION_SEL_MODE** and **CTRL_DIRECTION_SEL** parameters in register 0x14. To use the host interface to control the direction mode, first choose host interface select mode by writing 1_b to **CTRL_DIRECTION_SEL_MODE** (default = 0_b pin mode). Once the device is in host interface select mode, the host can put the device in cable equalizer mode by writing 0_b to the **CTRL_DIRECTION_SEL** control parameter (default = 1_b cable driver mode).

4.1.2 Sleep Mode

To enable low-power operation, the GS12090 has Manual and Automatic Sleep Mode control.

The default mode is Automatic Sleep Mode on LOS (Loss Of Signal). The device can also be manually put into Sleep Mode. When the device is in Sleep Mode, all the core blocks are powered-down, except the host interface and carrier detect circuits. The SDIO Cable Driver output buffer is always disabled (powered-down) in sleep mode, while the DDO Trace Driver can be disabled or muted.

The CTRL_AUTO_SLEEP and CTRL_MANUAL_SLEEP parameters in register 0x3, control the sleep mode of the device. The default value of the CTRL_AUTO_SLEEP parameter is 1_b (Auto Sleep). While in Auto Sleep Mode, the CTRL_MANUAL_SLEEP parameter has no effect. To enable host control of the sleep mode, set the CTRL_AUTO_SLEEP parameter to 0_b for Manual Sleep Control. To prevent the device from entering sleep, set the CTRL_MANUAL_SLEEP parameter to 0_b (not sleep). To manually configure the device to sleep, set the CTRL_MANUAL_SLEEP parameter to 0_b (sleep).

The device can also be manually made to sleep through the *GPIO* pins. The default *GPIO* pin to control sleep is *GPIO2* (pin 33). Drive this pin HIGH to make the device sleep.

Section 4.7 describes the PRBS Generator function. If the device's PRBS Generator is intended to be used without a valid input signal, the device should be manually set to not sleep as described above. Without a valid input signal, an LOS status will be generated and the device will enter sleep mode and the PRBS block will be disabled. For a description of LOS thresholds and settings, see Section 4.2.3 and Section 4.3.2.

4.2 Cable Equalizer

When the GS12090 is operating in Cable Equalizer Mode, it can automatically adjust its gain to equalize and restore SMPTE-compliant signals received over different lengths of coaxial cable having loss characteristics similar to Belden 8281 or 1694A. With the default settings, the device will automatically equalize MADI at 125Mb/s and most common SMPTE compliant signals between SD at 270Mb/s and UHD-SDI at 11.88Gb/s and bypass signals below 125Mb/s.

The GS12090 features programmable Launch Swing Compensation, Squelch Threshold Adjust, and Bypass, all of which can be set through the device's host interface.

The equalized or bypassed signal is then routed to the serial digital re-timer (CDR) block.

4.2.1 Cable Equalizer Bypass

With the default settings, the device will automatically bypass signals below 125Mb/s. During Equalizer Bypass Mode, the device supports low data rate and slow edge signals such as SMPTE310 and AES3id. The rise/fall times must not exceed 62ns. These signals will not be re-timed by the CDR block. The following two methods allow the user to force the signal to bypass the equalization and DC restoration stages:

- 1. Via the host interface, by setting CTRL_CEQ_AUTO_BYPASS to 0_b , and CTRL_CEQ_MANUAL_BYPASS to 1_b in register 0x17.
- 2. Via the GPIO[0:3] pin (see Section 4.9).

4.2.2 Upstream Launch Swing Compensation

The GS12090 Cable Equalizer has an automatic gain control circuit, that is optimized on the assumption that the Cable Driver in the upstream device is SMPTE-compliant and has a launch swing of $800 \text{mV}_{pp} \pm 10\%$. When the source amplitude is known to be non-SMPTE compliant, a compensation adjustment can be made in the GS12090. The GS12090 can adjust for launch swings in the range of 250mV to 1V in approximately 50mV_{ppd} increments. Upstream launch swing compensation can be adjusted through the **CFG_EQ_INPUT_LAUNCH_SWING_COMP** parameter in control register 0x18. The default parameter value is 80_{d} (50_{h}), which corresponds to a nominal launch swing of 800mV_{ppd} .

4.2.3 Carrier Detect, Squelch Control, and Loss of Signal

The GS12090 Cable Equalizer has highly-configurable carrier detection and squelching capability. The carrier detection can be made more robust against spurious signals and noise at the inputs and the squelch control can be configured and enabled to reduce false outputs to low level signals such as crosstalk.

The GS12090 reports two separate carrier detect parameters—**STAT_PRI_CD** and **STAT_SEC_CD**. They are described in Section 4.2.3.1 and Section 4.2.3.2 respectively.

Note: The parameters referred to within Section 4.2.3 to Section 4.2.3.2 are linked to their respective registers in Table 4-1.

4.2.3.1 Primary Carrier Detection (STAT_PRI_CD) Configuration

Primary carrier detection (**STAT_PRI_CD**) can be configured for higher stability by filtering-out longer transients or glitches. This can be achieved by increasing the sampling window over which the signal is sampled and the number of samples required to assert or de-assert it.

There are three configuration parameters that control assertion or de-assertion of **STAT PRI CD**:

- CFG CD FILTER SAMPLE WIN
- CFG_FILTER_DEASSERT_CNT
- CFG_CD_FILTER_ASSERT_CNT

See Figure 4-1 for a visual representation of the **STAT_PRI_CD** configuration parameters.

With the default values in place:

- An assertion (setting HIGH) of STAT_PRI_CD will take place after a valid signal is present for ~6.5ms
- A de-assertion (setting LOW) of STAT_PRI_CD will take place after loss of a valid signal for ~96ms

If the application requires any adjustment of the sampling window, assertion count, or de-assertion count, please consult the following equations to calculate the associated time to assert or de-assert **STAT_PRI_CD**.

STAT_PRI_CD de-assert time:

• (1.6µs) * (CFG_CD_FILTER_SAMPLE_WIN + 1) * CFG_CD_FILTER_DEASSERT_CNT

STAT PRI CD assert time:

(1.6μs) * (CFG_CD_FILTER_SAMPLE_WIN + 1) * CFG_CD_FILTER_ASSERT_CNT

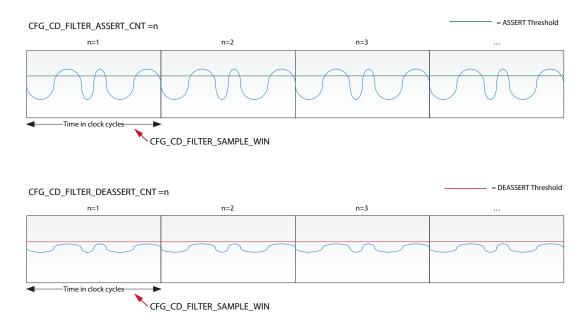


Figure 4-1: STAT_PRI_CD Configuration Parameters

4.2.3.2 Secondary Carrier Detection (STAT_SEC_CD) Configuration

The secondary carrier detection signal acts as an additional carrier detection which can be further filtered through squelch controls. It also serves as the control signal for Mute on LOS (Loss Of Signal) and Disable on LOS. Please refer to Section 4.8.7 to Section 4.8.7.3 for further information on this.

If the application requires the use of squelch settings, start by setting the following:

• CFG_SEC_CD_INCL_CLI_SQUELCH = 1

Once this parameter is set, the device will apply squelch based on the settings found within the following parameters:

- CFG_CLI_SQUELCH_THRESHOLD
- CFG_CLI_SQUELCH_HYSTERESIS

The device will use these parameters to determine squelch status and set that within **STAT_CLI_SQUELCH**. Based off of this, secondary carrier detection can be described as:

• STAT_SEC_CD = inverse of (STAT_CLI_SQUELCH & STAT_PRI_CD).

To help detail how the device determines the state of Squelch, we define the following variables:

- CLI = STAT_CABLE_LEN_INDICATION
- THR = CFG CLI SQUELCH THRESHOLD
- HYS = CFG_CLI_SQUELCH_HYSTERESIS
- SQL = STAT_CLI_SQUELCH

The following rules define the state of SQL.

Note: If the cable equalizer is in bypass (**STAT_CEQ_BYPASS** = 1), the device will set SQL to 0.

- If CLI > (THR + HYS), the device will set SQL to 1, otherwise:
- If CLI < (THR HYS), the device will set SQL to 0, otherwise:
- If CLI ≥ (THR HYS) and CLI ≤ (THR + HYS), SQL remains unchanged.
- If SQL = 1, the device will not indicate lock and the trace driver state will be defined by output state control parameters settings, see Section 4.8.7 for more details.

Table 4-1: Cable Equalizer Status and Configuration Parameters

Register Address _h and Name	Parameter Name	Parameter Description		
15, CARR_ DET_CFG	CFG_SEC_CD_INCL_CLI_SQUELCH	Enables or disables squelch control.		
16, SQUELCH_ PARAMETERS	CFG_CLI_SQUELCH_THRESHOLD	Used to tune the squelch threshold based on the tolerance requirements of the application.		
	CFG_CLI_SQUELCH_HYSTERESIS	Used to tune the squelch hysteresis based on the tolerance requirements of the application.		
20, CD_FILTER_ DELAYS_0	CFG_CD_FILTER_SAMPLE_WIN	Primary carrier detect sampling window size.		
21, CD_FILTER_ DELAYS_1	CFG_CD_FILTER_DEASSERT_CNT	Primary carrier detect de-assertion count.		
22, CD_FILTER_ DELAYS_2	CFG_CD_FILTER_ASSERT_CNT	Primary carrier detect assertion count.		
84, STICKY_COUNTS_0	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.		
	STAT_CNT_SEC_CD_CHANGES	A counter showing the number of times the secondary Carrier Detect signal changed.		
86, CURRENT_ STATUS_0	STAT_CLI_SQUELCH	Cable equalizer Squelch status.		
OZ CURRENT STATUS 1	STAT_PRI_CD	Primary filtered carrier detect of the analogue carrier detect signal.		
87, CURRENT_STATUS_1	STAT_SEC_CD	Secondary filtered carrier detect of the analogue carrier detect signal.		
88, EQ_GAIN_IND	STAT_CABLE_LEN_INDICATION	SDIO cable length indication when in cable equalizer mode.		

4.3 Trace Equalizer

The GS12090 features a differential input buffer with 100Ω differential input termination, which includes a Trace Equalizer that can be configured to compensate for up to 20" of 7mil strip-line in FR4 at 11.88Gb/s and up to 60" at 2.97Gb/s.

Note: The parameters referred to within Section 4.3 to Section 4.3.2 are linked to their respective registers in Table 4-2.

The differential input signal can be either DC-coupled or AC-coupled, and is capable of operation with any binary coded signal between 1Mb/s and 11.88Gb/s.

The input circuit is compatible with industry standard CML differential transmitters when DC-coupled using industry standard 100Ω differential termination circuitry.

The Trace Equalizer includes an automatic input offset compensation circuit. This reduces offset-induced data jitter in the link due to asymmetric performance of DC-coupled upstream differential drivers. The input offset compensation circuit also improves the input sensitivity of the Trace Equalizer.

4.3.1 Input Trace Equalization

The Trace Equalizer can compensate for up to 17dB of insertion loss at 5.94GHz in 8 increments, which can be adjusted through the **CFG_TREQ0_BOOST** parameter in control register 0x1E. The default value of **CFG_TREQ0_BOOST** is (0_h), which corresponds to the minimum equalization boost level.

Please refer to Figure 4-2 for recommended boost setting.

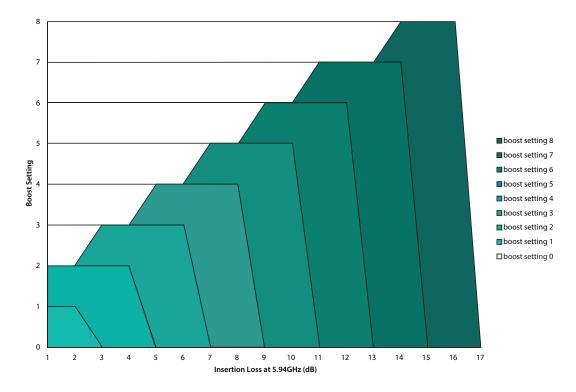


Figure 4-2: GS12090 Trace EQ Boost Setting Recommendation

By default at power up or after system reset, the trace equalizer is configured to compensate for up to 3" of 7mil strip-line in FR4 material at high-frequencies.

Note: Although not a requirement, launch swing of 800mV_{ppd} is recommended for trace lengths longer than 5".

4.3.2 CD (Carrier Detect) and LOS (Loss of Signal)

LOS is the complement of CD and is used by various automatic control modes including mute on LOS, which will be covered in the output section of this document.

The default settings of the Trace Equalizer Carrier Detection sub-block should satisfy most applications; however the Carrier Detection mechanism in the Trace Equalizer is highly-configurable and allows the system designer to optimize the sensitivity and hysteresis of Carrier Detection mechanism to meet specific system requirements.

The trace equalizer Carrier Detect is reported by status parameter **STAT_PRI_CD** in register 0x87.

The first CD control parameter is $\mathbf{CFG_TREQ0_CD_BOOST}$ in register 0x1E. This parameter determines the method and therefore the level of equalization to be used on the input signal routed to the Carrier Detection sub-block. The default value is $0_{\rm b}$, which maximizes the level of equalization. Alternatively, the designer can choose to have this signal equalized at the same level as the main signal routed to the CDR by setting $\mathbf{CFG_TREQ0_CD_BOOST}$ to $1_{\rm b}$. The setting of this parameter has no impact on the main signal routed to the CDR.

The last two CD control parameters can be found in register 0x1F. Parameters CFG_TREQ0_CD_ASSERT_THRESH and CFG_TRE0Q_CD_DEASSERT_THRESH set the Carrier Detect assert and de-assert thresholds to the input signal, which also defines the hysteresis of CD signal.

The default values of **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TREQ0_CD_DEASSERT_THRESH** are 4_d and 3_d respectively. With the default settings, the minimum launch swing needed to assert the carrier detect is 200mV and it will be de-asserted when the signal level falls below 150mV.

The **STAT_PRI_CD** (Carrier Detect) parameter will be set to 0_b and the LOS will be set to 1_b whenever a new signal at the input does not exceed the assert threshold, or an existing signal falls below the de-assert threshold. The result is that the device will not indicate lock, and the outputs will mute (assuming Mute on LOS is left to its default value in the **CONTROL_OUTPUT_MUTE** register—0x49). See Section 4.8.7 for more details.

Given a differential input trace with 17dB of insertion loss at 5.94GHz and $\mathbf{CFG_TREQ_CD_BOOST} = 0_{br}$, Figure 4-3 illustrates the relationship between launch swing voltage, and minimum threshold setting to assert or de-asset Carrier Detect at all rates up to threshold setting at 11.88Gb/s.

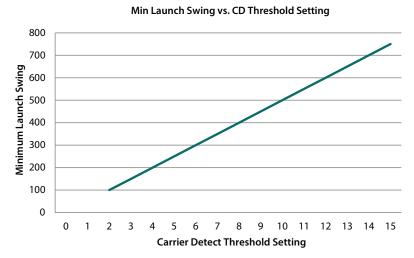


Figure 4-3: Input Voltage Vs. Carrier Detect Threshold Setting

Table 4-2: Trace Equalizer Status and Configuration Parameters

Register Address _h and Name	Parameter Name	Description		
84, STICKY_ COUNTS_0	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.		
87, CURRENT_ STATUS_1	STAT_PRI_CD	Primary filtered carrier detect of the analogue carrier detect signal.		
1F, TREQ0 CD HYSTERESIS	CFG_TREQ0_CD_ASSERT_THRESH	Sets the Carrier Detect assert threshold.		
IF, INEQU_CD_ HTSTERESIS	CFG_TREQ0_CD_DEASSERT_THRESH	Sets the Carrier Detect de-assert threshold.		
1E, TREQ0 INPUT BOOST	CFG_TREQ0_BOOST	Sets the Trace Equalizer boost level.		
TE, INEQU_INFOT_BOOST	CFG_TREQ0_CD_BOOST	Selects the boost method of the CD signal.		

4.4 Serial Digital Re-timer (CDR)

The GS12090 includes an integrated CDR, whose purpose is to lock to a valid incoming signal from the Cable Equalizer stage (when operating in cable equalizer mode) or the Trace Equalizer stage (when operating in cable driver mode) and produce a lower jitter signal at the Cable Driver or Trace Driver outputs. The CDR has the ability to lock to any of the following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), 3G-SDI (2.97Gb/s), 6G-SDI (5.94Gb/s) and 12G-SDI (11.88Gb/s). This includes the f/1.001 rates.

The default settings of the re-timer block are optimal for most applications. However, the following controls allow the user to customize the behaviour of the re-timer: LBW control, Automatic and Manual Rate Detection.

Note: The parameters referred to within Section 4.4.1 to Section 4.4.2 are linked to their respective registers in Table 4-4: CDR Control and Status Parameters. For a complete list of registers and functions, please see Section 5.