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GS1500M

802.11 b/g/n
LOW-POWER
WI-FI MODULE

DATA SHEET

Reference: GS1500M-DS
Version: SP-1.4
Date: November 2014

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1 Overview

1.1 Document Overview

THIS DOCUMENT describes the GS1500M Low Power module hardware specification. The GS1500M module provides a cost effective, low power, and flexible platform to add Wi-Fi® connectivity for embedded devices for a variety of applications, such as wireless sensors and thermostats. It combines ARM7-based processors with an RF transceiver, 802.11 MAC, security, & PHY functions, FLASH and SRAM, onboard and off module certified antenna options, and various RF front end options for end customer range needs in order to provide a WiFi and regulatory certified IEEE 802.11 radio with concurrent application processing services for variety of applications, while leverage existing 802.11 [1] wireless network infrastructures.

1.2 Product Overview

- ▶ GS1500M module:
 - Dimensions are 1.450 inches by 0.900 inches by 0.143 inches (Length * Width * Height) 48-pin Dual Flat pack PCB Surface Mount Package.
 - Simple API for embedded markets covering large areas of applications
- ▶ Compliant with IEEE 802.11 and regulatory domains:
 - Fully compatible with IEEE 802.11b/g/n.
 - DSSS modulation for data rate of 1 Mb/s and 2 Mb/s; CCK modulation rates of 5.5 and 11 Mb/s.
 - OFDM modulation for data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mb/s.
 - 802.11n 1x1 HT20 for data rates of MCS0 – 7.
 - Supports short preamble and short slot times.
 - WiFi Certified Solution
 - Supports 802.11i security
 - WPA™ - Enterprise, Personal
 - WPA2™ - Enterprise, Personal
 - Vendor EAP Type(s)
 - EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1/EAP-GTC, EAP-FAST, EAP-TLS
 - Hardware encryption/decryption engines for WEP, WPA/WPA2 (AES and TKIP)
 - RoHS and CE compliant
 - FCC/IC/ETSI Certified
- ▶ Dual ARM7 Processor Platform:
 - 1st ARM7 processor (WLAN CPU) for WLAN software
 - 2nd ARM7 (APP CPU) for networking software
 - Based on Advanced Microprocessor Bus Architecture (AMBA) system:
 - AMBA High-Speed Bus (AHB).
 - AMBA Peripheral Bus (APB).
 - On-chip WLAN boot code located in dedicated boot ROM.

- ▶ Interfaces:
 - PCB or external antenna options, electronically selected.
 - Two SPI interfaces
 - One Master SPI for external flash memory device only
 - One Slave SPI interface (which can be configured as master, or slave or fast slave SPI). This interface can be used for external CPU interface, or for sensors and memory..
 - Two multi-purpose UART interfaces.
 - Up to 23 configure able general purpose I/Os.
 - Single 3.3V supply option
 - One PWM output
 - I²C master/slave interface.
 - Two 10-bit ADC channels, aggregate sample rate 32 kS/s.
 - Two alarm inputs to asynchronously awaken the chip.
 - Support of up to two control outputs for power supply and sensors.
- ▶ Embedded RTC (Real Time Clock) can run directly from battery.
- ▶ Power supply monitoring capability.
- ▶ Low-power mode operations
 - ▶ Standby, Sleep and Deep Sleep

2 Architecture

2.1 G1500M Block Diagram

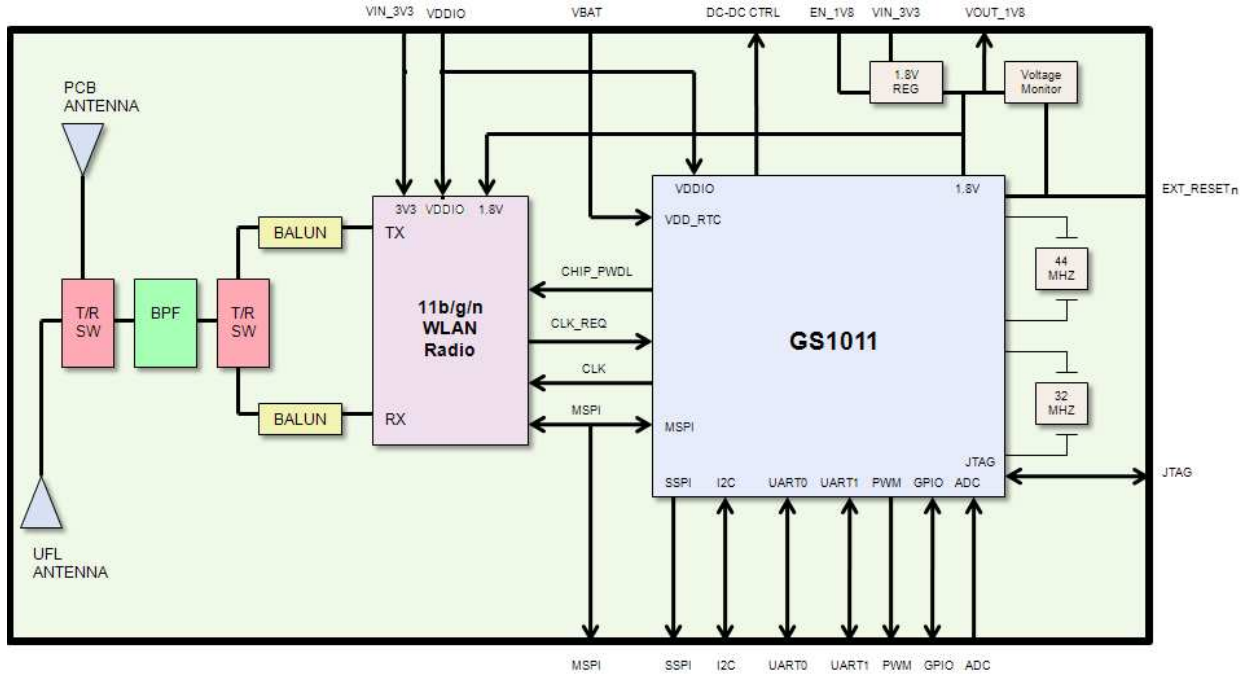


Figure 2-1: GS1500M Block Diagram

2.2 Block Diagram Description

2.2.1 Overview

- The GS1500M module includes:
 - a highly integrated IEEE 802.11b/g/n WLAN chip, which contains a MAC, baseband, security and radio functions in a single package
 - a GS1011 Chip (ultra-low power Wi-Fi system-on-chip (SOC), containing two ARM7-based processors (one dedicated to Networking services, and the other dedicated to Wireless services), on-chip flash memory and SRAM in a single package
- The module carries an 802.11b/g/n radio with onboard 32 KHz & 44 MHz crystal circuitries, RF, and certified PCB antenna or external antenna options.
- Variety of interfaces are available such as two UART blocks using only two data lines per port with optional hardware flow controls, two SPI block, I²C with Master or slave operation, JTAG port, low-power 10-bit ADC capable of running at up to 32 KSamples/sec., GPIO's, and LED Drivers/GPIO with 20mA capabilities.
- GS1500M requires an always available power source on the VBAT pin, which powers the Real Time Clock (RTC). Frequently this is connected directly to a battery. The GS1500M contains a 1.8V regulator, which is turned on and off by the EV_1V8 pin. In systems that enable standby

mode, this pin is driven from the DC_DC_CNTL pin. The GS1500M also has a VDDIO power supply input that provides the logic signal level for the I/O pins. VDDIO **must** turn on and off with the 1.8V power. So, if the 1.8V power is controlled by the DC_DC_CNTL signal, then the DC_DC_CNTL signal also must turn VDDIO and VIN 3V3 on and off. The VIN_3V3 pin provides the input power for the 1.8V regulator. In addition this pin provides power for the external 802.11 radio.

2.2.2 Wireless LAN and System Control Subsystem

The GS1500M Wireless LAN and system control subsystem consists of an ARM7 TDMI-S CPU providing system control functions which provides for control and management functions of the external 802.11b/g/n WLAN chip.

2.2.3 Network Services Subsystem

2.2.3.1 APP CPU

The Network services subsystem consists of an APP CPU which is based on an ARM7 TDMI-S core. It incorporates an AHB interface and a JTAG debug interface. The network RTOS, network stack, and customer application code can reside on this CPU. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.2.4 Memory Subsystem

2.2.4.1 Overview

The GS1500M module contains several memory blocks:

- ▶ Boot ROM blocks.
 - ▶ The software contained in this ROM provides the capability to download new firmware via the SPI Slave or UART interfaces and to control the update of WLAN and APP Flash Memory.
- ▶ 384 Kbytes of Embedded Flash to store program code.
 - ▶ Three embedded Flash blocks of 128K bytes each
 - ▶ WLAN Flash (contains the wireless LAN and system control subsystem software)
 - ▶ APP Flash 0 and 1 (contain the Network/Application Software)
- ▶ 128 Kbytes of RAM shared between the two integrated CPU's.
- ▶ 512 bytes of RTC memory ((retains data in all states, as long as the battery or other voltage supply is present)

For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.2.5 Clock Circuitries

The GS1500M architecture uses a low-power oscillator (i.e. 32 kHz) to provide a minimal subset of functions when the chip is in its low-power deep sleep mode, and a high-speed 44 MHz oscillator to provide clock signals for the processors, bus, and interfaces during active operation. Intermediate modes of operation, in which the 44 MHz oscillator is active but some modules are inactive, are obtained by gating the clock signal to different subsystems. The Clock & Reset Controller, within the device, is

responsible for generation, selection and gating of the clocks used in the module to reduce power consumption in various power states.

2.2.5.1 Real Time Clock (RTC) Overview

To provide global time (and date) to the system, the GS1500M is equipped with a low-power Real Time Clock (RTC).

RTC key features include:

- ▶ 32.768 kHz crystal support.
- ▶ Two external alarm inputs to wake up the device.
- ▶ Two programmable periodic outputs (one for a DC/DC regulator and one for a sensor).
- ▶ Embedded 128x32 non-volatile (battery-powered) RAM.
- ▶ Embedded Power On Reset.
- ▶ Real Time Counter (48 bits; 46 bits effective).

An overview of RTC block diagram is shown in Figure 2-3. The RTC contains a low-power oscillator that can use 32.768 kHz crystals. In normal operation the RTC is always powered up, even in the Power Up state (see Figure 2-3).

Two programmable embedded alarm counters (wrap-around) are provided to enable periodic wake-up of the remainder of the system, and one independent external component (typically a sensor). Two external alarm inputs enable wake-up of the system on external events. The global times are recorded on each external event and if the system is in the Power-ON state (see Figure 2-8), an interrupt is provided. The RTC includes a Power-On Reset (POR) circuit, to eliminate the need for an external component. The RTC contains low-leakage non-volatile (battery-powered) RAM, to enable storage of data that needs to be preserved.

Total current consumption of the RTC in the worst case is typically less than 5 μ A without data storage, using the 32.768 kHz oscillator.

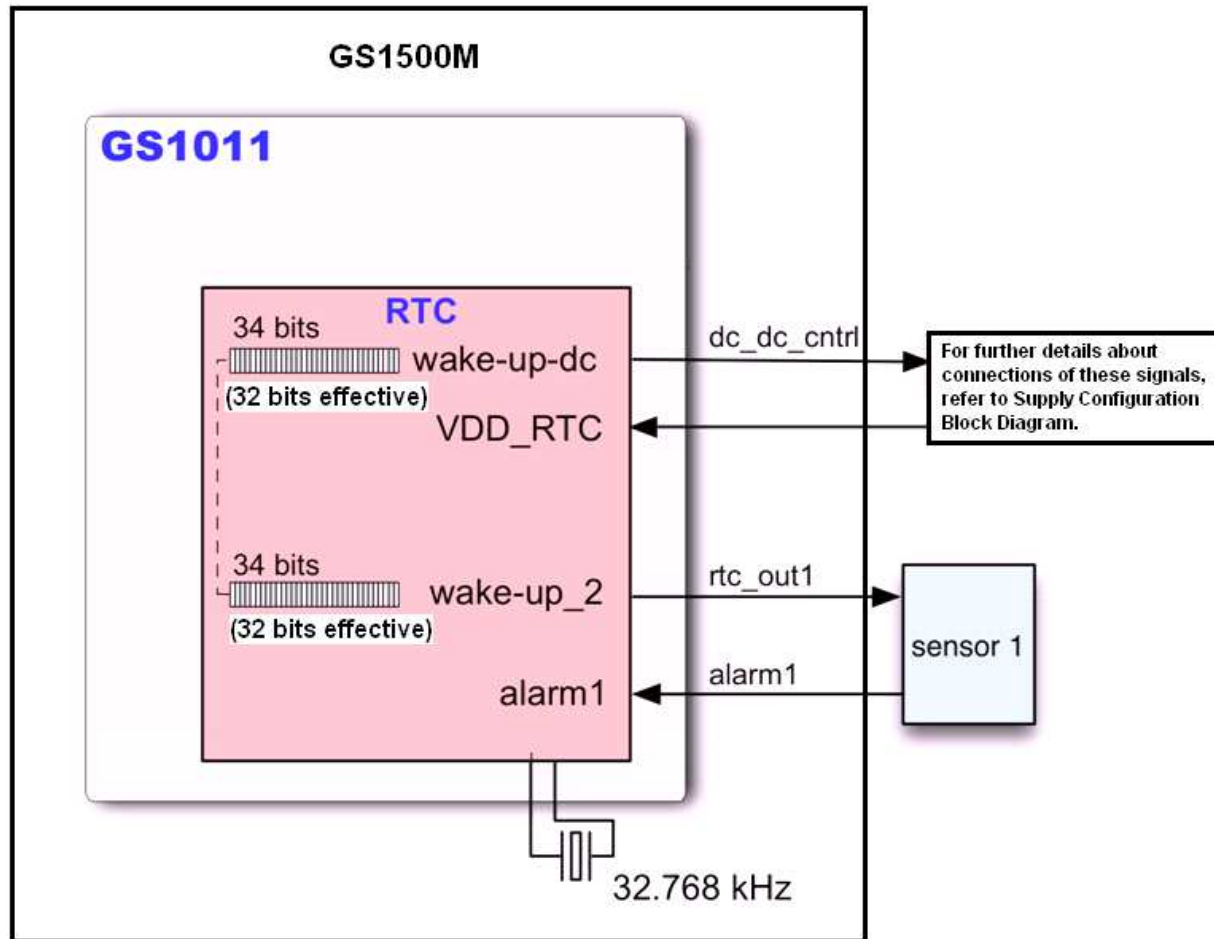


Figure 2-2: RTC Interface Diagram

Resolution of the wake-up timer is one clock cycle, and, with onboard 32KHz. CLK, each 32bit effective register can provide up to 1.5 days' worth of standby duration as the longest standby period. Polarity of the rtc_out1 pin is programmable.

2.2.5.2 Real Time Counter

The Real Time Counter features:

- ▶ 48-bit length (with absolute duration dependent on the crystal frequency used).
- ▶ Low-power design.

This counter is automatically reset by power-on-reset.

This counter wraps around (returns to “all-0” once it has reached the highest possible “all-1” value).

2.2.5.3 RTC Outputs

There are two RTC outputs (dc_dc_cntrl and rtc_out1) that can be used to control external devices, such as sensors or voltage regulators. For more information, consult the GS1011 Peripheral and Register Description for detailed descriptions.

2.2.5.3.1 DC_DC_CNTL

During RTC Power-on-Reset (e.g. when the battery is connected), the dc_dc_cntl pin is held low; it goes high to indicate completion of RTC power-on-reset. This pin can be used as an enable into an external device such as voltage regulator. For more information, consult the GS1011 Peripheral and Register Description for detailed descriptions.

2.2.5.3.2 RTC_OUT1

The rtc_out1 signal can be disabled or driven by the Wake-up Counter 2. This counter is 34 bits long, and operates in the same fashion as Wake-up Counter 1. The rtc_out1 signal can be configured to output the low-power crystal oscillator clock (i.e. the 32 kHz clock) instead of a simple state transition. Wake-up Counter 2 is automatically reset at Power-on-Reset. For more information, consult the GS1011 Peripheral and Register Description for detailed descriptions.

2.2.5.4 RTC Alarm Inputs 1 and 2

The RTC inputs alarm1 and alarm2 operate as follows:

- ▶ dc_dc_cntl is set to “1” (typically enabling the power supply to the rest of the GS1500M) whenever either of these inputs changes state.
- ▶ The RTC counter value is stored each time either of these inputs changes state.

The inputs alarm1 and alarm2 have programmable polarity. Their task is to wake up the system (by setting dc_dc_cntl output pin to “1”) when an external event occurs. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.3 Peripherals

Note: For register identification and additional details on the use of shared peripherals, refer to the GS1011 Peripheral and Register Description [3].

2.3.1 SPI

There are two SPI interfaces. The Master SPI (MSPI) is used by WLAN CPU to communicate to external flash memory device only. The MSPI interface cannot be controlled directly by the APP CPU and hence the MSPI interface cannot be used for general purpose SPI devices

The Slave SPI (SSPI) is general purpose and is configurable as master, slave or fast slave SPI. The SSPI interface could be used for external sensors, memory, or external CPU interface; The Fast SPI Slave is not shared, and is accessible only by the APP CPU. The Fast SPI operates only in the Motorola-compatible SPI slave mode, using 8-bit words and a 64-word FIFO buffer for both transmit and receive. The Serial to Wi-Fi firmware which uses SPI interface uses this Fast SPI mode. The recommended host clock speed when using the Serial to Wi-Fi firmware with SPI interface is 1.4MHz. Each block provides synchronous serial communication with slave or master devices, using one of the following protocols:

- ▶ Motorola Serial Peripheral Interface (SPI).
- ▶ Texas Instruments Synchronous Serial Protocol (SSP).
- ▶ National Semiconductor Microwire Protocol.

Only Motorola Serial Peripheral Interface (SPI) timing is shown in this data sheet; however, National Semiconductor Microwire Protocol or Texas Instruments Synchronous Serial Protocol (SSP) modes are certainly supported. The SPI interface can also be used to access non-volatile external memory, such as an EEPROM block. The interface uses the SPI master mode to allow easy connection to industry-standard EEPROMs.

The SPI block provides the following general features:

- ▶ 32-bit AMBA APB interface to allow access to data, control, and status information by the host processor.
- ▶ Full-duplex serial-master or serial-slave operation.
- ▶ Two clock design:
 - APB bus clock for bus interface and registers.
 - Serial input clock for core logic.
- ▶ The Slave SPI block supports connections of external EEPROM or other non-volatile memory when used in Master mode.
- ▶ Programmable choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire.
- ▶ Programmable control of the serial bit rate of the data transfer in serial-master mode of operation.
- ▶ Programmable phase and polarity of the bit rate clock.
- ▶ Programmable transfer modes to perform transmit and receive, transmit only, receive only and EEPROM read transfers.
- ▶ Programmable data word size (8, 16, 24 & 32 bits) for each data transfer.
- ▶ Transmit and receive FIFO buffer depth 8 words (of the selected size).
- ▶ Configurable number of slave select outputs in serial-master mode of operation: 1 to 4 serial slave-select output signals can be generated.
- ▶ Combined interrupt line with independent masking of interrupts.
- ▶ Transmit FIFO overflow, transmit FIFO empty, transmit FIFO underflow, receive FIFO full, receive FIFO underflow, receive FIFO overflow, and receive FIFO timeout interrupts.
- ▶ Transmit FIFO empty and receive FIFO full interrupts provide programmable threshold values.

Both SPI blocks are configured to provide a FIFO depth of eight entries.

The SPI slave interface can be used to provide control of the GS1500M from an external CPU.

In master mode SPI chip select (MSPI_CS0 or MSPI_CS1) signals frame each data word. If the chip select is required to remain asserted for multiple data words, then a GPIO pin should be used for the chip select instead of the SPI chip select signals. For clock architecture and rates, please refer to section 7.1 Clock Architecture of GS1011 Peripheral and Register Description [2]. For other SPI Interface Timing, please refer to section 4.8.

2.3.2 I²C

The I²C block provides a two-wire I²C serial interface. It provides the following features:

- ▶ 32-bit AMBA APB interface to allow access to data, control, and status Information by the host processor.
- ▶ Serial 2-wire I²C bus, compliant to the I²C Bus Specification Version 2.1.
- ▶ Supports only one transfer in Standard mode (100 Kb/s) and fast speed mode with a bit rate of up to 392 Kb/s.
- ▶ Supports Multi-Master System Architecture through I²C bus SCL line Synchronization and Arbitration.

- ▶ Transmitter and Receiver: The I²C block can act as the Transmitter or Receiver depending on the operation being performed.
- ▶ Master or slave I²C operation.
- ▶ 7- or 10-bit addressing.
- ▶ Ignores CBUS addresses (an older ancestor of I²C that used to share the I²C bus).
- ▶ Interrupt or polled mode operation.
- ▶ Combined interrupt line triggered by:
 - Tx FIFO not FULL.
 - Rx FIFO not EMPTY.
 - Rx FIFO FULL (can be used to transfer data by host interface in bursts).
 - Tx FIFO EMPTY (can be used to transfer data by host interface in bursts).
 - Rx FIFO OVER RUN.
 - Master mode to Slave Transfer Request.
 - Slave Transmit Request.
 - Break Interrupt (master mode): No Acknowledge received from slave for slave address or write data.
- ▶ Digital de-bounce logic for the received SDA and SCL lines.
- ▶ Hold Delay Insertion on SDA line.

2.3.3 UART

The GS1500M includes two UART blocks. Each UART block provides an asynchronous communication interface, using only two data lines: Rx data and Tx data. Hardware flow control using RTS/CTS signaling is provided as an option. The UART is a standard asynchronous serial interface, 16450/16550 compatible. It provides the following features:

- ▶ Operation in full-duplex mode.
- ▶ All standard bit rates up to 921.6 kbps are supported.
- ▶ RTS/CTS flow control handshake (standard 16550 approach).
- ▶ 5, 6, 7 and 8-bit character format.
- ▶ 1 or 2 stop bits (1.5 in case of a 5-bit character format).
- ▶ Parity bit: none, even, odd, mark, or space.
- ▶ 16-byte Rx and 16-byte Tx FIFOs.

The UART Serial port can be used to communicate with a PC or other devices, for debug or additional functionality.

2.3.4 JTAG

The JTAG ports facilitate debugging of the board and system designs. This block has the following features:

- ▶ Compliant to IEEE-1149.1 TAP ports.
- ▶ One JTAG boundary scans TAP port.
- ▶ One set of JTAG pins, which support the following mode of operation:

- APP ARM7TDMI-S Debug Mode.

2.3.5 GPIO & LED Driver / GPIO

The GPIO ports are referenced to VDDIO. Two GPIO pins called GPIO30_LED1 & GPO31_LED2 have the capability to sink/source 20 mA typical (VDDIO=3.3V) to connect to devices such as switch contacts or LEDs. I2C_DATA/GPIO8 & I2C_CLK/GPIO9 have the capability to sink/source 12 mA typical (VDDIO=3.3V). Other GPIO's have the capability to sink/source 4 mA typical (VDDIO=3.3V). All inputs are capable of generating processor interrupts. They can be individually programmed to provide edge- or level-triggered interrupts. For details on configuring GPIO ports, refer to the GS1011 Peripheral and Register Description [2].

2.3.6 ADC

The ADC is a 10-bit, low-power, A-to-D converter capable of running at up to 32 ksps. The ADC contains an internal band-gap reference which provides a stable 1.2 V reference voltage. The ADC can be programmed to use the 1.8 V supply as the full-scale reference. The ADC uses an input clock with a maximum frequency of 1 MHz. A conversion requires 32 clock cycles.

When the internal band-gap reference is used, the reported integer *Value* at temperature T (°C) is related to the voltage V_{actual} at the input pin as:

$$V_{actual} = Value \left(\frac{1.2444 - 0.00014(25 - T)}{1023} \right)$$

When the 1.8V supply voltage is used as the reference, the corresponding relation is:

$$V_{actual} = Value \left(\frac{V_{DD,ADC} - 0.036}{1023} \right)$$

To reduce power consumption the ADC can be disabled automatically between periodic measurements and after single measurements.

For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

2.4 System States

Figure 2-8 shows the power management/clock states of the GS1500M system.

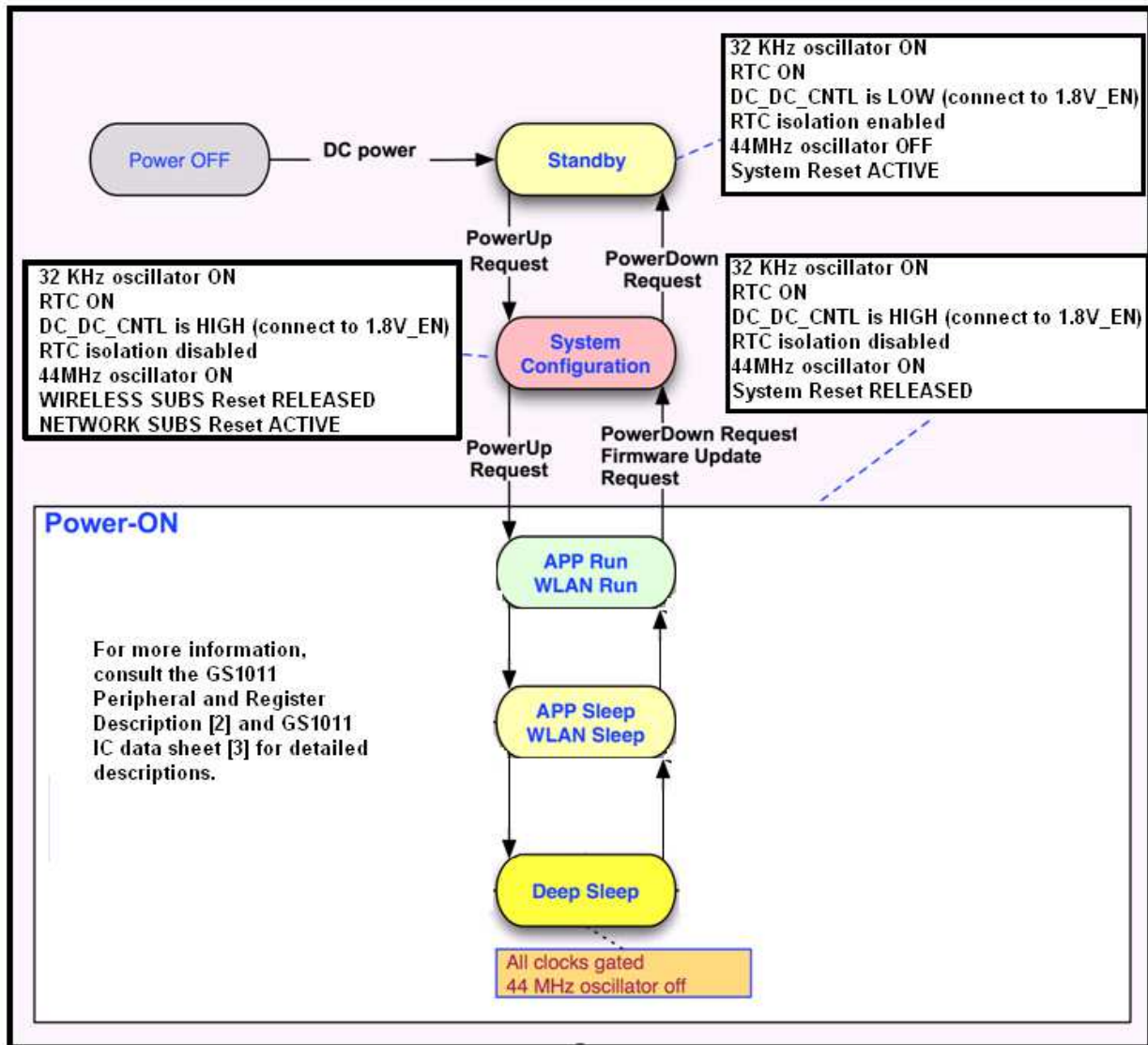


Figure 2-3: GS1500M System States

The system states of the GS1500M system are as follows:

Power OFF: No power source connected to the system. I/O's should not be driven high by an external device during this state.

Standby: In the standby state, only the RTC portion of the GS1500M is powered from the VBAT pin. The other power supplies are turned off by the DC_DC_CNTL pin being low. Power supplies which **MUST** be powered on and off together, controlled by the DC_DC_CNTL pin, include the EN_1V8 pin (which controls VOUT_1V8), VDDIO, and the VIN_3V3 pin.

In standby state the 32.768KHz oscillator keeps running and only the RTC RAM retains the state. SRAM, CPUs and I/Os are all in OFF state, as there is no 1.8V and no VDDIO being supplied to the GS1011 device. I/O pins (except alarms) should not be driven high by an external device during standby state due to diodes in the internal ESD protection circuitry.

Driving I/O pins high during standby could result in incorrect operation on exit from standby state.

This is the lowest-power-consumption state. In a typical application, the system returns to the Standby state between periods of activity, to keep the average power very low and enable years of operation using conventional batteries. During standby, the RTC isolates itself from the rest of the chip, since the signals from the rest of the chip are invalid. This prevents corruption of the RTC registers.

Exit from standby occurs when a pre-specified wakeup time occurs, or when one of the two alarm pins sees the programmed polarity of signal edge. When one of the wakeup conditions occurs, the RTC asserts reset to the chip and sets the DC_DC_CNTL pin high to enable power to the rest of the module. After 3mS, the power to the rest of the module is assumed to be good, the isolation between the RTC and the rest of the chip is released, and the EXT_RESETE pin is released. The WLAN CPU now runs at 32KHz for another 10mS until the 44MHz oscillator is stable, at which time it switches over to running at 22MHz. Another ~900mS are required to initialize the application software.

Note that the alarm pins are strictly edge detected, and cannot be read like GPIO pins. If it is necessary to read the DC level of an alarm input, the signal must be connected to a GPIO pin thru an over-voltage tolerant buffer, powered from VDDIO, so that it stops driving the GPIO pin when VDDIO is turned off in standby mode.

Note: During first battery plug, i.e. when power is applied the first time to the RTC power rail (VBAT), the power detection circuit in the RTC also causes a wakeup request. The RTC startup up latency will be at least a couple of hundred ms (and may be as much as 3 seconds) as it is waiting for stabilization of the 32KHz crystal. After the oscillator startup delay, at first battery plug, there is a 7.8mS delay for power to be assumed good and a 31.25mS delay for 44MHz oscillator startup. These delays are reduced for subsequent startups by the first battery plug software. Again, ~900mS are required to initialize the application software.

System Configuration: When a power-up is requested, the system transitions from the Standby state to the System Configuration state. In this state, the WLAN CPU is released from reset by the RTC. The APP CPU remains in the reset state during System Configuration. The WLAN CPU then executes the required system configurations, releases the APP CPU from reset, and transitions to the Power-ON state.

The System Configuration state is also entered on transition from the Power-ON state to the Standby state, to complete necessary preparations before shutting off the power to the core system. Finally, the System Configuration state is used for firmware updates.

Power-ON: This is the active state where all system components can be running. The Power-ON state has various sub-states, in which unused parts of the system can be in sleep mode, reducing power consumption. Sleep states are implemented by gating the clock signal off for a specific system component.

Sleep: In the Sleep state, the 44MHz crystal remains running, but it is gated off to one or both CPUs. Each CPU can independently control its own entry into Sleep state. Any enabled interrupt will cause the interrupted CPU to exit from Sleep state, and this will occur within a few clock cycles.

Deep Sleep: Deep sleep is entered only when both CPUs agree that the wakeup latency is OK. In Deep Sleep mode, the 44MHz crystal oscillator is turned off to save power, but all power supplies remain turned on. Thus all registers, memory, and I/O pins retain their state. Any enabled interrupt will cause an exit from Deep Sleep state, but this now requires startup of the 44MHz oscillator, which requires 10mS.

The following are not system states, but are related design notes:

Power Control: The GS1500M was designed with the intent that power to the non-RTC portions of the chip be controlled from the DC_DC_CNTL signal. In applications where it is preferred that an external host control the power, this is OK if ALL power, including VBAT power, is turned on and off by the external host. In this case, all state is lost when power goes off, and the latencies from first battery plug apply.

If these latencies are not acceptable, then the GS1500M MUST control power. The external host would use an alarm to wake it up, and a serial command to put it into standby. And the DC_DC_CNTL pin would control the power supplies. It is NOT reliable for the external host to directly control the power supplies if VBAT is to be left turned on. This is because the RTC would not know when to isolate itself from the rest of the chip, and might get corrupted during power up or power down.

EXT_RESETE_n pin: If the external host is driving the EXT_RESETE_n pin, it MUST do so with an open drain driver. This is because this pin also must be able to be driven low by the RTC and by the voltage monitor chip on the GS module. In addition, if an external host is connected to the EXT_RESETE_n pin, there must be an external 10K ohm pull-up resistor on the board, pulling up to VDDIO. This is needed to overcome a possible pull-down in the host at first power application. It is also recommended that the host not actively assert EXT_RESETE_n until all the startup latencies have expired.

One possible usage of the EXT_RESETE_n pin by an external host is to monitor the pin as an input to detect when the 32KHz oscillator has started up after first application of VBAT power. When the EXT_RESETE_n pin goes high, the oscillator has started. Under most conditions, this will be considerably faster than the 3 second worst case.

It should also be noted that the constraint that I/O pins not be driven high during standby also applies to the EXT_RESETE_n pin. It should be pulled only to VDDIO, which shuts off in standby mode.

For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 SoC data sheet [3] for detailed descriptions.

3 Pin-out and Signal Description

3.1 GS1500M Device Pin-out Diagram (Module top view)

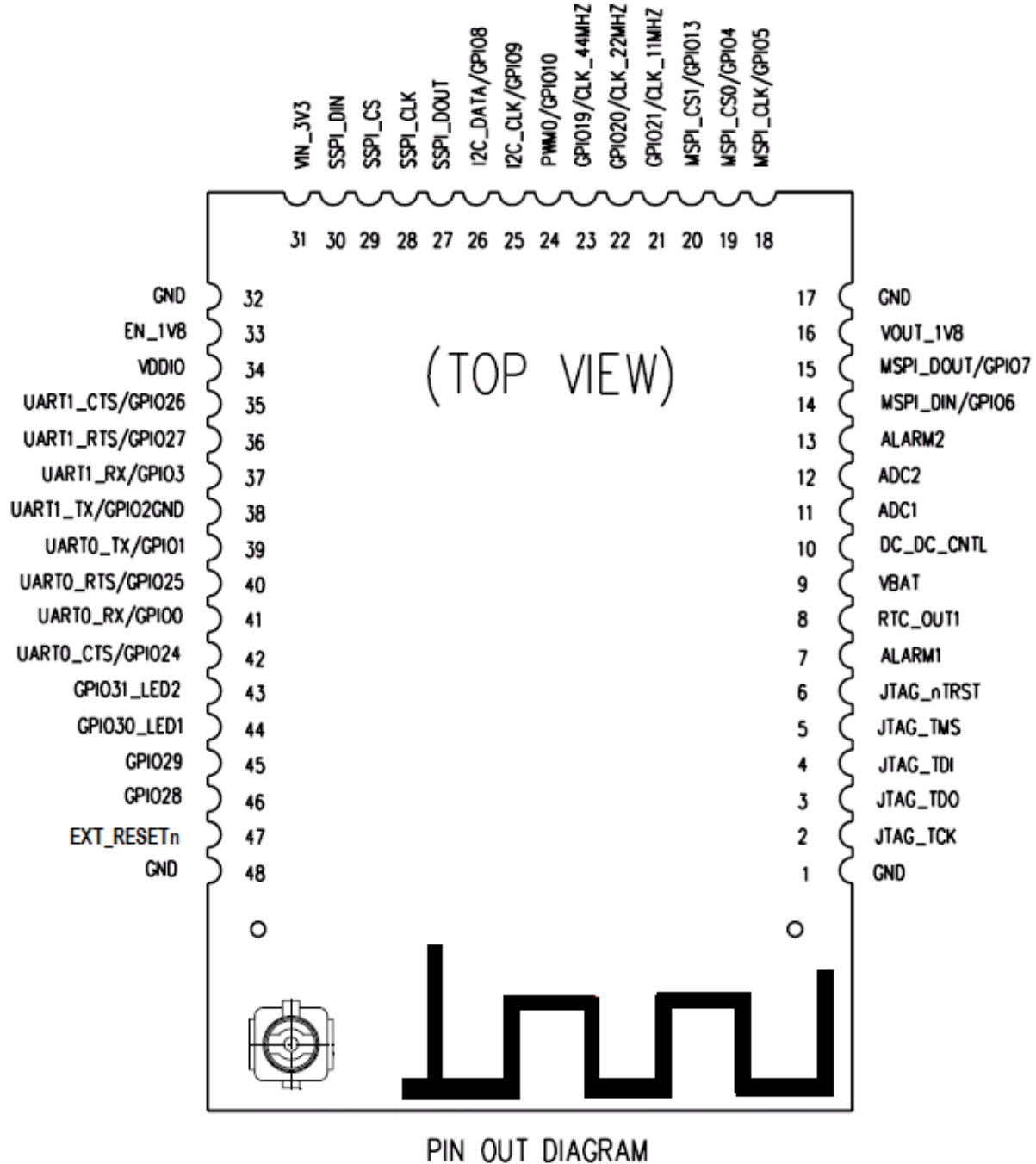


Figure 3-1: GS1500M Device Pin-out Diagram (Module top view)

3.1.1 GS1500M Module Pins Description

PINS	NAME	VOLTAGE	INTERNAL BI-	SIGNAL	DESCRIPTION
	GND	0V	Not Applicable	Analog port	Ground
	JTAG_TCK	VDDIO	Pull-up (See Note 1)	Digital Input	Joint Test Action Group Test Clock
	JTAG_TDO	VDDIO	Not Applicable	Digital Output	Joint Test Action Group Test Data Out
	JTAG_TDI	VDDIO	Pull-up (See Note 1)	Digital Input	Joint Test Action Group Test Data In
	JTAG_TMS	VDDIO	Pull-up (See Note 1)	Digital Input	Joint Test Action Group Test Mode Select
6	JTAG_nTRST	VDDIO	Pull-up (See Note 1)	Digital Input	Joint Test Action Group Test Mode Reset Active Low
7	ALARM1	VBAT	Pull-down (See Note 1)	RTC Input	Embedded Real Time Clock Wake Up Input 1
8	RTC_OUT1	VBAT	Not Applicable	RTC Output	Embedded Real Time Clock Wake Up Output 1
9	VBAT	VBAT	Not Applicable	Analog port	Embedded Real Time Clock Power Supply
10	DC_DC_CNTL	VBAT	Not Applicable	Digital Output	VIN_3V3 Regulator Control Output
11	ADC1	VDD18 (internal)	Not Applicable	Analog Input	General Analog to Digital Converter 1
12	ADC2	VDD18 (internal)	Not Applicable	Analog Input	General Analog to Digital Converter 2
	ALARM2	VBAT	Pull-down (See Note 1)	RTC Input	Embedded Real Time Clock Wake Up Input 2
14	MSPI_DIN / GPIO6	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Data Input / General Purpose Input Output
15	MSPI_DOUT / GPIO7	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Data Output / General Purpose Input Output
16	VOUT_1V8	VIN_3V3 (internally regulated)	Not Applicable	Analog port	Internal 1.8V Vout
	GND	0V	Not Applicable	Analog port	Ground
18	MSPI_CLK / GPIO5	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Clock / Gen- eral Purpose Input Output
19	MSPI_CS0 / GPIO4	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Chip Select 0 / General Purpose Input Output
20	MSPI_CS1 / GPIO13	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Chip Select 1 / General Purpose Input Output
21	GPO21_11MHZ	VDDIO	Pull-down	Digital Input / Output	Internal Clock Circuitry Test Point / General Purpose Input Output
22	GPO20_22MHZ	VDDIO	Pull-down	Digital Input / Output	Internal Clock Circuitry Test Point / General Purpose Input Output

PINS	NAME	VOLTAGE	INTERNAL BI-	SIGNAL	DESCRIPTION
23	GPO19_44MHZ	VDDIO	Pull-down	Digital Input / Output	Internal Clock Circuitry Test Point / General Purpose Input Output
24	PWM0 / GPIO10	VDDIO	Pull-down	Digital Input / Output	Pulse Width Modulator / General Purpose Input Output
25	I2C_CLK/GPIO9	VDDIO	Pull-down (NOTE 4)	Digital Input / Output	Inter-Integrated Circuit Clock / General Purpose Input Output
26	I2C_DATA/GPIO8	VDDIO	Pull-down (NOTE 4)	Digital Input / Output	Inter-Integrated Circuit Data / General Purpose Input Output
	SSPI_DOUT	VDDIO	Pull-up (See Note 1)	Digital Output	SPI Slave Transmit Data Output to the HOST
28	SSPI_CLK	VDDIO	Pull-up (See Note 1)	Digital Input	SPI Slave Clock Input from the HOST
29	SSPI_CS	VDDIO	Pull-up (See Note 1)	Digital Input	SPI Slave Chip Select Input from the HOST
30	SSPI_DIN	VDDIO	Pull-down (See Note 1)	Digital Input	SPI Slave Receive Data Input from the HOST
31	VIN_3V3	VIN_3V3	Not Applicable	Analog port	Single Supply Port
32	GND	0V	Not Applicable	Analog port	Ground
33	EN_1V8	VDDIO	Need to be driven HIGH or LOW externally	Digital Input	Internal 1.8V regulator enable port-Active High
34	VDDIO	VDDIO	Not Applicable	Analog port	All I/O voltage domain (can be tied to VIN_3V3 or tied to HOST I/O supply)
35	UART1_CTS / GPIO26	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 1 Clear to Send Input (See Note 6) / General Purpose Input Output
36	UART1_RTS / GPIO27	VDDIO	Pull-down (See Note 2)	Digital Input / Output	Universal Asynchronous Receiver Transmitter 1 Request to Send Output (See Note 6) / General Purpose Input Output
37	UART1_RX / GPIO3	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 1 Receive Input / General Purpose Input Output
38	UART1_TX / GPIO4	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 1 Transmitter Output / General Purpose Input Output
39	UART0_TX / GPIO1	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 0 Transmitter Output / General Purpose Input Output
40	UART0_RTS / GPIO25	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 0 Request to Send Output (See Note 6) / General Purpose Input Output
41	UART0_RX / GPIO0	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 0 Receive Input / General Purpose Input Output

PINS	NAME	VOLTAGE	INTERNAL	SIGNAL	DESCRIPTION
42	UART0_CTS / GPIO24	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 0 Clear to Send Input (See Note 6) / General Purpose Input Output
43	GPO31_LED2	VDDIO	Pull-down	Digital Input / Output	Light Emitting Diode Driver / General Purpose Input Output
44	GPIO30_LED1	VDDIO	Pull-down	Digital Input / Output	Light Emitting Diode Driver / General Purpose Input Output
45	GPIO29	VDDIO	Pull-down (See Note 3)	Digital Input / Output	General Purpose Input Output
46	GPIO28	VDDIO	Pull-down (See Note 3)	Digital Input / Output	General Purpose Input Output
47	EXT_RESETh (See Note 5)	VDDIO	Pull-up	Digital Open Drain Input / Out-	Module Hardware Reset Input and Power Supply Reset Monitor Indicator Active Low
48	GND	0V	Not Applicable	Analog port	Ground

Table 3-1: Signal Description

Notes:

1. These pins have onboard hardware configured pull-ups/downs and cannot be changed by software.
2. If UART1_RTS (GPIO27) is high during reset or power on, then the GS1500M will wait for Flash download via UART0 or SSPI interface. Route this pin on the base board so it can be pulled up to VDDIO for programming the module.
3. GPIO 28 and 29 are sampled at reset to establish JTAG configuration for debugging. These signals should not be driven from an external device. If using JTAG, configure these pins as outputs.
4. If I²C interface is used, provide 2K Ohm pull-ups, to VDDIO, for pins 25 and 26 (I2C_CLK and I2C_DATA)
5. EXT_RESETh is an active low signal. It is an output during power up, indicating to the system when GS1500M is out of power-on-reset. After power-on-reset, this pin is an input. It is not necessary to assert reset to the GS1500M after power on, since the GS1500M has a built-in power on reset. Also, the EXT_RESETh signal does not clear the RTC RAM or the SRAM.
6. CTS and RTS signals indicate it is clear to send or ready to send when they are LOW. If signals are high, indicates device is not ready.
7. The WLAN CPU controls the MSPI interface and its driver supports an external Flash Memory device only (compatible with Numonyx M25P80 device). The MSPI interface cannot be controlled directly by the APP CPU and hence the MSPI interface cannot be used for general purpose SPI devices.

3.1.2 Example Module Pin Connections

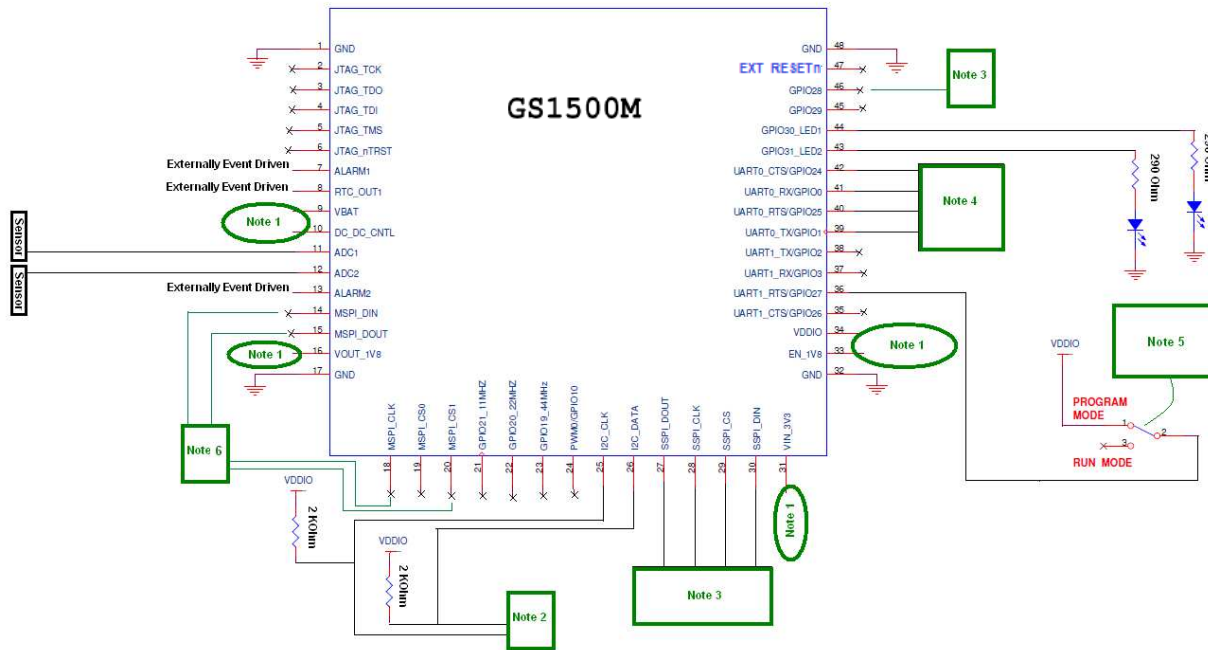


Figure 3-2: Module pin connection diagram

- Note 1) For the noted pin configurations, please refer to data sheet power supply section.
- Note 2) If I²C interface is used, provide 2KOhm pull-ups, to VDDIO, for pins 25 and 26 (I2C_CLK and I2C_DATA). If not used, leave pins 25 and 26 as No Connects.
- Note 3) Connect to external HOST SPI (can be left as No Connects if not used).
- Note 4) Connect to external serial HOST UART (can be left as No Connections if not used)
- Note 5) This switch enables the programming of GS1500M onboard flash. Switch is recommended for development purposes. For production it is recommended designers provide option to pull this pin (GPIO27) high during reset or power-on for in-circuit programming of the module. .
- Note 6) The need for external flash memory depends on advanced firmware features selected/required such as factory backup, a more robust over-the-air firmware update and Wi-Fi direct. The serial flash memory should be instruction set compliant with Numonyx M25P80.

3.2 Power Supply Connections

In this section, diagrams are shown for various application power supply connection.

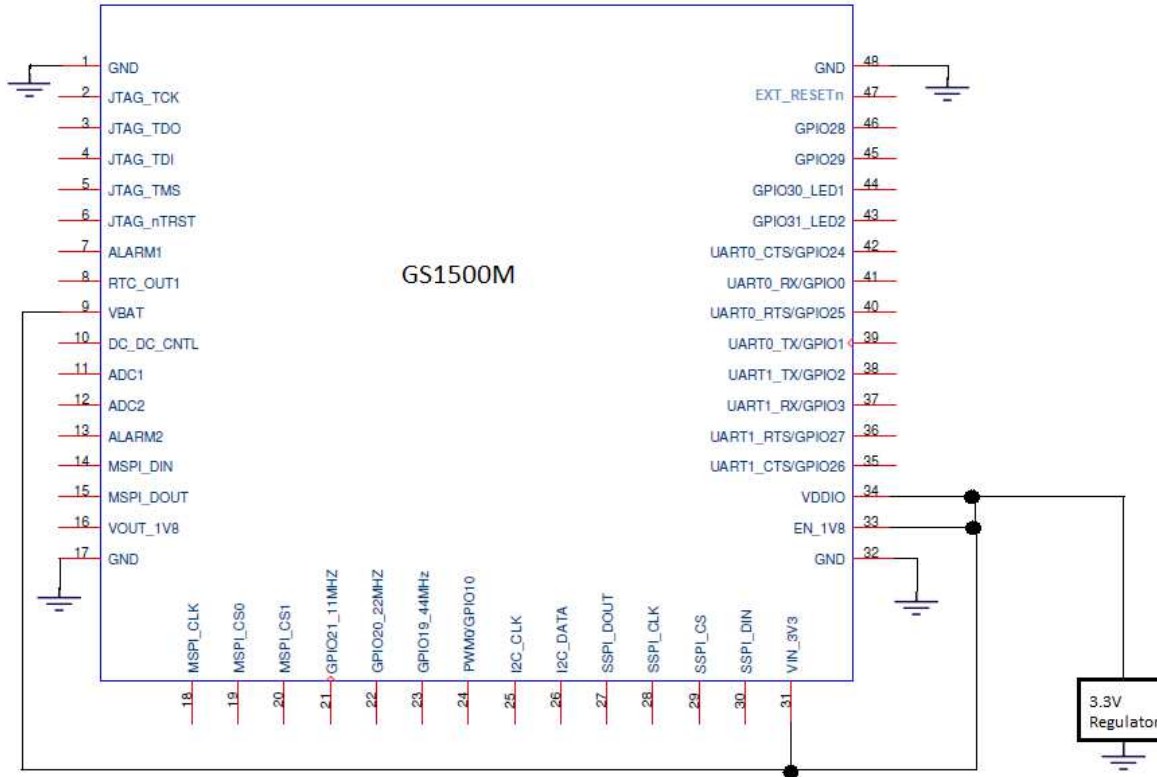


Figure 3-3 : GS1500M Always ON Power Supply Connection

Notes:

- 1) This connection applies generally for designs that target to keep system power on always and use 3.3V I/O
- 2) Always On is obtained by tying EN_1V8 high which is the enable for the 1.8V voltage regulator.
- 3) In this state system can still go to deep sleep state and take advantage of low power consumption, but system will not go into the lowest power consumption state (i.e. standby state).