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GS1559 HD-LINX™ II Multi-Rate Deserializer with Loop-Through Cable Driver

Key Features

- SMPTE 292M and SMPTE 259M-C compliant descrambling and NRZI →NRZ decoding (with bypass)
- DVB-ASI 8b/10b decoding
- Auto-configuration for HD-SDI and SD-SDI
- Serial loop-through Cable Driver output selectable as reclocked or non-reclocked
- Dual serial digital input buffers with 2 x 1 mux
- Integrated serial digital signal termination
- Integrated Reclocker
- Automatic or Manual rate selection/indication (HD/SD)
- Descrambler Bypass option
- User selectable additional processing features including:
  - CRC, TRS, ANC data checksum, line number and EDH CRC error detection and correction
  - Programmable ANC data detection
  - Illegal code remapping
- Internal Flywheel for noise immune H, V, F extraction
- FIFO load Pulse
- 20-bit/10-bit CMOS parallel output data bus
- 148.5MHz / 74.25MHz / 27MHz / 13.5MHz parallel digital output
- Automatic standards detection and indication
- 1.8V core Power Supply and 3.3V Charge Pump Power Supply
- 3.3V digital I/O supply
- JTAG test interface
- Available in a Pb-free package
- Small footprint (11mm x 11mm)

Applications

- SMPTE 292M Serial Digital Interfaces
- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS1559 is a reclocking Deserializer with a serial loop-through Cable Driver. When used in conjunction with the GS1574 Automatic Cable Equalizer and the GO1555/GO1525* Voltage Controlled Oscillator, a receive solution can be realized for HD-SDI, SD-SDI and DVB-ASI applications.

In addition to reclocking and deserializing the input data stream, the GS1559 performs NRZI-to-NRZ decoding, descrambling as per SMPTE 292M/259M-C, and word alignment when operating in SMPTE mode. When operating in DVB-ASI mode, the device will word align the data to K28.5 sync characters and 8b/10b decode the received stream.

Two serial digital input buffers are provided with a 2x1 Multiplexer to allow the device to select from one of two serial digital input signals.

The Integrated Reclocker features a very wide Input Jitter Tolerance of ±0.3 UI (total 0.6 UI), a rapid asynchronous lock time, and full compliance with DVB-ASI data streams.

An integrated Cable Driver is provided for serial input loop-through applications and can be selected to output either buffered or reclocked data. This Cable Driver also features an output mute on loss of signal, high-impedance mode, adjustable signal swing, and automatic dual slew-rate selection depending on HD/SD operational requirements.

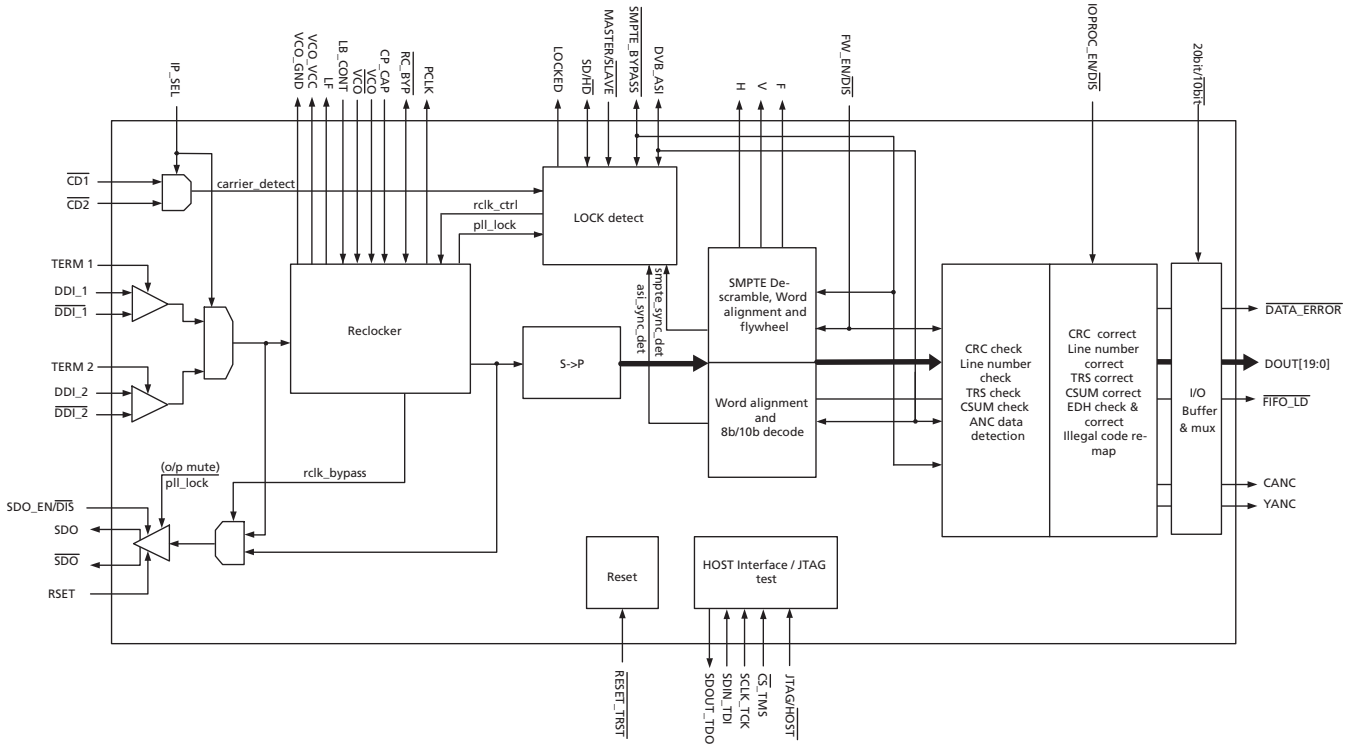
The GS1559 also includes a range of data processing functions such as error detection and correction, automatic standards detection, and EDH support. The device can also detect and extract SMPTE 352M payload identifier packets and independently identify the received video standard. This information is read from internal registers via the Host Interface port.

Line-based CRC errors, line number errors, TRS errors, EDH CRC errors and ancillary data checksum errors can all be detected. A single 'DATA_ERROR' pin is provided which is a logical 'OR'ing of all detectable errors. Individual error status is stored in internal 'ERROR_STATUS' registers.

Finally, the device can correct detected errors and insert new TRS ID words, line-based CRC words, ancillary data checksum words, EDH CRC words, and line numbers. Illegal code re-mapping is also available. All processing functions may be individually enabled or disabled via Host Interface control.

*For new designs use the GO1555.

Functional Block Diagram



GS1559 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and / or Modifications
8	147971	50711	July 2008	Changed register RASTER_STRUCTURE2 from 12 bits to 13 bits in Table 4-8: Host Interface Description for Raster Structure Registers. Changed SMPTE 352 Lines from 13 to 10 in Table 4-9: Supported Video Standards. Removed references to DVB_ASI in Master mode. Updated document to new format.
7	145031	–	May 2007	Updated description of H2 from PDBUFF_GND to EQ_GND in Table 1-1: Pin Descriptions. Changed GND_EQ to EQ_GND in 5.2 Typical Application Circuit (Part B).
6	143592	42774	January 2007	Added RoHS compliance statement to 7.3 Packaging Data. Recommended GO1555 VCO for new designs.
5	140420	39452	May 2006	Corrected minor typing errors in Functional Block Diagram. Modified video format numbers for system 1125 on Table 4-4: Switch Line Position for Digital Systems.

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	LF	VCO_ VCC	VCO_ GND	$\overline{\text{VCO}}$	VCO	NC	PCLK	IO_VDD	DOUT18	DOUT19
B	CP_CAP	CP_VDD	CP_GND	LB_ CONT	NC	NC	FW_EN /$\overline{\text{DIS}}$	IO_GND	DOUT16	DOUT17
C	BUFF _VDD	PD_VDD	PD/BUFF _GND	NC	NC	MASTER/ $\overline{\text{SLAVE}}$	$\overline{\text{RC\_BYP}}$	YANC	DOUT14	DOUT15
D	DDI1	NC	NC	IP_SEL	DVB_ASI	LOCKED	NC	CANC	DOUT12	DOUT13
E	$\overline{\text{DDI1}}$	TERM1	NC	SD/$\overline{\text{HD}}$	CORE _GND	CORE _VDD	NC	IO_VDD	DOUT10	DOUT11
F	$\overline{\text{CD1}}$	NC	NC	20bit/ $\overline{\text{10bit}}$	CORE _GND	CORE _VDD	NC	IO_GND	DOUT8	DOUT9
G	DDI2	NC	NC	IOPROC _EN/$\overline{\text{DIS}}$	$\overline{\text{SMPTE\_}}$ $\overline{\text{BYPASS}}$	$\overline{\text{RESET}}$ $\overline{\text{\_TRST}}$	NC	$\overline{\text{FIFO\_LD}}$	DOUT6	DOUT7
H	$\overline{\text{DDI2}}$	TERM2	NC	$\overline{\text{CS}}$_ TMS	SCLK _TCK	SDOUT _TDO	$\overline{\text{DATA\_}}$ $\overline{\text{ERROR}}$	H	DOUT4	DOUT5
J	$\overline{\text{CD2}}$	NC	NC	NC	SDO_EN /$\overline{\text{DIS}}$	SDIN _TDI	V	IO_GND	DOUT2	DOUT3
K	RSET	CD_VDD	SDO	$\overline{\text{SD0}}$	CD_GND	JTAG/ $\overline{\text{HOST}}$	F	IO_VDD	DOUT0	DOUT1

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
A1	LF	Analog	Output	Control voltage to external Voltage Controlled Oscillator. Nominally +1.25V DC.
A2	VCO_VCC	–	Output Power	Power Supply for the external Voltage Controlled Oscillator. Connect to pin 7 of the GO1555/GO1525*. This pin is an output. Should be isolated from all other power supplies. *For new designs use the GO1555.
A3	VCO_GND	–	Output Power	Ground reference for the external Voltage Controlled Oscillator. Connect to pins 2, 4, 6, and 8 of the GO1555/GO1525*. This pin is an output. Should be isolated from all other grounds. *For new designs use the GO1555.
A4, A5	$\overline{VCO}$, VCO	Analog	Input	Differential inputs for the external VCO reference signal. For single ended devices such as the GO1555/GO1525*, $\overline{VCO}$ should be AC coupled to VCO_GND. VCO is nominally 1.485GHz. *For new designs use the GO1555.
A6, B5, B6, C4, C5, D2, D3, D7, E3, E7, F2, F3, F7, G2, G3, G7, H3, J2, J3, J4,	NC	–	–	No Connect.
A7	PCLK	–	Output	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS/LVTTL compatible.
				HD 20-bit mode: PCLK = 74.25MHz or 74.25/1.001MHz
				HD 10-bit mode: PCLK = 148.5MHz or 148.5/1.001MHz
				SD 20-bit mode: PCLK = 13.5MHz
				SD 10-bit mode: PCLK = 27MHz
A8, E8, K8	IO_VDD	–	Power	Power Supply connection for digital I/O buffers. Connect to +3.3V DC digital.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
A10, A9, B10, B9, C10, C9, D10, D9, E10, E9	DOUT[19:10]	Synchronous with PCLK	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DOUT19 is the MSB and DOUT10 is the LSB.	
				HD 20-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = HIGH	Luma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW
				SD 20-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = HIGH	Luma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
B1	CP_CAP	Analog	Input	PLL lock time constant capacitor connection. Normally connected to VCO_GND through 2.2nF.	
B2	CP_VDD	–	Power	Power supply connection for the Charge Pump. Connect to +3.3V DC analog.	
B3	CP_GND	–	Power	Ground connection for the Charge Pump. Connect to analog GND.	
B4	LB_CONT	Analog	Input	Control voltage to set the loop bandwidth of the integrated Reclocker. Normally connected to VCO_GND through 40kΩ	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
B7	FW_EN/$\overline{DIS}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the noise immune Flywheel of the device. When set HIGH, the internal Flywheel is enabled. This Flywheel is used in the extraction and generation of TRS timing signals, in automatic video standards detection, and in manual switch line lock handling. When set LOW, the internal Flywheel is disabled and TRS correction and insertion is unavailable.
B8, F8, J8	IO_GND	–	Power	Ground connection for digital I/O buffers. Connect to digital GND.
C1	BUFF_VDD	–	Power	Power Supply connection for the Serial Digital Input buffers. Connect to +1.8V DC analog.
C2	PD_VDD	–	Power	Power Supply connection for the Phase Detector. Connect to +1.8V DC analog.
C3	PDBUFF_GND	–	Power	Ground connection for the Phase Detector and Serial Digital Input buffers. Connect to analog GND.
C6	MASTER/$\overline{SLAVE}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to determine the input / output selection for the DVB_ASI, SD/$\overline{HD}$, $\overline{RC\_BYP}$ and $\overline{SMPTE\_BYPASS}$ pins. When set HIGH, the GS1559 is set to operate in Master mode where SD/$\overline{HD}$, $\overline{RC\_BYP}$ and $\overline{SMPTE\_BYPASS}$ become status signal output pins set by the device. In this mode, the GS1559 will automatically detect, reclock, deserialize and process SD SMPTE and HD SMPTE input data. When set LOW, the GS1559 is set to operate in Slave mode where DVB_ASI, SD/$\overline{HD}$, $\overline{RC\_BYP}$ and $\overline{SMPTE\_BYPASS}$ become control signal input pins. In this mode, the application layer must set these external device pins for the correct reception of either SMPTE or DVB-ASI data. Slave mode also supports the reclocking and deserializing of data not conforming to SMPTE or DVB-ASI streams.
C7	$\overline{RC\_BYP}$	Non Synchronous	Input /Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be an input set by the application layer in Slave mode, and will be an output set by the device in Master mode. Master mode (MASTER/$\overline{SLAVE}$ = HIGH) The $\overline{RC\_BYP}$ signal will be HIGH only when the device has successfully locked to a SMPTE compliant input data stream. In this case, the serial digital loop-through output will be a reclocked version of the input. The $\overline{RC\_BYP}$ signal will be LOW whenever the input does not conform to a SMPTE compliant data stream. In this case, the serial digital loop-through output will be a buffered version of the input. Slave mode (MASTER/$\overline{SLAVE}$ = LOW) When set HIGH, the serial digital output will be a reclocked version of the input signal regardless of whether the device is in SMPTE, DVB-ASI or Data-Through mode. When set LOW, the serial digital output will be a buffered version of the input signal in all modes.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
C8	YANC	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of ancillary data in the video stream. HD Mode (SD/$\overline{HD}$ = LOW) The YANC signal will be HIGH when the device has detected VANC or HANC data in the luma video stream and LOW otherwise. SD Mode (SD/$\overline{HD}$ = LOW) For 20-bit demultiplexed data (20bit/$\overline{10bit}$ = HIGH), the YANC signal will be HIGH when VANC or HANC data is detected in the Luma video stream and LOW otherwise. For 10-bit multiplexed data (20bit/$\overline{10bit}$ = LOW), the YANC signal will be HIGH when VANC or HANC data is detected anywhere in the data stream and LOW otherwise.
D1, E1	DDI1, $\overline{DDI1}$	Analog	Input	Differential input pair for serial digital input 1.
D4	IP_SEL	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select DDI1 / $\overline{DDI1}$ or DDI2 / $\overline{DDI2}$ as the Serial Digital Input signal, and $\overline{CD1}$ or $\overline{CD2}$ as the Carrier Detect input signal. When set HIGH, DDI1 / $\overline{DDI1}$ is selected as the Serial Digital Input and $\overline{CD1}$ is selected as the Carrier Detect input signal. When set LOW, DDI2 / $\overline{DDI2}$ Serial Digital Input and $\overline{CD2}$ Carrier Detect input signal is selected.
D5	DVB_ASI	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be an input set by the application layer in Slave mode. This pin and its function are not supported in Master mode. Slave mode (MASTER/$\overline{SLAVE}$ = LOW) When set HIGH in conjunction with SD/$\overline{HD}$ = HIGH and $\overline{SMPTE\_BYPASS}$ = LOW, the device will be configured to operate in DVB-ASI mode. When set LOW, the device will not support the decoding or word alignment of received DVB-ASI data.
D6	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. The LOCKED signal will be HIGH whenever the device has correctly received and locked to SMPTE compliant data in SMPTE mode or DVB-ASI compliant data in DVB-ASI mode. It will be LOW otherwise.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
D8	CANC	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of ancillary data in the video stream. HD Mode (SD/$\overline{HD}$ = LOW) The CANC signal will be HIGH when the device has detected VANC or HANC data in the chroma video stream and LOW otherwise. SD Mode (SD/$\overline{HD}$ = LOW) For 20-bit demultiplexed data (20bit/$\overline{10bit}$ = HIGH), the CANC signal will be HIGH when VANC or HANC data is detected in the Chroma video stream and LOW otherwise. For 10-bit multiplexed data (20bit/$\overline{10bit}$ = LOW), the CANC signal will be HIGH when VANC or HANC data is detected anywhere in the data stream and LOW otherwise.
E2	TERM1	Analog	Input	Termination for Serial Digital Input 1. AC couple to EQ_GND.
E4	SD/$\overline{HD}$	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be an input set by the application layer in Slave mode, and will be an output set by the device in Master mode. Master mode (MASTER/$\overline{SLAVE}$ = HIGH) The SD/$\overline{HD}$ signal will be LOW whenever the received serial digital signal is 1.485Gb/s or 1.485/1.001Gb/s. The SD/$\overline{HD}$ signal will be HIGH whenever the received serial digital signal is 270Mb/s. Slave mode (MASTER/$\overline{SLAVE}$ = LOW) When set LOW, the device will be configured for the reception of 1.485Gb/s or 1.485/1.001Gb/s signals only and will not lock to any other serial digital signal. When set HIGH, the device will be configured for the reception of 270Mb/s signals only and will not lock to any other serial digital signal. NOTE: When in Slave mode, reset the device after the SD/$\overline{HD}$ input has been initially configured, and after each subsequent SD/HD data rate change. NOTE: This pin has an internal pull-up resistor of 100K.
E5, F5	CORE_GND	–	Power	Ground connection for the digital core logic. Connect to digital GND.
E6, F6	CORE_VDD	–	Power	Power Supply connection for the digital core logic. Connect to +1.8V DC digital.
F1	$\overline{CD1}$	Non Synchronous	Input	STATUS SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of a serial digital input signal. Normally generated by a Gennum automatic cable Equalizer. When LOW, the serial digital input signal received at the DDI1 and $\overline{DDI1}$ pins is considered valid. When HIGH, the associated serial digital input signal is considered to be invalid. In this case, the LOCKED signal is set LOW and all parallel outputs are muted.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
F4	20bit/$\overline{10bit}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select the output data bus width in SMPTE or Data-Through modes. This signal is ignored in DVB-ASI mode. When set HIGH, the parallel output will be 20-bit demultiplexed data. When set LOW, the parallel outputs will be 10-bit multiplexed data.	
F10, F9, G10, G9, H10, H9, J10, J9, K10, K9	DOUT[9:0]	Synchronous with PCLK	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DOUT9 is the MSB and DOUT0 is the LSB.	
				HD 20-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = HIGH	Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ =HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = LOW	Forced LOW in all modes.
				SD 20-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = HIGH	Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW Forced LOW in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = LOW	Forced LOW in all modes.
G1, H1	DDI2, $\overline{DDI2}$	Analog	Input	Differential input pair for serial digital input 2.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G4	IOPROC_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • EDH CRC Error Correction (SD-only) • ANC Data Checksum Correction • Line-based CRC Error Correction (HD-only) • Line Number Error Correction (HD-only) • TRS Error Correction • Illegal Code Remapping To enable a subset of these features, keep IOPROC_EN/$\overline{\text{DIS}}$ HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the Host Interface. When set LOW, the I/O processing features of the device are disabled, regardless of whether the features are enabled in the IOPROC_DISABLE register.
G5	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be an input set by the application layer in Slave mode, and will be an output set by the device in Master mode. Master mode (MASTER/$\overline{\text{SLAVE}}$ = HIGH) The $\overline{\text{SMPTE\_BYPASS}}$ signal will be HIGH only when the device has locked to a SMPTE compliant data stream. It will be LOW otherwise. Slave mode (MASTER/$\overline{\text{SLAVE}}$ = LOW) When set HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode. When set LOW, the device will not support the descrambling, decoding or word alignment of received SMPTE data. No I/O processing features will be available.
G6	$\overline{\text{RESET\_TRST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG test sequence. Host mode (JTAG/$\overline{\text{HOST}}$ = LOW) When asserted LOW, all functional blocks will be set to default conditions and all input and output signals become high-impedance, including the Serial Digital Outputs SDO and $\overline{\text{SDO}}$. Must be set HIGH for normal device operation. NOTE: When in Slave mode, reset the device after the SD/$\overline{\text{HD}}$ input has been initially configured, and after each subsequent SD/HD data rate change. JTAG test mode (JTAG/$\overline{\text{HOST}}$ = HIGH) When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G8	$\overline{\text{FIFO\_LD}}$	Synchronous with PCLK	Output	CONTROL SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used as a control signal for external FIFO(s). Normally HIGH but will go LOW for one PCLK period at SAV.
H2	TERM2	Analog	Input	Termination for serial digital input 2. AC couple to EQ_GND.
H4	$\overline{\text{CS}}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip Select/Test Mode Select Host mode (JTAG/$\overline{\text{HOST}}$ = LOW) $\overline{\text{CS}}$_TMS operates as the Host Interface Chip Select, $\overline{\text{CS}}$, and is active LOW. JTAG Test mode (JTAG/$\overline{\text{HOST}}$ = HIGH) $\overline{\text{CS}}$_TMS operates as the JTAG Test Mode Select, TMS, and is active HIGH. NOTE: If the Host Interface is not being used, tie this pin HIGH.
H5	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Clock/Test Clock. Host mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the Host Interface Burst Clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SCLK_TCK operates as the JTAG test clock, TCK. NOTE: If the Host Interface is not being used, tie this pin HIGH.
H6	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Output/Test Data Output Host mode (JTAG/$\overline{\text{HOST}}$ = LOW) SDOUT_TDO operates as the Host Interface Serial Digital Output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SDOUT_TDO operates as the JTAG test data output, TDO.
H7	$\overline{\text{DATA\_ERROR}}$	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. The $\overline{\text{DATA\_ERROR}}$ signal will be LOW when an error within the received data stream has been detected by the device. This pin is a logical 'OR'ing of all detectable errors listed in the internal ERROR_STATUS register. Once an error is detected, $\overline{\text{DATA\_ERROR}}$ will remain LOW until the start of the next video frame/field, or until the ERROR_STATUS register is read via the Host Interface. The $\overline{\text{DATA\_ERROR}}$ signal will be HIGH when the received data stream has been detected without error. NOTE: It is possible to program which error conditions are monitored by the device by setting appropriate bits of the ERROR_MASK register HIGH. All error conditions are detected by default.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H8	H	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the portion of the video line containing active video data. H signal timing is configurable via the H_CONFIG bit of the IOPROC_DISABLE register accessible via the Host Interface. Active Line Blanking (H_CONFIG = 0_h) The H signal will be HIGH for the entire Horizontal blanking period, including the EAV and SAV TRS words, and LOW otherwise. This is the default setting. TRS Based Blanking (H_CONFIG = 1_h) The H signal will be HIGH for the entire Horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise.
J1	$\overline{CD2}$	Non Synchronous	Input	STATUS SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of a serial digital input signal. Normally generated by a Gennum automatic Cable Equalizer. When LOW, the serial digital input signal received at the DDI2 and $\overline{DDI2}$ pins is considered valid. When HIGH, the associated serial digital input signal is considered to be invalid. In this case, the LOCKED signal is set LOW and all parallel outputs are muted.
J5	SDO_EN/$\overline{DIS}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the serial digital output loop-through stage. When set LOW, the Serial Digital Output signals SDO and $\overline{SDO}$ are disabled and become high-impedance. When set HIGH, the Serial Digital Output signals SDO and $\overline{SDO}$ are enabled.
J6	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data In/Test Data Input Host mode (JTAG/$\overline{HOST}$ = LOW) SDIN_TDI operates as the Host Interface Serial Digital Input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH) SDIN_TDI operates as the JTAG test data input, TDI. NOTE: If the Host Interface is not being used, tie this pin HIGH.
J7	V	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the portion of the video field/frame that is used for Vertical blanking. The V signal will be HIGH for the entire Vertical blanking period as indicated by the V bit in the received TRS signals. The V signal will be LOW for all lines outside of the Vertical blanking interval.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
K1	RSET	Analog	Input	Used to set the serial digital loop-through output signal amplitude. Connect to CD_VDD through 281Ω +/- 1% for 800mV$_{p-p}$ single-ended output swing.
K2	CD_VDD	–	Power	Power Supply connection for the serial digital Cable Driver. Connect to +1.8V DC analog.
K3, K4	SDO, $\overline{\text{SDO}}$	Analog	Output	Serial digital loop-through output signal operating at 1.485Gb/s, 1.485/1.001Gb/s, or 270Mb/s. The slew rate of these outputs is automatically controlled to meet SMPTE 292M and 259M requirements according to the setting of the SD/$\overline{\text{HD}}$ pin.
K5	CD_GND	–	Power	Ground connection for the serial digital Cable Driver. Connect to analog GND.
K6	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG Test mode or Host Interface mode. When set HIGH, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured as GSPI pins for normal Host Interface operation.
K7	F	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the ODD/EVEN field of the video signal. The F signal will be HIGH for the entire period of field 2 as indicated by the F bit in the received TRS signals. The F signal will be LOW for all lines in field 1 and for all lines in progressive scan systems.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +4.6V
Input Voltage Range (any input)	-2.0V to + 5.25V
Ambient Operating Temperature	-20°C ≤ T_A ≤ 85°C
Storage Temperature	-40°C ≤ T_{STG} ≤ 125°C
ESD Protection On All Pins (see Note 1)	1kV

NOTES:

1. HBM, per JESDA-114B.

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Level	Notes
System								
Operation Temperature Range	T_A	–	0	–	70	°C	3	1
Digital Core Supply Voltage	CORE_VDD	–	1.71	1.8	1.89	V	3	1
Digital I/O Supply Voltage	IO_VDD	–	3.13	3.3	3.47	V	3	1
Charge Pump Supply Voltage	CP_VDD	–	3.13	3.3	3.47	V	3	1
Phase Detector Supply Voltage	PD_VDD	–	1.71	1.8	1.89	V	3	1
Input Buffer Supply Voltage	BUFF_VDD	–	1.71	1.8	1.89	V	3	1
Cable Driver Supply Voltage	CD_VDD	–	1.71	1.8	1.89	V	3	1
External VCO Supply Voltage Output	VCO_VCC	–	2.25	–	2.75	V	1	–
+1.8V Supply Current	I_{1V8}	SDO Enabled	–	–	245	mA	3	4
+3.3V Supply Current	I_{3V3}	–	–	–	55	mA	3	5

Table 2-1: DC Electrical Characteristics (Continued)

T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Level	Notes
Total Device Power	P_D	SDO Enabled	–	–	550	mW	3	–
	P_D	SDO Disabled	–	–	450	mW	3	–
Digital I/O								
Input Logic LOW	V_{IL}	–	–	–	0.8	V	4	–
Input Logic HIGH	V_{IH}	–	2.1	–	–	V	4	–
Output Logic LOW	V_{OL}	+8mA	–	0.2	0.4	V	4	–
Output Logic HIGH	V_{OH}	-8mA	IO_VDD - 0.4	–	–	V	4	–
Input								
Input Bias Voltage	V_B	–	–	1.45	–	V	1	2
RSET Voltage	V_{RSET}	RSET=281Ω	0.54	0.6	0.66	V	1	3
Output								
Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET=281Ω, SD and HD	0.8	1.0	1.2	V	1	–

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. All DC and AC electrical parameters within specification.
2. Input common mode is set by internal biasing resistors.
3. Set by the value of the RSET resistor.
4. Sum of all 1.8V supplies.
5. Sum of all 3.3V supplies.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Level	Notes
System								
Serial Digital Input Jitter Tolerance	IJT	Nominal loop bandwidth	0.6	–	–	UI	1	1
Master Mode Asynchronous Lock Time		No data to HD	–	–	468	us	6,7	2
		HD to SD	–	–	260	us	6,7	2
		No data to SD	–	–	340	us	6,7	2
		SD to HD	–	–	256	us	6,7	2
		No data to DVB-ASI	–	–	65	us	6,7	2
Slave Mode Asynchronous Lock Time		No data to HD	–	–	240	us	6,7	2
		No data to SD	–	–	197	us	6,7	2
		No data to DVB-ASI	–	–	68	us	6,7	2
Device Latency		10-bit SD	–	21	–	PCLK	8	–
		20-bit HD	–	19	–	PCLK	8	–
		DVB-ASI	–	11	–	PCLK	8	–
Reset Pulse Width	t_{reset}	–	1	–	–	ms	8	4
Serial Digital Differential Input								
Serial Input Data Rate	DR_{DDI}	–	–	1.485	–	Gb/s	1	–
		–	–	1.485/1.001	–	Gb/s	9	–
		–	–	270	–	Mb/s	1	–
Serial Digital Input Signal Swing	ΔV_{DDI}	Differential with internal 100Ω input termination	200	600	1000	mV_{p-p}	1	–
Serial Digital Output								
Serial Output Data Rate	DR_{SDO}	–	–	1.485	–	Gb/s	1	–
		–	–	1.485/1.001	–	Gb/s	9	–
		–	–	270	–	Mb/s	1	–
Serial Output Swing	ΔV_{SDO}	RSET = 281Ω Load = 75Ω	650	800	950	mVp-p	1	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	HD signal	–	–	260	ps	1	–
		SD signal	400	550	1500	ps	1	–
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	HD signal	–	–	260	ps	1	–
		SD signal	400	550	1500	ps	1	–

Table 2-2: AC Electrical Characteristics (Continued)

T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Level	Notes
Serial Output Intrinsic Jitter	t_{IJ}	Pseudorandom and pathological HD signal	–	90	125	ps	5	3
		Pseudorandom and pathological SD signal	–	270	350	ps	5	3
Parallel Output								
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	4	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	50	60	%	4	–
Output Data Hold Time	t_{OH}	20-bit HD, 15pF	1.0	–	–	ns	4	–
		10-bit SD, 15pF	19.5	–	–	ns	8	–
Output Data Delay Time	t_{OD}	20-bit HD, 15pF	–	–	4.5	ns	4	–
		10-bit SD, 15pF	–	–	22.8	ns	8	–
Output Data Rise/Fall Time	tr/tf	–	–	–	1.5	ns	3	–
GSPI								
GSPI Input Clock Frequency	f_{SCLK}	–	–	–	6.6	MHz	8	–
GSPI Input Clock Duty Cycle	DC_{SCLK}	–	40	–	60	%	8	–
GSPI Input Data Setup Time	–	–	0	–	–	ns	8	–
GSPI Input Data Hold Time	–	–	1.43	–	–	ns	8	–
GSPI Output Data Hold Time	–	–	2.1	–	–	ns	8	–
GSPI Output Data Delay Time	–	–	–	–	7.27	ns	8	–

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. 6MHz sinewave modulation.
2. HD = 1080i, SD = 525i
3. Serial Digital Output Reclocked ($\overline{RC\_BYP}$ = HIGH).
4. See Device Reset on page 64, Figure 4-16.

3. Input/Output Circuits

All resistors in ohms, all capacitors in farads, unless otherwise shown.

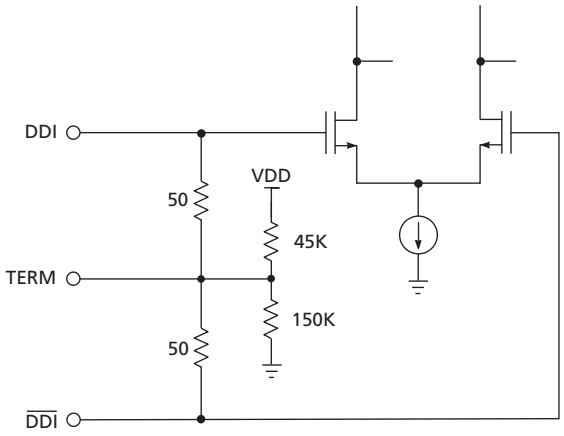

Figure 3-1: Serial Digital Input

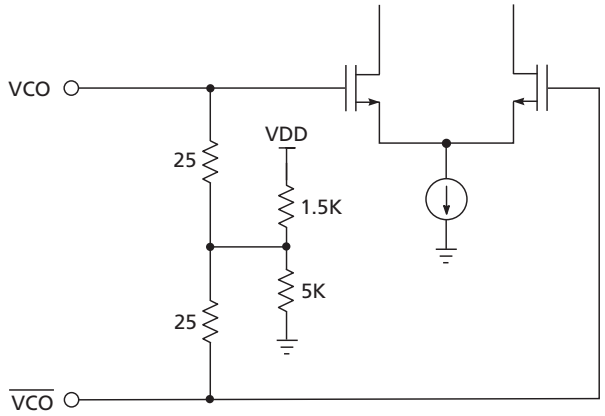

Figure 3-2: VCO Input

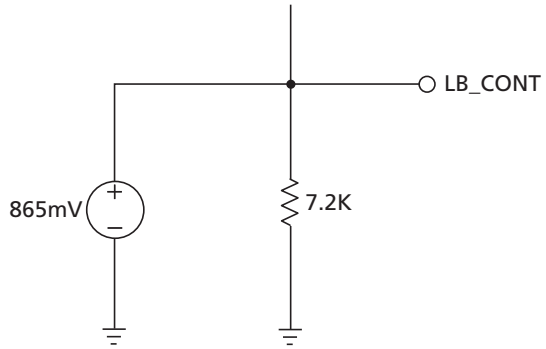

Figure 3-3: PLL Loop Bandwidth Control

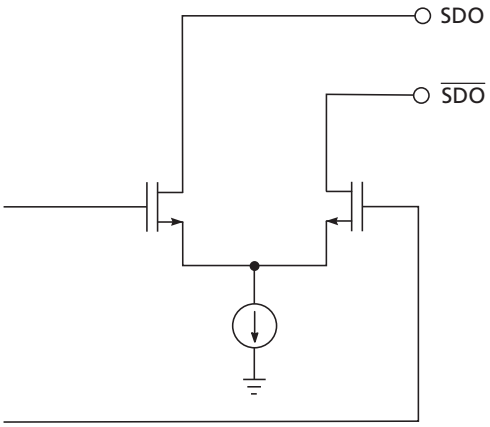

Figure 3-4: Serial Digital Output

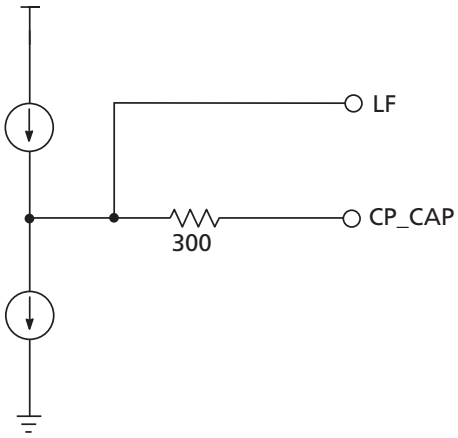

Figure 3-5: VCO Control Output & PLL Lock Time Capacitor

3.1 Host Interface Map

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROR_MASK	01Ah	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ ERR_ MASK	FF_CRC_ ERR_ MASK	AP_CRC_ ERR_ MASK	LOCK_ ERR_ MASK	CCS_ERR_MASK	YCS_ERR_MASK	CCRC_ ERR_ MASK	YCRC_ ERR_ MASK	LNUM_ERR_ MASK	SAV_ERR_MASK	EAV_ERR_MASK
FF_LINE_END_F1	019h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1	018h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0	017h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0	016h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1	015h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1	014h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0	013h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0	012h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE4	011h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3	010h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2	00Fh	Not Used	Not Used	Not Used	Not Used	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1	00Eh	Not Used	Not Used	Not Used	Not Used	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B	00Dh	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A	00Ch	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	00Bh																
	00Ah																
ANC_TYPE5	009h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE4	008h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE3	007h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE2	006h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE1	005h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_STANDARD	004h	Not Used	VDS-b4	VDS-b3	VDS-b2	VDS-b1	VDS-b0	INT_PROG	STD_ LOCK	CDF-b3	CDF-b2	CDF-b1	CDF-b0	YDF-b3	YDF-b2	YDF-b1	YDF-b0
EDH_FLAG	003h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	002h																
ERROR_STATUS	001h	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ ERR	FF_CRC_ ERR	AP_CRC_ ERR	LOCK_ ERR	CCS_ERR	YCS_ERR	CCRC_ ERR	YCRC_ ERR	LNUM_ERR	SAV_ERR	EAV_ERR
IOPROC_DISABLE	000h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	H_CONFIG	Not Used	Not Used	ILLEGAL_REMAP	EDH_CRC_INS	ANC_ CSUM_INS	CRC_INS	LNUM_ INS	TRS_INS

3.1.1 Host Interface Map (R/W Configurable Registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROR_MASK	01Ah						VD_STD_ ERR_ MASK	FF_CRC_ ERR_ MASK	AP_CRC_ ERR_ MASK	LOCK_ ERR_ MASK	CCS_ERR_MASK	YCS_ERR_MASK	CCRC_ ERR_ MASK	YCRC_ ERR_ MASK	LNUM_ERR_ MASK	SAV_ERR_MASK	EAV_ERR_MASK
FF_LINE_END_F1	019h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1	018h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0	017h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0	016h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1	015h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1	014h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0	013h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0	012h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	011h																
	010h																
	00Fh																
	00Eh																
	00Dh																
	00Ch																
	00Bh																
	00Ah																
ANC_TYPE5	009h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE4	008h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE3	007h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE2	006h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE1	005h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	004h																
	003h																
	002h																
	001h																
IOPROC_DISABLE	000h								H_CONFIG			ILLEGAL_REMAP	EDH_CRC_INS	ANC_ CSUM_INS	CRC_INS	LNUM_ INS	TRS_INS

3.1.2 Host Interface Map (Read Only Registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	01Ah																
	019h																
	018h																
	017h																
	016h																
	015h																
	014h																
	013h																
	012h																
RASTER_STRUCTURE4	011h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3	010h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2	00Fh					b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1	00Eh					b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B	00Dh	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A	00Ch	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	00Bh																
	00Ah																
	009h																
	008h																
	007h																
	006h																
	005h																
VIDEO_STANDARD	004h		VDS-b4	VDS-b3	VDS-b2	VDS-b1	VDS-b0	INT_PROG	STD_ LOCK	CDF-b3	CDF-b2	CDF-b1	CDF-b0	YDF-b3	YDF-b2	YDF-b1	YDF-b0
EDH_FLAG	003h		ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	002h																
ERROR_STATUS	001h						VD_STD_ ERR	FF_CRC_ ERR	AP_CRC_ ERR	LOCK_ ERR	CCS_ERR	YCS_ERR	CCRC_ ERR	YCRC_ ERR	LNUM_ERR	SAV_ERR	EAV_ERR
	000h																

4. Detailed Description

4.1 Functional Overview

The GS1559 is a multi-rate reclocking Deserializer with an integrated serial digital loop-through output. When used in conjunction with the multi-rate GS1574 Adaptive Cable Equalizer and the external GO1555/GO1525* Voltage Controlled Oscillator, a receive solution at 1.485Gb/s, 1.485/1.001Gb/s or 270Mb/s is realized.

The device has two basic modes of operation which determine precisely how SMPTE or DVB-ASI compliant input data streams are reclocked and processed.

In Master mode, (MASTER/$\overline{\text{SLAVE}}$ = HIGH), the GS1559 will automatically detect, reclock, deserialize and process SD SMPTE 259M-C or HD SMPTE 292M input data.

In Slave mode, (MASTER/$\overline{\text{SLAVE}}$ = LOW), the application layer must set external device pins for the correct reception of either SMPTE or DVB-ASI data. Slave mode also supports the reclocking and deserializing of data not conforming to SMPTE or DVB-ASI streams.

The provided serial loop-through outputs may be selected as either buffered or reclocked versions of the input signal, and feature a high-impedance mode, output mute on loss of signal and adjustable signal swing.

In the digital signal processing core, several data processing functions are implemented, including error detection and correction, and automatic video standards detection. These features are all enabled by default, but may be individually disabled via internal registers accessible through the GSPI Host Interface.

Finally, the GS1559 contains a JTAG interface for boundary scan test implementations.

*For new designs use the GO1555.

4.2 Serial Digital Input

The GS1559 contains two current mode differential serial digital input buffers, allowing the device to be connected to two SMPTE 259M-C or 292M compliant input signals.

Both input buffers have internal 50Ωtermination resistors which are connected to ground via the TERM1 and TERM2 pins. The input common mode level is set by internal biasing resistors such that the serial digital input signals must be AC coupled into the device. Gennum recommends using a capacitor value of 4.7µF to accommodate pathological signals.

The input buffers use a separate power supply of +1.8V DC supplied via the BUFF_VDD and PDBUFF_GND pins.

4.2.1 Input Signal Selection

A 2x1 input Multiplexer is provided to allow the application layer to select between the two serial digital input streams using a single external pin. When IP_SEL is set HIGH,