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GS1560A/GS1561 HD-LINX® II Dual-Rate Deserializer

Key Features

- SMPTE 292M and SMPTE 259M-C compliant descrambling and NRZI → NRZ decoding (with bypass)
- DVB-ASI 8b/10b decoding
- auto-configuration for HD-SDI and SD-SDI
- serial loop-through cable driver output selectable as reclocked or non-reclocked (GS1560A only)
- dual serial digital input buffers with 2 x 1 mux
- integrated serial digital signal termination
- integrated reclocker
- automatic or manual rate selection / indication (HD/SD)
- descrambler bypass option
- user selectable additional processing features including:
  - CRC, TRS, ANC data checksum, line number and EDH CRC error detection and correction
  - programmable ANC data detection
  - illegal code remapping
- internal flywheel for noise immune H, V, F extraction
- FIFO load Pulse
- 20-bit / 10-bit CMOS parallel output data bus
- 148.5MHz / 74.25MHz / 27MHz / 13.5MHz parallel digital output
- automatic standards detection and indication
- Pb-free and RoHS Compliant
- 1.8V core power supply and 3.3V charge pump power supply
- 3.3V digital I/O supply
- JTAG test interface
- small footprint compatible with GS9060, GS1532, and GS9062

Applications

- SMPTE 292M Serial Digital Interfaces
- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS1560A/GS1561 is a reclocking deserializer. When used in conjunction with the GS1524 Automatic Cable Equalizer and the GO1555/GO1525* Voltage Controlled Oscillator, a receive solution can be realized for HD-SD, SD-SDI and DVB-ASI applications.

In addition to reclocking and deserializing the input data stream, the GS1560A/GS1561 performs NRZI-to-NRZ decoding, descrambling as per SMPTE 259M-C/292M, and word alignment when operating in SMPTE mode. When operating in DVB-ASI mode, the device will word align the data to K28.5 sync characters and 8b/10b decode the received stream.

Two serial digital input buffers are provided with a 2x1 multiplexer to allow the device to select from one of two serial digital input signals.

The integrated reclocker features a very wide Input Jitter Tolerance of ±0.3 UI (total 0.6 UI), a rapid asynchronous lock time, and full compliance with DVB-ASI data streams.

The GS1560A includes an integrated cable driver is for serial input loop-through applications. It can be selected to output either buffered or reclocked data. The cable driver also features an output mute on loss of signal, high impedance mode, adjustable signal swing, and automatic dual slew-rate selection depending on HD/SD operational requirements.

The GS1560A/GS1561 also includes a range of data processing functions such as error detection and correction, automatic standards detection, and EDH support. The device can also detect and extract SMPTE 352M payload identifier packets and independently identify the received video standard. This information is read from internal registers via the host interface port.

Line-based CRC errors, line number errors, TRS errors, EDH CRC errors and ancillary data checksum errors can all be detected.

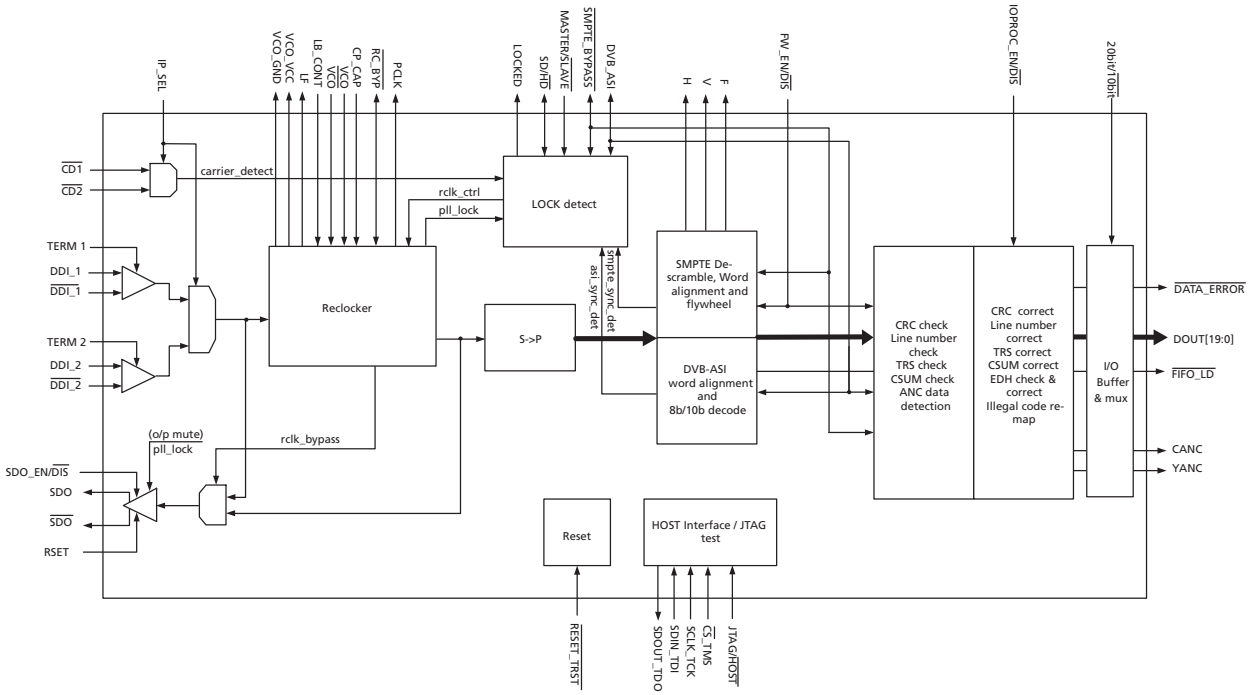
Finally, the device can correct detected errors and insert new TRS ID words, line-based CRC words, ancillary data checksum words, EDH CRC words, and line numbers. Illegal code re-mapping is also available. All processing functions may be individually enabled or disabled via host interface control.

The GS1560A/GS1561 is Pb-free and the encapsulation compound does not contain halogenated flame retardant.

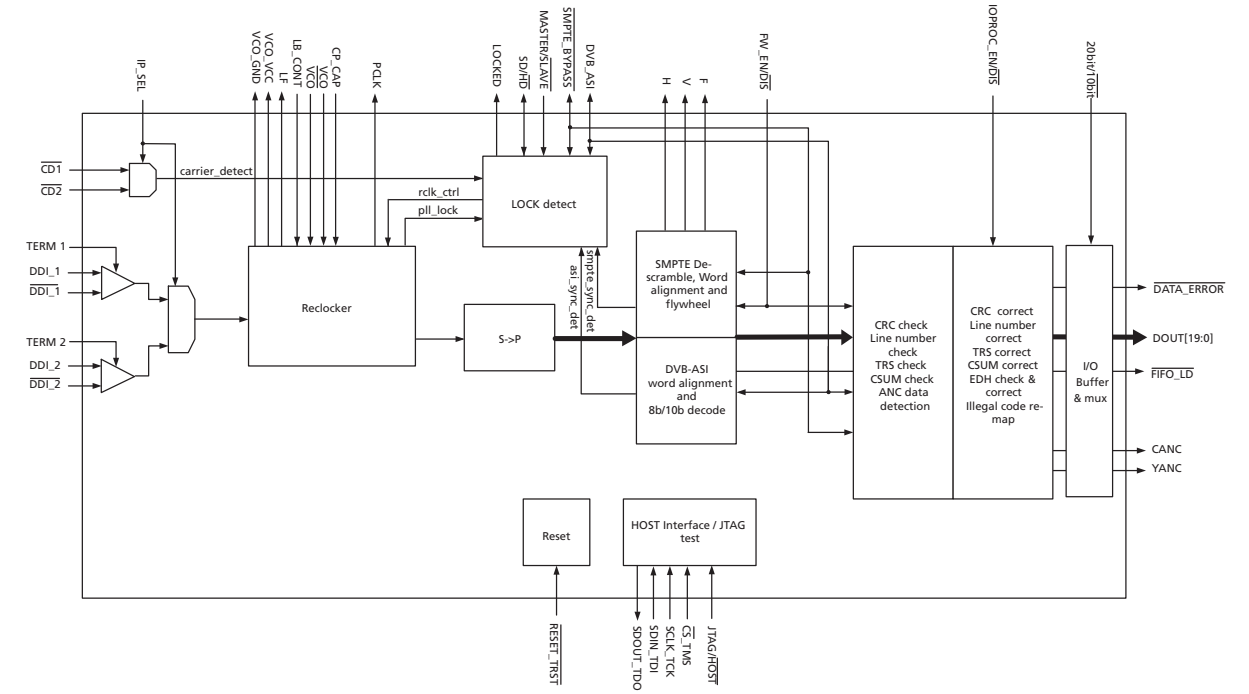
This component and all homogeneous subcomponents are RoHS compliant.

*For new designs use GO1555

Functional Block Diagrams



GS1560A Functional Block Diagram



GS1561 Functional Block Diagram

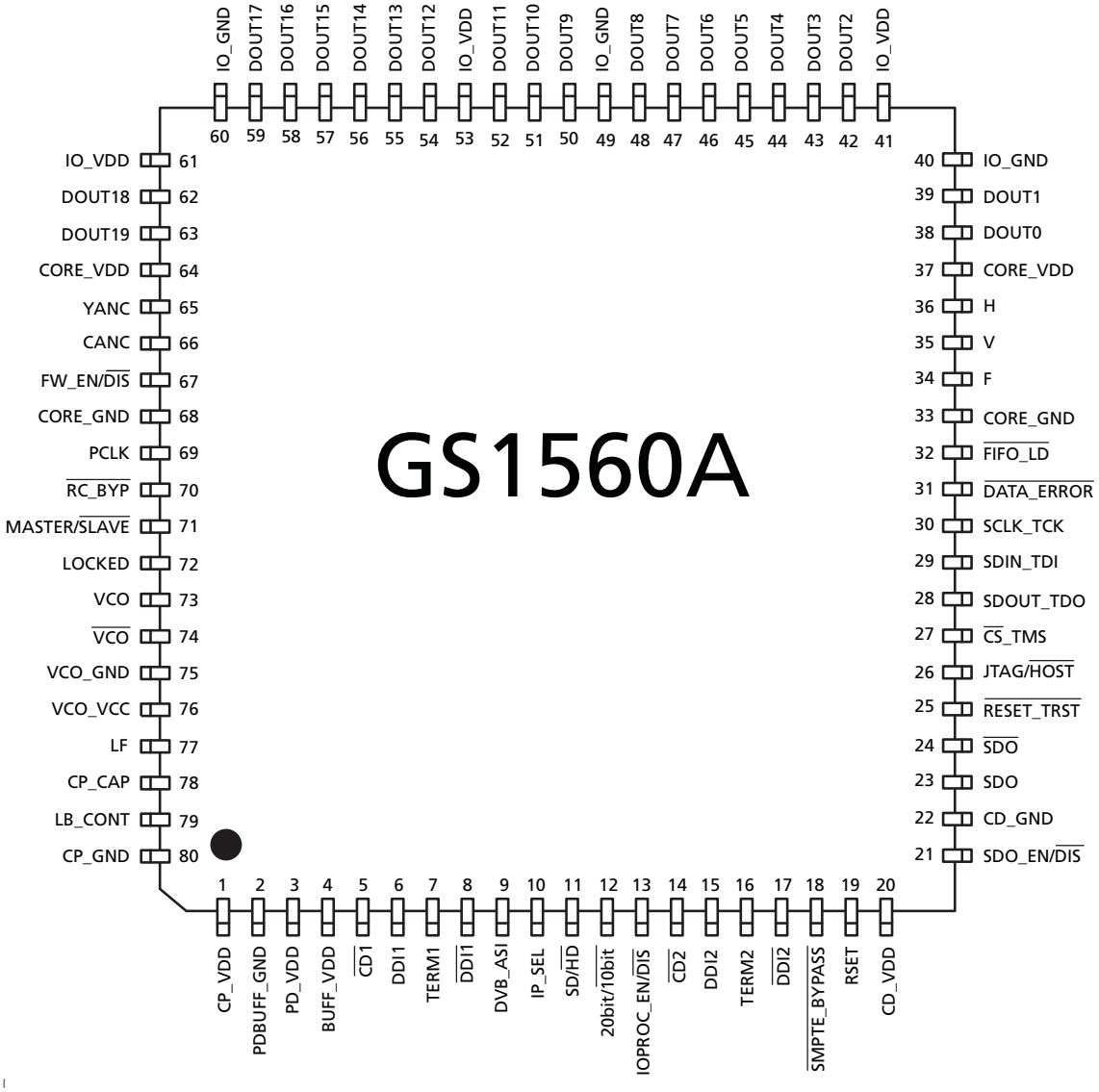
Revision History

Version	ECR	PCN	Date	Changes and / or Modifications
12	152053	–	June 2009	Removed 'Proprietary & Confidential' from the footer.
11	150195	50711	July 2008	DVB_ASI operation specification change in Master mode.
10	143666	42774	January 2007	Recommended the new GO1555 VCO for new designs.
9	140423	39452	May 2006	Corrected minor typing errors in Functional Block Diagram. Modified video format numbers for system 1125 on Table 4-4: Switch Line Position for Digital Systems.
8	137405	–	September 2005	Conversion to Data Sheet. Added note on max device power and current to Table 2-1: DC Electrical Characteristics. Corrected Solder Reflow Profile labels.
7	136978	–	June 2005	Restored missing overlines to pin names. Corrected missing TERM pin in Serial Digital Input connection diagram. Rephrased RoHS compliance statement.
6	134906	–	April 2005	Added Solder Reflow Profile description. Clarified setting of VD_STD[4:0], INT_$\overline{\text{PROG}}$ and STD_LOCK bits following a reset and/or removal of input. Minor correction to Typical Application Circuits for both parts. Added DVB-ASI Packet Counter information. Added Packaging Data section. Changed 'Green' references to RoHS Compliant.

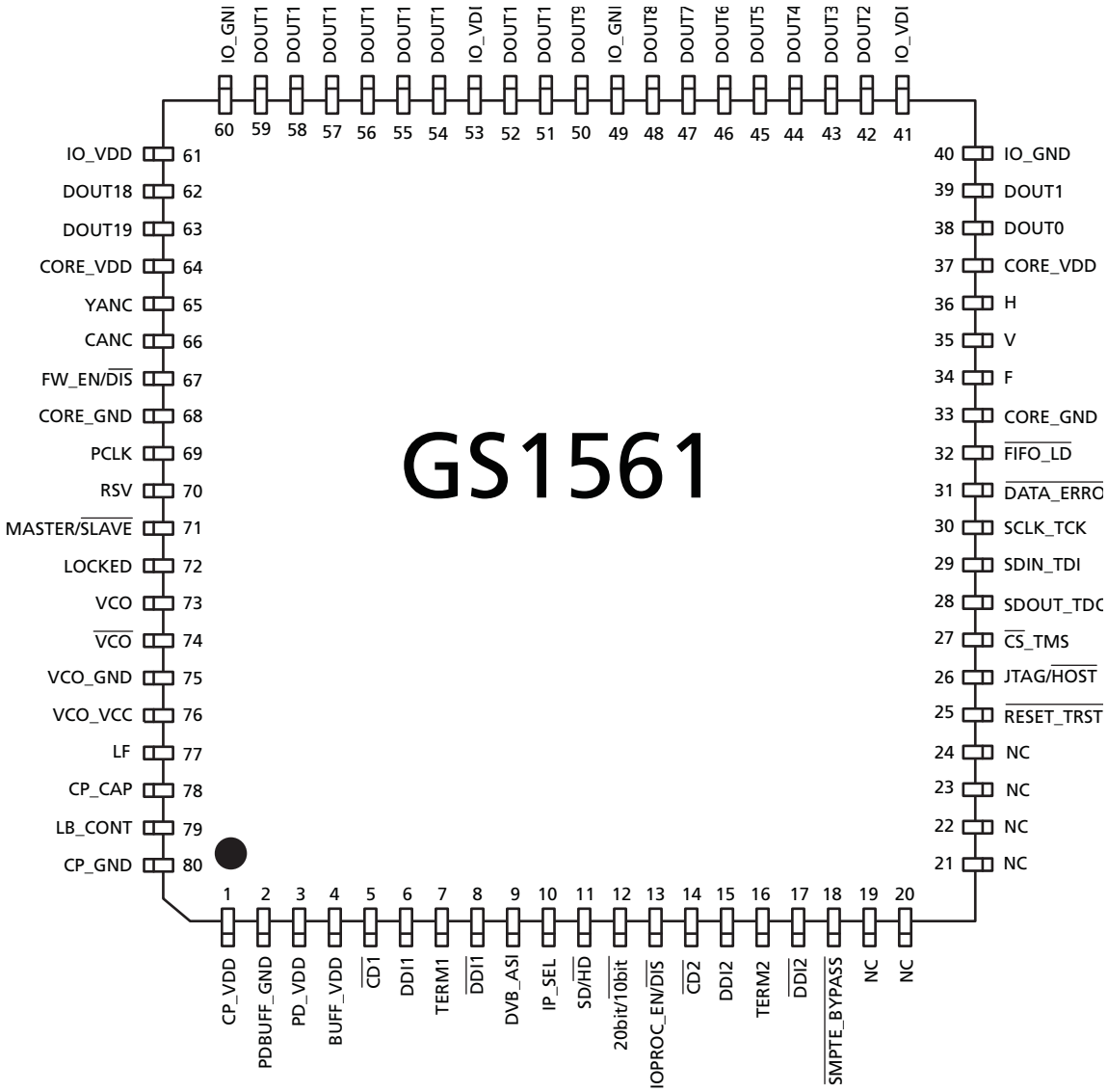
Contents

1. Pin Out

1.1 Pin Assignment GS1560A



1.2 Pin Assignment GS1561



1.3 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	CP_VDD	–	Power	Power supply connection for the charge pump. Connect to +3.3V DC analog.
2	PDBUFF_GND	–	Power	Ground connection for the phase detector and serial digital input buffers. Connect to analog GND.
3	PD_VDD	–	Power	Power supply connection for the phase detector. Connect to +1.8V DC analog.
4	BUFF_VDD	–	Power	Power supply connection for the serial digital input buffers. Connect to +1.8V DC analog.
5	$\overline{\text{CD1}}$	Non Synchronous	Input	STATUS SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of a serial digital input signal. Normally generated by a Gennum automatic cable equalizer. When LOW, the serial digital input signal received at the DDI1 and $\overline{\text{DDI1}}$ pins is considered valid. When HIGH, the associated serial digital input signal is considered to be invalid. In this case, the LOCKED signal is set LOW and all parallel outputs are muted.
6, 8	DDI1, $\overline{\text{DDI1}}$	Analog	Input	Differential input pair for serial digital input 1.
7	TERM1	Analog	Input	Termination for serial digital input 1. AC couple to EQ_GND.
9	DVB_ASI	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be an input set by the application layer in slave mode. This pin and its function are not supported in Master mode. Slave Mode (MASTER/$\overline{\text{SLAVE}}$ = LOW) When set HIGH in conjunction with SD/$\overline{\text{HD}}$ = HIGH and $\overline{\text{SMPTE\_BYPASS}}$ = LOW, the device will be configured to operate in DVB-ASI mode. When set LOW, the device will not support the decoding or word alignment of received DVB-ASI data.
10	IP_SEL	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select DDI1 / $\overline{\text{DDI1}}$ or DDI2 / $\overline{\text{DDI2}}$ as the serial digital input signal, and $\overline{\text{CD1}}$ or $\overline{\text{CD2}}$ as the carrier detect input signal. When set HIGH, DDI1 / $\overline{\text{DDI1}}$ is selected as the serial digital input and $\overline{\text{CD1}}$ is selected as the carrier detect input signal. When set LOW, DDI2 / $\overline{\text{DDI2}}$ serial digital input and $\overline{\text{CD2}}$ carrier detect input signal is selected.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
11	SD/$\overline{\text{HD}}$	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be an input set by the application layer in slave mode, and will be an output set by the device in master mode. Master Mode (MASTER/$\overline{\text{SLAVE}}$ = HIGH) The SD/$\overline{\text{HD}}$ signal will be LOW whenever the received serial digital signal is 1.485Gb/s or 1.485/1.001Gb/s. The SD/$\overline{\text{HD}}$ signal will be HIGH whenever the received serial digital signal is 270Mb/s. Slave Mode (MASTER/$\overline{\text{SLAVE}}$ = LOW) When set LOW, the device will be configured for the reception of 1.485Gb/s or 1.485/1.001Gb/s signals only and will not lock to any other serial digital signal. When set HIGH, the device will be configured for the reception of 270Mb/s signals only and will not lock to any other serial digital signal. NOTE: When in slave mode, reset the device after the SD/$\overline{\text{HD}}$ input has been initially configured, and after each subsequent SD/HD data rate change. NOTE: This pin has an internal pull-up resistor of 100K.
12	20bit/$\overline{\text{10bit}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select the output data bus width in SMPTE or Data-Through modes. This signal is ignored in DVB-ASI mode. When set HIGH, the parallel output will be 20-bit demultiplexed data. When set LOW, the parallel outputs will be 10-bit multiplexed data.
13	IOPROC_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • EDH CRC Error Correction (SD-only) • ANC Data Checksum Correction • Line-based CRC Error Correction (HD-only) • Line Number Error Correction (HD-only) • TRS Error Correction • Illegal Code Remapping To enable a subset of these features, keep IOPROC_EN/$\overline{\text{DIS}}$ HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When set LOW, the I/O processing features of the device are disabled, regardless of whether the features are enabled in the IOPROC_DISABLE register.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
14	$\overline{\text{CD2}}$	Non Synchronous	Input	STATUS SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of a serial digital input signal. Normally generated by a Gennum automatic cable equalizer. When LOW, the serial digital input signal received at the DDI2 and $\overline{\text{DDI2}}$ pins is considered valid. When HIGH, the associated serial digital input signal is considered to be invalid. In this case, the LOCKED signal is set LOW and all parallel outputs are muted.
15, 17	DDI2, $\overline{\text{DDI2}}$	Analog	Input	Differential input pair for serial digital input 2.
16	TERM2	Analog	Input	Termination for serial digital input 2. AC couple to PDBUFF_GND.
18	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be an input set by the application layer in slave mode, and will be an output set by the device in master mode. Master Mode (MASTER/$\overline{\text{SLAVE}}$ = HIGH) The $\overline{\text{SMPTE\_BYPASS}}$ signal will be HIGH only when the device has locked to a SMPTE compliant data stream. It will be LOW otherwise. Slave Mode (MASTER/$\overline{\text{SLAVE}}$ = LOW) When set HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode. When set LOW, the device will not support the descrambling, decoding or word alignment of received SMPTE data. No I/O processing features will be available.
19	RSET	Analog	Input	GS1560A Used to set the serial digital loop-through output signal amplitude. Connect to CD_VDD through 281Ω +/- 1% for 800mV_{p-p} single-ended output swing.
	NC	–	–	GS1561 No Connect.
20	CD_VDD	–	Power	GS1560A Power supply connection for the serial digital cable driver. Connect to +1.8V DC analog.
	NC	–	–	GS1561 No Connect.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
21	SDO_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	GS1560A CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the serial digital output loop-through stage. When set LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When set HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled.
	NC	–	–	GS1561 No Connect.
22	CD_GND	–	Power	GS1560A Ground connection for the serial digital cable driver. Connect to analog GND.
	NC	–	–	GS1561 No Connect.
23, 24	SDO, $\overline{\text{SDO}}$	Analog	Output	GS1560A Serial digital loop-through output signal operating at 1.485Gb/s, 1.485/1.001Gb/s, or 270Mb/s. The slew rate of these outputs is automatically controlled to meet SMPTE 292M and 259M specifications according to the setting of the SD/$\overline{\text{HD}}$ pin.
	NC	–	–	GS1561 No Connect.
25	$\overline{\text{RESET\_TRST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG test sequence. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) When asserted LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance, including the serial digital outputs SDO and $\overline{\text{SDO}}$. Must be set HIGH for normal device operation. NOTE: When in slave mode, reset the device after the SD/$\overline{\text{HD}}$ input has been initially configured, and after each subsequent SD/HD data rate change. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
26	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured as GSPI pins for normal host interface operation.
27	$\overline{\text{CS}}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip Select / Test Mode Select Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) $\overline{\text{CS}}$_TMS operates as the host interface chip select, $\overline{\text{CS}}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) $\overline{\text{CS}}$_TMS operates as the JTAG test mode select, TMS, and is active HIGH. NOTE: If the host interface is not being used, tie this pin HIGH.
28	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SDOUT_TDO operates as the JTAG test data output, TDO.
29	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data In / Test Data Input Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SDIN_TDI operates as the JTAG test data input, TDI. NOTE: If the host interface is not being used, tie this pin HIGH.
30	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Clock / Test Clock. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SCLK_TCK operates as the JTAG test clock, TCK. NOTE: If the host interface is not being used, tie this pin HIGH.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
31	$\overline{\text{DATA\_ERROR}}$	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. The $\overline{\text{DATA\_ERROR}}$ signal will be LOW when an error within the received data stream has been detected by the device. This pin is a logical 'OR'ing of all detectable errors listed in the internal ERROR_STATUS register. Once an error is detected, $\overline{\text{DATA\_ERROR}}$ will remain LOW until the start of the next video frame / field, or until the ERROR_STATUS register is read via the host interface. The $\overline{\text{DATA\_ERROR}}$ signal will be HIGH when the received data stream has been detected without error. NOTE: It is possible to program which error conditions are monitored by the device by setting appropriate bits of the ERROR_MASK register HIGH. All error conditions are detected by default.
32	$\overline{\text{FIFO\_LD}}$	Synchronous with PCLK	Output	CONTROL SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used as a control signal for external FIFO(s). Normally HIGH but will go LOW for one PCLK period at SAV.
33, 68	CORE_GND	–	Power	Ground connection for the digital core logic. Connect to digital GND.
34	F	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the ODD / EVEN field of the video signal. The F signal will be HIGH for the entire period of field 2 as indicated by the F bit in the received TRS signals. The F signal will be LOW for all lines in field 1 and for all lines in progressive scan systems.
35	V	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the portion of the video field / frame that is used for vertical blanking. The V signal will be HIGH for the entire vertical blanking period as indicated by the V bit in the received TRS signals. The V signal will be LOW for all lines outside of the vertical blanking interval.
36	H	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the portion of the video line containing active video data. H signal timing is configurable via the H_CONFIG bit of the IOPROC_DISABLE register accessible via the host interface. Active Line Blanking (H_CONFIG = 0_h) The H signal will be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words, and LOW otherwise. This is the default setting. TRS Based Blanking (H_CONFIG = 1_h) The H signal will be HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
37, 64	CORE_VDD	–	Power	Power supply connection for the digital core logic. Connect to +1.8V DC digital.	
38, 39, 42-48, 50	DOUT[0:9]	Synchronous with PCLK	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DOUT9 is the MSB and DOUT0 is the LSB.	
				HD 20-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = HIGH	Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ =HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = LOW	Forced LOW in all modes.
				SD 20-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = HIGH	Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW Forced LOW in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = LOW	Forced LOW in all modes.
40, 49, 60	IO_GND	–	Power	Ground connection for digital I/O buffers. Connect to digital GND.	
41, 53, 61	IO_VDD	–	Power	Power supply connection for digital I/O buffers. Connect to +3.3V DC digital.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
51, 52, 54-59, 62, 63	DOUT[19:10]	Synchronous with PCLK	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DOUT19 is the MSB and DOUT10 is the LSB.	
				HD 20-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = HIGH	Luma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW
				SD 20-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = HIGH	Luma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
65	YANC	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of ancillary data in the video stream. HD Mode (SD/$\overline{HD}$ = LOW) The YANC signal will be HIGH when the device has detected VANC or HANC data in the luma video stream and LOW otherwise. SD Mode (SD/$\overline{HD}$ = LOW) For 20-bit demultiplexed data (20bit/$\overline{10bit}$ = HIGH), the YANC signal will be HIGH when VANC or HANC data is detected in the luma video stream and LOW otherwise. For 10-bit multiplexed data (20bit/$\overline{10bit}$ = LOW), the YANC signal will be HIGH when VANC or HANC data is detected anywhere in the data stream and LOW otherwise.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
66	CANC	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of ancillary data in the video stream. HD Mode (SD/$\overline{HD}$ = LOW) The CANC signal will be HIGH when the device has detected VANC or HANC data in the chroma video stream and LOW otherwise. SD Mode (SD/$\overline{HD}$ = LOW) For 20-bit demultiplexed data (20bit/$\overline{10bit}$ = HIGH), the CANC signal will be HIGH when VANC or HANC data is detected in the chroma video stream and LOW otherwise. For 10-bit multiplexed data (20bit/$\overline{10bit}$ = LOW), the CANC signal will be HIGH when VANC or HANC data is detected anywhere in the data stream and LOW otherwise.
67	FW_EN/$\overline{DIS}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the noise immune flywheel of the device. When set HIGH, the internal flywheel is enabled. This flywheel is used in the extraction and generation of TRS timing signals, in automatic video standards detection, and in manual switch line lock handling. When set LOW, the internal flywheel is disabled and TRS correction and insertion is unavailable.
69	PCLK	–	Output	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS/LVTTL compatible. HD 20-bit mode: PCLK = 74.25MHz or 74.25/1.001MHz HD 10-bit mode: PCLK = 148.5MHz or 148.5/1.001MHz SD 20-bit mode: PCLK = 13.5MHz SD 10-bit mode: PCLK = 27MHz

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
70	$\overline{\text{RC\_BYP}}$	Non Synchronous	Input /Output	GS1560A CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be an input set by the application layer in slave mode, and will be an output set by the device in master mode. Master Mode (MASTER/$\overline{\text{SLAVE}}$ = HIGH) The $\overline{\text{RC\_BYP}}$ signal will be HIGH only when the device has successfully locked to a SMPTE compliant input data stream. In this case, the serial digital loop-through output will be a reclocked version of the input. The $\overline{\text{RC\_BYP}}$ signal will be LOW whenever the input does not conform to a SMPTE compliant data stream. In this case, the serial digital loop-through output will be a buffered version of the input. Slave Mode (MASTER/$\overline{\text{SLAVE}}$ = LOW) When set HIGH, the serial digital output will be a reclocked version of the input signal regardless of whether the device is in SMPTE, DVB-ASI or Data-Through mode. When set LOW, the serial digital output will be a buffered version of the input signal in all modes.
	RSV	–	–	GS1561 Connect to CORE_VDD through 2.2kΩ.
71	MASTER/$\overline{\text{SLAVE}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to determine the input / output selection for the DVB_ASI, SD/$\overline{\text{HD}}$, $\overline{\text{RC\_BYP}}$ and $\overline{\text{SMPTE\_BYPASS}}$ pins. When set HIGH, the GS1560A is set to operate in master mode where SD/$\overline{\text{HD}}$, $\overline{\text{RC\_BYP}}$ (GS1560A only) and $\overline{\text{SMPTE\_BYPASS}}$ become status signal output pins set by the device. In this mode, the GS1560A will automatically detect, reclock, deserialize and process SD SMPTE and HD SMPTE input data. When set LOW, the GS1560A is set to operate in slave mode where DVB_ASI, SD/$\overline{\text{HD}}$, $\overline{\text{RC\_BYP}}$ (GS1560A only) and $\overline{\text{SMPTE\_BYPASS}}$ become control signal input pins. In this mode, the application layer must set these external device pins for the correct reception of either SMPTE or DVB-ASI data. Slave mode also supports the reclocking and deserializing of data not conforming to SMPTE or DVB-ASI streams.
72	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. The LOCKED signal will be HIGH whenever the device has correctly received and locked to SMPTE compliant data in SMPTE mode or DVB-ASI compliant data in DVB-ASI mode. It will be LOW otherwise.
73, 74	VCO, $\overline{\text{VCO}}$	Analog	Input	Differential inputs for the external VCO reference signal. For single ended devices such as the GO1555/GO1525*, $\overline{\text{VCO}}$ should be AC coupled to VCO_GND. VCO is nominally 1.485GHz. *For new designs use GO1555

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
75	VCO_GND	–	Output Power	Ground reference for the external voltage controlled oscillator. Connect to pins 2, 4, 6, and 8 of the GO1555/GO1525*. This pin is an output. Should be isolated from all other grounds. *For new designs use GO1555
76	VCO_VCC	–	Output Power	Power supply for the external voltage controlled oscillator. Connect to pin 7 of the GO1555/GO1525*. This pin is an output. Should be isolated from all other power supplies. *For new designs use GO1555
77	LF	Analog	Output	Control voltage to external voltage controlled oscillator. Nominally +1.25V DC.
78	CP_CAP	Analog	Input	PLL lock time constant capacitor connection. Normally connected to VCO_GND through 2.2nF.
79	LB_CONT	Analog	Input	Control voltage to set the loop bandwidth of the integrated reclocker. Normally connected to VCO_GND through 40kΩ.
80	CP_GND	–	Power	Ground connection for the charge pump. Connect to analog GND.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +4.6V
Input Voltage Range (any input)	-2.0V to + 5.25V
Ambient Operating Temperature	$-20°C \leq T_A \leq 85°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
Lead Temperature (soldering, 10 sec)	230°C
ESD Protection On All Pins (see Note 2)	1kV

NOTES:

1. See reflow solder profile (on page 21)
2. HBM, per JESDA-114B

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
System								
Operation Temperature Range	T_A	–	0	–	70	°C	–	1
Digital Core Supply Voltage	CORE_VDD	–	1.65	1.8	1.95	V	1	1
Digital I/O Supply Voltage	IO_VDD	–	3.0	3.3	3.6	V	1	1
Charge Pump Supply Voltage	CP_VDD	–	3.0	3.3	3.6	V	1	1
Phase Detector Supply Voltage	PD_VDD	–	1.65	1.8	1.95	V	1	1
Input Buffer Supply Voltage	BUFF_VDD	–	1.65	1.8	1.95	V	1	1
Cable Driver Supply Voltage	CD_VDD	–	1.71	1.8	1.89	V	1	1
External VCO Supply Voltage Output	VCO_VCC	–	2.25	2.50	2.75	V	1	–

Table 2-1: DC Electrical Characteristics (Continued)

T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
+1.8V Supply Current GS1560A	I_{1V8}	–	–	–	245	mA	1	4
+1.8V Supply Current GS1561	I_{1V8}	–	–	–	200	mA	1	–
+3.3V Supply Current	I_{3V3}	–	–	–	55	mA	1	5
Total Device Power GS1560A	P_D	–	–	–	625	mW	5	4, 5
Total Device Power GS1561	P_D	–	–	–	545	mW	5	5
Digital I/O								
Input Logic LOW	V_{IL}	–	–	–	0.8	V	1	–
Input Logic HIGH	V_{IH}	–	2.1	–	–	V	1	–
Output Logic LOW	V_{OL}	8mA	–	0.2	0.4	V	1	–
Output Logic HIGH	V_{OH}	8mA	IO_VDD - 0.4	–	–	V	1	–
Input								
Input Bias Voltage	V_B	–	–	1.45	–	V	6	2
RSET Voltage (GS1560A only)	V_{RSET}	RSET=281Ω	0.54	0.6	0.66	V	1	3
Output (GS1560A only)								
Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET=281Ω, SD and HD	0.8	1.0	1.2	V	1	–

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. All DC and AC electrical parameters within specification.
2. Input common mode is set by internal biasing resistors.
3. Set by the value of the RSET resistor. (GS1560A only)
4. Loop-through enabled. (GS1560A only)
5. Measured in 20-bit mode.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
System								
Serial Digital Input Jitter Tolerance	IJT	Nominal loop bandwidth	0.6	–	–	UI	1	1
Master Mode Asynchronous Lock Time		No data to HD	–	–	468	us	6,7	2
		HD to SD	–	–	260	us	6,7	2
		No data to SD	–	–	340	us	6,7	2
		SD to HD	–	–	256	us	6,7	2
Slave Mode Asynchronous Lock Time		No data to HD	–	–	240	us	6,7	2
		No data to SD	–	–	197	us	6,7	2
		No data to DVB-ASI	–	–	68	us	6,7	2
Device Latency		10-bit SD	–	21	–	PCLK	6	–
		20-bit HD	–	21	–	PCLK	6	–
		DVB-ASI	–	11	–	PCLK	6	–
Reset Pulse Width	t_{reset}	–	1	–	–	ms	7	6
Serial Digital Differential Input								
Serial Input Data Rate	DR_{DDI}	–	–	1.485, 1.485/1.001, 270	–	Gb/s Gb/s Mb/s	1	–
Serial Digital Input Signal Swing	ΔV_{DDI}	Differential with internal 100Ω input termination	200	600	1000	mV_{p-p}	1	–
Serial Digital Output (GS1560A only)								
Serial Output Data Rate	DR_{SDO}	–	–	1.485, 1.485/1.001, 270	–	Gb/s Gb/s Mb/s	1	–
Serial Output Swing	ΔV_{SDO}	RSET = 281Ω Load = 75Ω V_{DD} = 1.8V	720	800	880	mVp-p	1	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	ORL compensation using recommended circuit — HD signal	–	200	260	ps	1	–
		ORL compensation using recommended circuit — SD signal	400	550	1500	ps	1	–

Table 2-2: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	ORL compensation using recommended circuit — HD signal	–	235	260	ps	1	–
		ORL compensation using recommended circuit — SD signal	400	550	1500	ps	1	–
Serial Output Intrinsic Jitter	t_{IJ}	Pseudorandom and pathological HD signal	–	90	125	ps	1	3
		Pseudorandom and pathological SD signal	–	270	350	ps	1	3
Serial Output Duty Cycle Distortion	DCD_{SDO}	HD (1.485Gb/s)	–	10	–	ps	6,7	4
		SD (270Mb/s)	–	20	–	ps	6,7	4
Parallel Output								
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	1	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	50	60	%	1	–
Output Data Hold Time	t_{OH}	20-bit HD	1.0	–	–	ns	1	5
		10-bit SD, 50% PCLK Duty Cycle	19.5	–	–	ns	1	5
Output Data Delay Time	t_{OD}	20-bit HD	–	–	4.5	ns	1	5
		10-bit SD, 50% PCLK Duty Cycle	–	–	22.8	ns	1	5
Output Data Rise/Fall Time	tr/tf	–	–	–	1.5	ns	6,7	5

Table 2-2: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
GSPI								
GSPI Input Clock Frequency	f_{SCLK}	–	–	–	6.6	MHz	1	–
GSPI Input Clock Duty Cycle	DC_{SCLK}	–	40	50	60	%	6,7	–
GSPI Input Data Setup Time	–	–	0	–	–	ns	6,7	–
GSPI Input Data Hold Time	–	–	–	–	1.43	ns	6,7	–
GSPI Output Data Hold Time	–	–	2.10	–	–	ns	6,7	–
GSPI Output Data Delay Time	–	–	–	–	7.27	ns	6,7	–

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. 6MHz sinewave modulation.
2. HD = 1080i, SD = 525i
3. Serial Digital Output Reclocked ($\overline{RC\_BYP}$ = HIGH).
4. Serial Duty Cycle Distortion is defined here to be the difference between the width of a '1' bit, and the width of a '0' bit. (GS1560A only)
5. With 15pF load. (GS1560A only)
6. See Device Reset on page 70, Figure 4-16. (GS1560A only)

3. Input/Output Circuits

All resistors in ohms, all capacitors in farads, unless otherwise shown.

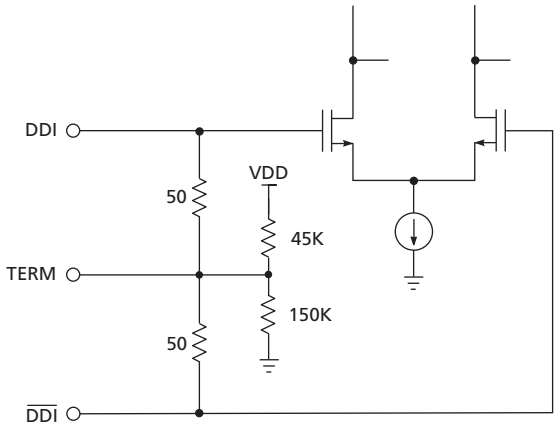


Figure 3-1: Serial Digital Input

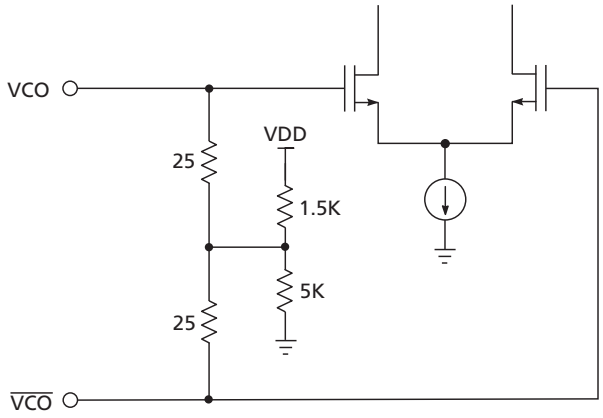


Figure 3-2: VCO Input

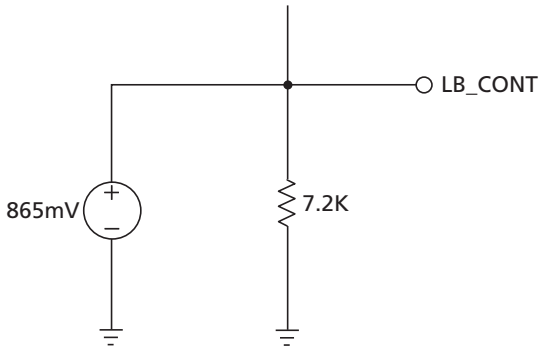


Figure 3-3: PLL Loop Bandwidth Control

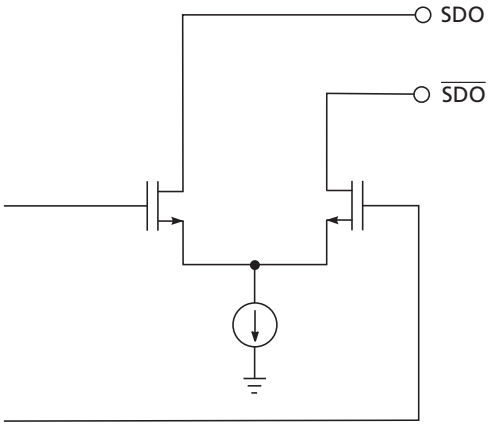


Figure 3-4: Serial Digital Output (GS1560A only)

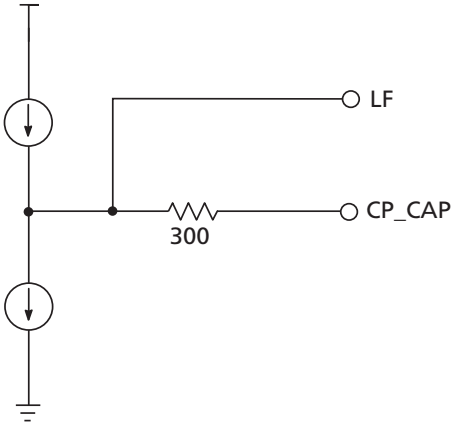


Figure 3-5: VCO Control Output & PLL Lock Time Capacitor