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GS1572 Multi-Rate Serializer with Cable Driver and ClockCleaner™

Key Features

- HD-SDI, SD-SDI, DVB-ASI transmitter
- Integrated SMPTE 292M and 259M-C compliant cable driver
- Integrated ClockCleaner™
- User selectable video processing features, including:
  - Generic ancillary data insertion
  - Support for HVF or EIA/CEA-861 timing input
  - Automatic standard detection and indication
  - Enhanced SMPTE 352M payload identifier generation and insertion
  - TRS, CRC, ANC data checksum, and line number calculation and insertion
  - EDH packet generation and insertion
  - Illegal code remapping
  - SMPTE 292M and SMPTE 259M-C compliant scrambling and NRZ → NRZI encoding
  - Blanking of input HANC and VANC space
- JTAG test interface
- 1.8V core and 3.3V charge pump power supply
- 1.8V and 3.3V digital I/O support
- Low power standby mode
- Operating temperature range: -20°C to +85°C
- Pb-free, RoHS compliant, 11mm x 11mm 100-ball BGA package

Applications

- SMPTE 292M and SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS1572 is the next generation multi-standard serializer with an integrated cable driver. The device provides robust parallel to serial conversion, generating a SMPTE 292M/259M-C compliant serial digital output signal. The integrated cable driver features an output disable (high-impedance) mode and an adjustable signal swing. Data input is accepted in 20-bit parallel format or 10-bit parallel format. An associated parallel clock input must be provided at the appropriate operating frequency - 74.25/74.1758/13.5MHz (20-bit mode) or 148.5/148.352/27MHz (10-bit mode).

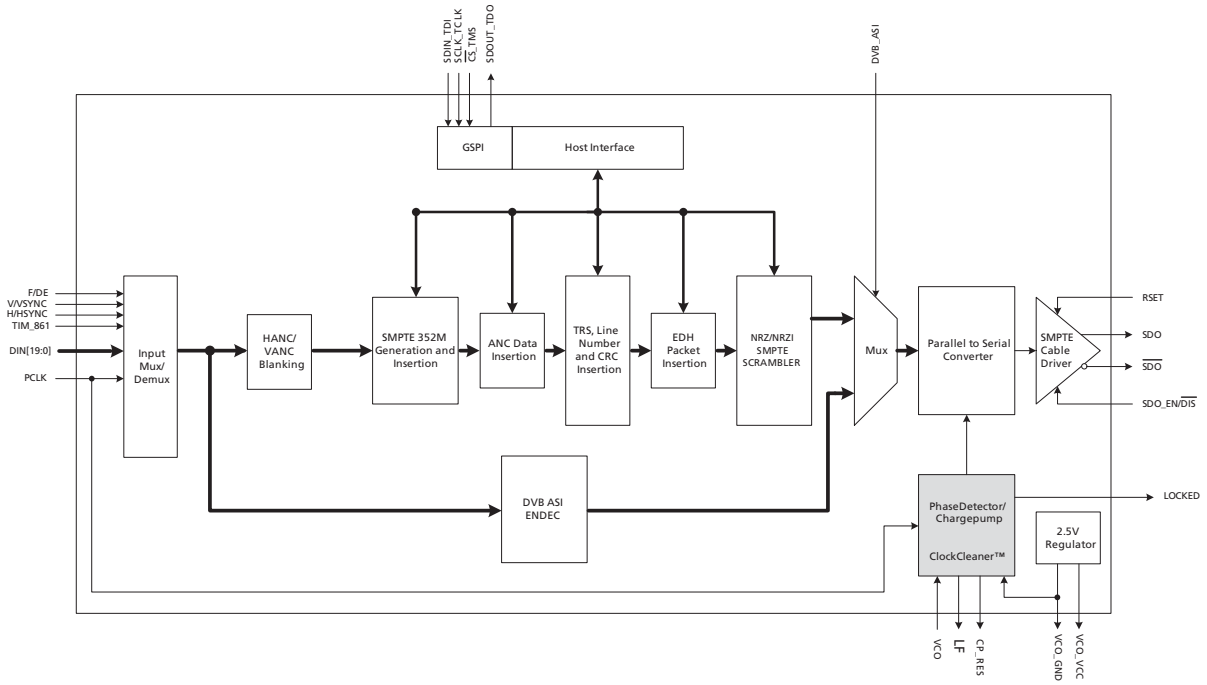
The GS1572 features an internal PLL which, if desired, can be configured for a loop bandwidth below 100kHz. When used in conjunction with the GO1555 Voltage Controlled Oscillator, the GS1572 can tolerate well in excess of 300ps jitter on the input PCLK and still provide output jitter within SMPTE specifications.

In addition to serializing the input, the GS1572 performs NRZ-to-NRZI encoding and scrambling as per SMPTE 292M/259M-C when operating in SMPTE mode. When operating in DVB-ASI mode, the device will insert K28.5 sync characters and 8b/10b encode the data prior to serialization. The device also provides a range of other data processing functions. All processing features are optional and may be enabled/disabled via external control pin(s) and/or host interface programming.

Typical power consumption, including the GO1555 VCO, is 440mW. The standby feature allows the power to be reduced to 125mW. Power may be reduced to less than 10mW by also removing the power to the cable driver and eliminating transitions at the parallel data and clock inputs.

The GS1572 is Pb-free and RoHS compliant.

Functional Block Diagram



GS1572 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
4	151052	52184	March 2009	Updated document format. Changed Figure 4-14: GSPI Write Mode Timing. Changed Parallel Input Data Hold Time from 2ns to 0.8ns in Table 2-4: AC Electrical Characteristics.
3	148226	–	November 2007	Converted from Preliminary Data Sheet to Data Sheet. Updates to; 2.1 Absolute Maximum Ratings, 4.12 GSPI Host Interface, Table 4-4: Host Interface Description for Raster Structure Registers, 2.3 DC Electrical Characteristics, 4.8.4.4 Ancillary Data Checksum Generation and Insertion, Table 2-4: AC Electrical Characteristics and 4.8.4.1 SMPTE 352M Payload Identifier Packet Insertion.
2	146447	–	July 2007	Updated Typical Application Circuit.
1	146292	–	July 2007	Format change.
0	145654	–	July 2007	Converted from Advance Information Note to Preliminary Data Sheet. Changes were made in the following areas: Pin Descriptions on page 8, Absolute Maximum Ratings on page 16, Recommended Operating Conditions on page 17, DC Electrical Characteristics on page 17, AC Electrical Characteristics on page 18, SMPTE Mode on page 26, HVF Timing on page 26, Standby Mode on page 33, on page 34, VANC Insertion on page 36, SMPTE 352M Payload Identifier Packet Insertion on page 40, EDH Generation and Insertion on page 42, Loop Filter on page 45, Lock Detect Output on page 46, Command Word Description on page 48, Device Reset on page 58, Typical Application Circuit on page 59, Package Dimensions on page 61, Solder Reflow Profiles on page 62, Packaging Data on page 63, Ordering Information on page 63.
A	144897	–	April 2007	New Document.

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1. Pin Out

1.1 Pin Assignment

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A	DIN17	DIN18	F/DE	H/HSYNC	CORE _VDD	PD_VDD	LF	VCO_ VCC	VCO	CP_VDD
B	DIN15	DIN16	DIN19	PCLK	CORE _GND	PD_VDD	CP_RES	VCO_ GND	VCO_ GND	CP_GND
C	DIN13	DIN14	DIN12	V/VSYNC	CORE _GND	PD_GND	PD_GND	PD_GND	CD_GND	SDO
D	DIN11	DIN10	STANDBY	SDO_EN/ $\overline{\text{DIS}}$	CORE _GND	NC	NC	NC	CD_GND	$\overline{\text{SDO}}$
E	CORE _VDD	CORE _GND	SD/$\overline{\text{HD}}$	NC	CORE _GND	CORE _GND	CORE _GND	NC	CD_GND	CD_VDD
F	DIN9	DIN8	DETECT _TRS	CORE _GND	CORE _GND	CORE _GND	CORE _GND	NC	CD_GND	RSET
G	IO_VDD	IO_GND	TIM 861	20bit/ $\overline{\text{10bit}}$	DVB_ASI	$\overline{\text{SMPTE\_}}$ $\overline{\text{BYPASS}}$	IOPROC _EN/$\overline{\text{DIS}}$	$\overline{\text{RESET}}$	CORE _GND	CORE _VDD
H	DIN7	DIN6	$\overline{\text{ANC\_}}$ $\overline{\text{BLANK}}$	LOCKED	RSV	RSV	RSV	JTAG/ $\overline{\text{HOST}}$	IO_GND	IO_VDD
J	DIN5	DIN4	DIN1	RSV	RSV	RSV	RSV	CORE _GND	SDOUT _TDO	SCLK _TCLK
K	DIN3	DIN2	DIN0	RSV	RSV	RSV	RSV	CORE _VDD	$\overline{\text{CS\_}}$ TMS	SDIN _TDI

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description	
A1, A2, B1, B2, B3, C1, C2, C3, D1, D2	DIN[19:10]	Synchronous with PCLK	Input	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DIN19 is the MSB and DIN10 is the LSB.	
				HD 20-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = HIGH	Luma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW
				SD 20-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = HIGH	Luma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data input in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data input in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A3	F/DE	Synchronous with PCLK	Input	PARALLEL DATA TIMING Signal levels are LVCMOS/LVTTL compatible. TIM_861 = LOW: Used to indicate the ODD / EVEN field of the video signal when DETECT_TRS is set LOW. The device will set the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH (IOPROC_EN/$\overline{DIS}$ must also be HIGH). The F signal should be set HIGH for the entire period of field 2 and should be set LOW for all lines in field 1 and for all lines in progressive scan systems. The F signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The DE signal is used to indicate the active video period. DE is HIGH for active data and LOW for blanking. See Section 4.3.1 and Section 4.3.2 for timing details. The DE signal is ignored when DETECT_TRS = HIGH.
A4	H/HSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING Signal levels are LVCMOS/LVTTL compatible. TIM_861 = LOW: The H signal is used to indicate the portion of the video line containing active video data, when DETECT_TRS is set LOW. Active Line Blanking The H signal should be set HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words, and LOW otherwise. This is the default setting. TRS Based Blanking (H_CONFIG = 1_h) The H signal should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise. The H signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The HSYNC signal indicates horizontal timing. See Section 4.3.1 for timing details. The HSYNC signal is ignored when DETECT_TRS = HIGH.
A5, E1, G10, K8	CORE_VDD	Non Synchronous	Input Power	Power supply connection for the digital core logic. Connect to +1.8V DC digital.
A6, B6	PD_VDD	Analog	Input Power	Power supply connection for the phase detector. Connect to +1.8V DC analog.
A7	LF	Analog	Input	PLL loop filter connection.
A8	VCO_VCC	Analog	Output Power	Power supply for the external voltage controlled oscillator. 2.5V DC supplied by the device to the external VCO.
A9	VCO	Analog	Input	Input from external VCO.
A10	CP_VDD	Analog	Input Power	Power supply connection for the charge pump and on chip VCO regulator. Connect to +3.3V DC analog.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
B4	PCLK	–	Input	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS/LVTTL compatible.	
				HD 20-bit mode	PCLK = 74.25MHz or 74.25/1.001MHz
				HD 10-bit mode	PCLK = 148.5MHz or 148.5/1.001MHz
				SD 20-bit mode	PCLK = 13.5MHz
				SD 10-bit mode	PCLK = 27MHz
B5, C5, D5, E2, E5, E6, E7, F4, F5, F6, F7, G9, J8	CORE_GND	Non Synchronous	Input Power	Ground connection for the digital core logic. Connect to digital GND.	
C6, C7, C8	PD_GND	Analog	Input Power	Ground connection for the phase detector. Connect to analog GND.	
B7	CP_RES	–	Input	Charge pump current setting resistor.	
B8, B9	VCO_GND	Analog	Output Power	Ground pins for the VCO.	
B10	CP_GND	Analog	Input Power	Ground pin for the charge pump and PLL.	
C4	V/VSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING Signal levels are LVCMOS/LVTTL compatible. TIM_861 = LOW: The V signal is used to indicate the portion of the video field/frame that is used for vertical blanking, when DETECT_TRS is set LOW. The V signal should be set HIGH for the entire vertical blanking period and should be set LOW for all lines outside of the vertical blanking interval. The V signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The VSYNC signal indicates vertical timing. See Section 4.3.1 for timing details. The VSYNC signal is ignored when DETECT_TRS = HIGH.	
C9, D9, E9, F9	CD_GND	Analog	Input Power	Ground connection for the serial digital cable driver. Connect to analog GND.	
C10, D10	SDO, $\overline{\text{SDO}}$	Analog	Output	Serial digital output signal operating at 1.485Gb/s, 1.485/1.001Gb/s, or 270Mb/s. The slew rate of these outputs is automatically controlled to meet SMPTE 292M and 259M requirements according to the setting of the SD/$\overline{\text{HD}}$ pin. Serial digital output signal from the internal cable driver. NOTE: The SDO/$\overline{\text{SDO}}$ output signals will be set to high impedance when $\overline{\text{RESET}}$ = LOW.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
D3	STANDBY	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Power down input. When set HIGH, the device will be in standby mode.
D4	SDO_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the serial digital output stage. When set LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When set HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled. The SDO and $\overline{\text{SDO}}$ outputs will also be high impedance when the $\overline{\text{RESET}}$ pin is LOW.
D6, D7, D8, E4, E8, F8	NC	–	–	No connect. Not connected internally.
E3	SD/$\overline{\text{HD}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set LOW, the device will be configured to transmit signals of 1.485Gb/s - 1.485/1.001Gb/s rates only. When set HIGH, the device will be configured to transmit signals of a 270Mb/s rate only.
E10	CD_VDD	Analog	Input Power	Power supply connection for the serial digital cable driver. Connect to +3.3V DC analog.
F1, F2, H1, H2, J1, J2, J3, K1, K2, K3	DIN[9:0]	Synchronous with PCLK	Input	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DIN9 is the MSB and DIN0 is the LSB.
				HD 20-bit mode SD/$\overline{\text{HD}}$ = LOW 20bit/$\overline{\text{10bit}}$ = HIGH — Chroma data input in SMPTE mode $\overline{\text{SMPTE\_BYPASS}}$ =HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{\text{SMPTE\_BYPASS}}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{\text{HD}}$ = LOW 20bit/$\overline{\text{10bit}}$ = LOW — High impedance in all modes.
				SD 20-bit mode SD/$\overline{\text{HD}}$ = HIGH 20bit/$\overline{\text{10bit}}$ = HIGH — Chroma data input in SMPTE mode $\overline{\text{SMPTE\_BYPASS}}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{\text{SMPTE\_BYPASS}}$ = LOW DVB_ASI = LOW Forced low in DVB-ASI mode $\overline{\text{SMPTE\_BYPASS}}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{\text{HD}}$ = HIGH 20bit/$\overline{\text{10bit}}$ = LOW — High impedance in all modes.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
F3	DETECT_TRS	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select external HVF timing mode or TRS Extraction timing mode. When DETECT_TRS = LOW, the device will use timing from the externally supplied H:V:F or CEA-861 timing signals, dependent on the state of the TIM_861 pin. When DETECT_TRS = HIGH, the device will extract timing from TRS signals embedded in the supplied video stream.
F10	RSET	Analog	Input	An external 1% resistor connected to this input is used to set the SDO/$\overline{\text{SDO}}$ output amplitude.
G1, H10	IO_VDD	Non Synchronous	Input Power	Power supply connection for digital I/O buffers. Connect to +3.3V or +1.8V DC digital.
G2, H9	IO_GND	Non Synchronous	Input Power	Ground connection for digital I/O buffers. Connect to digital GND.
G3	TIM_861	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select external CEA-861 timing mode. When DETECT_TRS = LOW and TIM_861 = LOW, the device will use externally supplied H:V:F timing signals. When DETECT_TRS = LOW and TIM_861 = HIGH, the device will use externally supplied HSYNC, VSYNC, DE timing signals. When DETECT_TRS = HIGH, the device will extract timing from TRS signals embedded in the supplied video stream.
G4	20bit/$\overline{\text{10bit}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select the input data bus width.
G5	DVB_ASI	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set HIGH, the device is configured for the transmission of DVB-ASI data in SD mode (SD/$\overline{\text{HD}}$ = HIGH). When set LOW, the device will not support the encoding of DVB-ASI data. NOTE: When operating in DVB-ASI mode the SD/$\overline{\text{HD}}$ pin must be set HIGH and $\overline{\text{SMPTE\_BYPASS}}$ must be set LOW.
G6	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable all forms of encoding/decoding, scrambling and EDH insertion. When set LOW, the device will operate in data through mode (DVB_ASI = LOW), or in DVB-ASI mode (DVB_ASI = HIGH). No SMPTE scrambling will take place and none of the I/O processing features of the device will be available when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW. When set HIGH, the device will perform SMPTE scrambling and I/O processing.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G7	IOPROC_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • EDH Packet Generation and Insertion (SD-only) • SMPTE 352M Packet Generation and Insertion • ANC Data Checksum Calculation • ANC Data Insertion • Line-based CRC Generation and Insertion (HD-only) • Line Number Generation and Insertion (HD-only) • TRS Generation and Insertion • Illegal Code Remapping To enable a subset of these features, set IOPROC_EN/$\overline{\text{DIS}}$ = HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When set LOW, the I/O processing features of the device are disabled, and can not be enabled by changing the settings in the IOPROC_DISABLE register.
G8	$\overline{\text{RESET}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG test sequence. Normal Mode (JTAG/$\overline{\text{HOST}}$ = LOW) When set LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance including the serial digital outputs SDO and $\overline{\text{SDO}}$. When set HIGH, normal operation of the device resumes 10usec after the low to high transition of the $\overline{\text{RESET}}$ signal. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) When set LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes.
H3	$\overline{\text{ANC\_BLANK}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable ANC data blanking. When set LOW, the HANC and VANC data is mapped to the appropriate blanking levels.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H4	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. This signal is set HIGH by the device when the internal PLL has achieved lock to the supplied PCLK signal. This pin is set LOW by the device under all other conditions. IO_VDD = 3.3V Drive Strength = 8mA IO_VDD = 1.8V Drive Strength = 4mA
H5, H6, H7, J4, J5, J6, J7, K4, K5, K6, K7	RSV	Non Synchronous	Input	Reserved. Do not connect.
H8	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured as Gennum Serial Peripheral Interface (GSPI) pins for normal host interface operation.
J9	SDOUT_TDO	Synchronous with SCLK_TCK	Output	COMMUNICATION SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) This pin operates as the host interface serial output, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is used to shift test results and operates as the JTAG test data output, TDO. NOTE: If the host interface is not being used leave this pin unconnected. Drive Strength: IO_VDD = 3.3V = 12mA IO_VDD = 1.8V = 4mA
J10	SCLK_TCK	Non Synchronous	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Clock / Test Clock. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is the TEST MODE START pin, used to control the operation of the JTAG test clock, TCK. NOTE: If the host interface is not being used, tie this pin HIGH.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
K9	CS_TMS	Synchronous with SCLK_TCK	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip Select / Test Mode Start. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) $\overline{\text{CS}}$_TMS operates as the host interface chip select, $\overline{\text{CS}}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) $\overline{\text{CS}}$_TMS operates as the JTAG test mode start, TMS, used to control the operation of the JTAG test, and is active HIGH. NOTE: If the host interface is not being used, tie this pin HIGH.
K10	SDIN_TDI	Synchronous with SCLK_TCK	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data In / Test Data Input Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) This pin operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is used to shift and operates as the JTAG test data input, TDI. NOTE: If the host interface is not being used, tie this pin HIGH.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Core (CORE_VDD)	-0.3V to +2.1V
Supply Voltage, Analog 1.8V (PD_VDD)	-0.3V to +2.1V
Supply Voltage, I/O (IO_VDD)	-0.3V to +3.6V
Supply Voltage, Analog 3.3V (CP_VDD, CD_VDD)	-0.3V to +3.6V
Input Voltage Range (PCLK, DIN)	-0.5V to IO_VDD+0.25V
Input Voltage Range (VCO, CP_RES, LF, RSET)	-0.5V to +3.6V
Input Voltage Range (All other pins)	-0.5V to +5.25V
Ambient Operating Temperature	$-40°C \leq T_A \leq 95°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	4000V
ESD Sensitivity, MM (JESD22-A115)	200V

NOTES:

1. Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	25	85	°C	
Supply Voltage, Digital Core	CORE_VDD	–	1.71	1.8	1.89	V	
Supply Voltage, Phase Detector	PD_VDD	–	1.71	1.8	1.89	V	
Supply Voltage, Charge Pump	CP_VDD	–	3.13	3.3	3.47	V	
Supply Voltage, Cable Driver	CD_VDD	–	3.13	3.3	3.47	V	
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	
Supply Voltage, Digital I/O	IO_VDD	3.3V mode	3.13	3.3	3.47	V	

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
External VCO Power Supply Voltage (VCO_VDD)			2.375	2.5	2.625	V	1
+1.8V Supply Current	I_{1V8}	10/20bit HD	–	109	130	mA	2,4
		10/20bit SD	–	104	120	mA	2,4
		DVB_ASI	–	100	120	mA	2,4
+3.3V Supply Current	I_{3V3}	10/20bit HD	–	74	86	mA	3,4
		10/20bit SD	–	74	86	mA	3,4
		DVB_ASI	–	74	86	mA	3,4
Total Device Power	P_D	10/20bit HD	–	440	540	mW	4
		10/20bit SD	–	430	530	mW	4
		DVB_ASI	–	424	510	mW	4
		Reset	–	310	–	mW	–
		Standby	10	125	–	mW	5

Table 2-3: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	–	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	–	V	–
Output Logic LOW	V_{OL}	1.8V mode	–	–	0.3	V	–
		3.3V mode	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	1.8V mode	1.4	–	–	V	–
		3.3V mode	2.4	–	–	V	–
Output							
Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET=750Ω SD and HD mode	–	CD_VDD - ΔV_{SDD}	–	V	–

NOTES

1. VCO_VDD guaranteed only when GO1555 is connected.
2. Sum of all 1.8V supplies.
3. Sum of all 3.3V supplies.
4. IO_VDD = 3.3V. When IO_VDD = 1.8V, the current/power consumption is lower by up to 5mA/10mW.
5. See 4.6 Standby Mode for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency	–	–	–	–	27	PCLK	–
	–	DVB-ASI	–	–	15	PCLK	–
Reset Pulse Width	t_{reset}	–	10	–	–	ms	1
Parallel Input							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Input Data Setup Time	t_{su}	50% levels; 3.3V or 1.8V operation	2	–	–	ns	4
Input Data Hold Time	t_{ih}		0.8	–	–	ns	4
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	–	1.485	–	Gb/s	–
		–	–	1.485/1.001	–	Gb/s	–
		–	–	270	–	Mb/s	–
Serial Output Swing	V_{SDD}	RSET = 750Ω 75Ω load	750	800	850	mVp-p	–

Table 2-4: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Output Rise/Fall Time 20% ~ 80%	trf_{SDO}	HD mode	–	120	270	ps	–
	trf_{SDO}	SD mode	400	660	800	ps	–
Mismatch in rise/fall time	$\Delta t_r, \Delta t_f$	–	–	–	35	ps	–
Duty Cycle Distortion	–	–	–	1	5	%	5
Overshoot	–	SD/$\overline{HD}$=0	–	5	10	%	5
	–	SD/$\overline{HD}$=1	–	3	8	%	5
Output Return Loss	ORL	5 MHz - 1.485 GHz	–	18	–	dB	6
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and SMPTE Colour Bars HD signal	–	35	80	ps	2
	t_{OJ}	Pseudorandom and SMPTE Colour Bars SD signal	–	100	200	ps	3
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	10	MHz	–
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	–
GSPI Input Data Setup Time	–		1.5	–	–	ns	–
GSPI Input Data Hold Time	–		1.5	–	–	ns	–
GSPI Output Data Hold Time	–	15pF load	1.5	–	–	ns	–
CS low before SCLK rising edge	–	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	–
CS high after SCLK rising edge	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	–

NOTES:

1. See 'Device Reset' on page 58, Figure 4-17.
2. Alignment Jitter = measured from 100kHz to 148.5MHz
3. Alignment Jitter = measured from 1kHz to 27MHz
4. Input setup and hold time is dependent on the rise and fall time on the parallel input. Parallel clock and data with rise time or fall time greater than 500ps require larger setup and hold times.
5. Single Ended into 75Ω external load.
6. ORL depends on board design. The GS1572 achieves this specification on Gennum's evaluation boards.

3. Input/Output Circuits

All resistors in ohms, all capacitors in farads, unless otherwise shown.

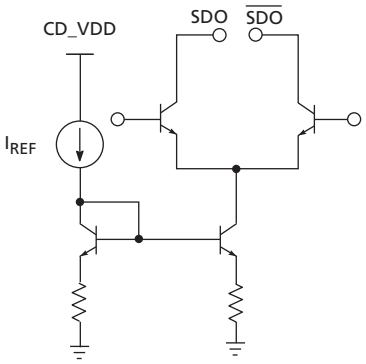

Figure 3-1: Differential Output Stage (SDO/$\overline{\text{SDO}}$)

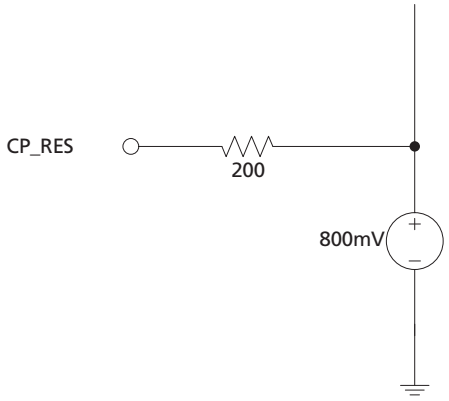

Figure 3-2: Charge Pump Current Setting Resistor (CP_RES)

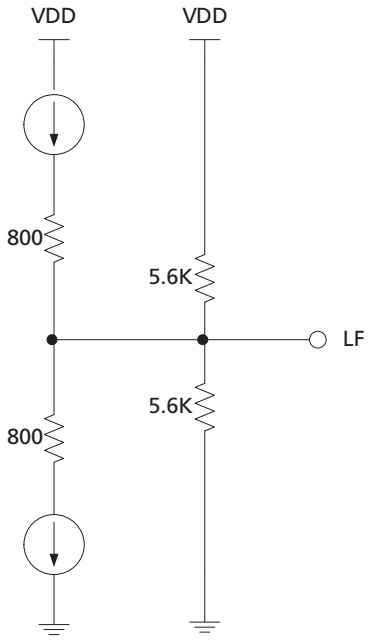

Figure 3-3: PLL Loop Filter

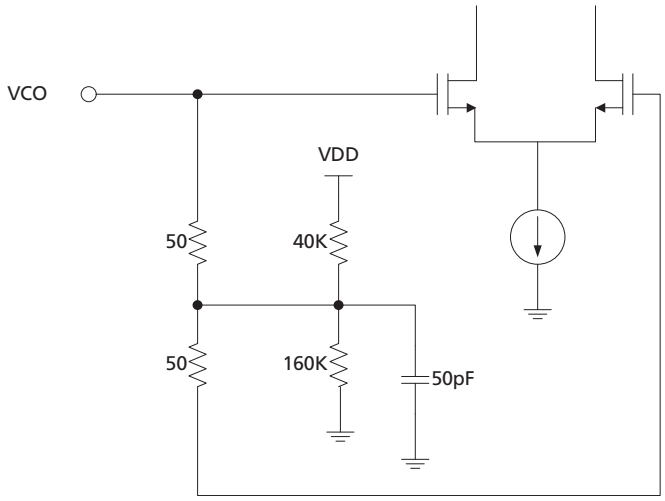

Figure 3-4: VCO Input

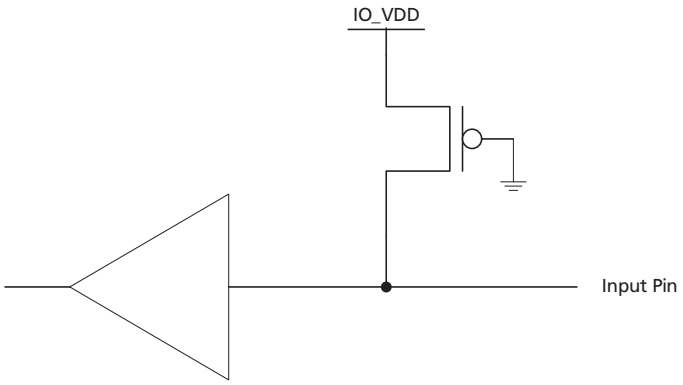

Figure 3-5: Digital Input Pin with Weak Pull Up(>33kΩ)
(PCLK, DIN[19:0])

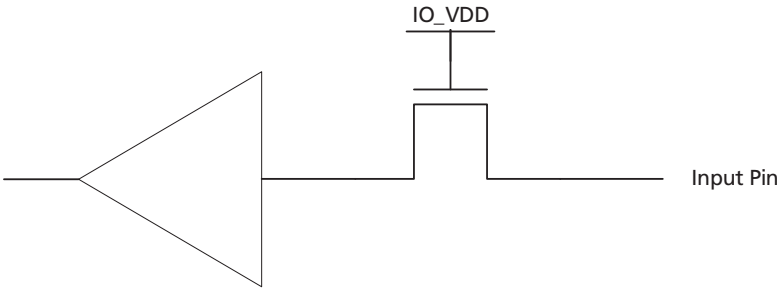

Figure 3-6: 5V Tolerant Input Pin (All Other Input Pins)

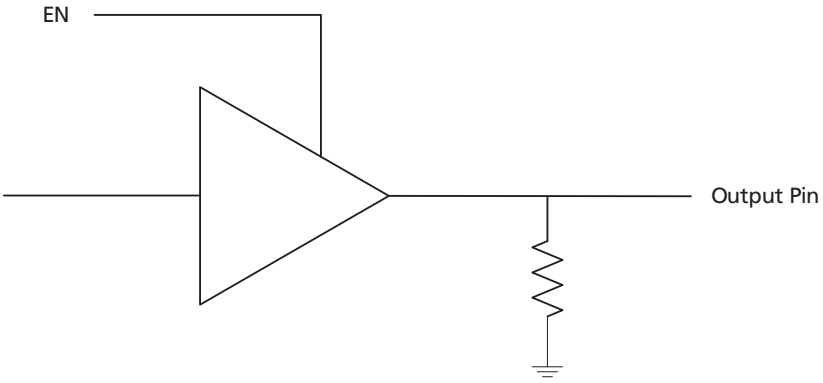

Figure 3-7: Digital Output Pin with High Impedance Mode
(LOCKED, SDOUT_TDO)

4. Detailed Description

4.1 Functional Overview

The GS1572 is a multi-rate Serializer with an Integrated Cable Driver. When used in conjunction with the external GO1555 Voltage Controlled Oscillator, a transmit solution at 1.485Gb/s, 1.485/1.001Gb/s or 270Mb/s is realized.

The device has three basic modes of operation that must be set through external device pins: SMPTE mode, DVB-ASI mode and Data-Through mode.

In SMPTE mode, the device will accept 10-bit multiplexed or 20-bit demultiplexed SMPTE compliant data at both HD and SD signal rates. By default, the device's additional processing features will be enabled in this mode.

In DVB-ASI mode, the GS1572 will accept an 8-bit parallel DVB-ASI compliant transport stream on DIN[17:10]. The serial output data stream will be 8b/10b encoded with stuffing characters added as per the standard.

Data-Through mode allows for the serializing of data not conforming to SMPTE or DVB-ASI streams. No additional processing will be done in this mode.

In Standby mode, the device power consumption will be reduced.

The Serial Digital Output features a high-impedance mode and adjustable signal swing. The output slew rate is automatically set by the SD/$\overline{\text{HD}}$ pin setting.

GS1572 provides several data processing functions including generic ANC insertion, SMPTE 352M and EDH data packet generation and insertion, automatic video standards detection, and TRS, CRC, ANC data checksum, and line number calculation and insertion. These features are all enabled/disabled collectively by using the external IO processing pin, but may be individually disabled via internal registers accessible through the GSPI Host Interface.

Finally, the GS1572 contains a JTAG interface for boundary scan test implementations.

4.2 Parallel Data Inputs

Data is clocked into the device on the rising edge of PCLK as shown in Figure 4-1.

The input data format is defined by the setting of the external SD/$\overline{\text{HD}}$, $\overline{\text{SMPTE\_BYPASS}}$, and DVB_ASI pins and may be presented in 10-bit or 20-bit format. The input data bus width is controlled by the 20bit/$\overline{\text{10bit}}$ input pin.

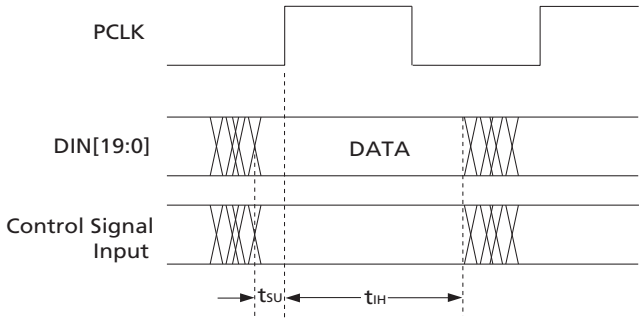

Figure 4-1: PCLK to Data Timing

4.2.1 Parallel Input in SMPTE Mode

When the device is operating in SMPTE mode, see SMPTE Mode on page 26, both SD and HD data may be presented to the input bus in either multiplexed or demultiplexed form depending on the setting of the 20bit/$\overline{10bit}$ input pin.

In 20-bit mode, (20bit/$\overline{10bit}$ = HIGH), the input data format should be word aligned, demultiplexed Luma and Chroma data. Luma words should be presented on DIN[19:10] while Chroma words should be presented on DIN[9:0].

In 10-bit mode, (20bit/$\overline{10bit}$ = LOW), the input data format should be word aligned, multiplexed Luma and Chroma data. The data should be presented on DIN[19:10]. DIN[9:0] will be high-impedance in this mode.

4.2.2 Parallel Input in DVB-ASI Mode

When operating in DVB-ASI mode, see DVB-ASI mode on page 32, the GS1572 must be set to 10-bit operation mode by setting the 20bit/$\overline{10bit}$ pin LOW.

The device will accept 8-bit data words on DIN[17:10] such that DIN17 = HIN is the most significant bit of the encoded transport stream data and DIN10 = AIN is the least significant bit.

In addition, DIN19 and DIN18 will be configured as the DVB-ASI control signals INSSYNCIN and KIN respectively. See DVB-ASI mode on page 32 for a description of these DVB-ASI specific input signals.

DIN[9:0] will have a logic level HIGH in DVB-ASI mode.

4.2.3 Parallel Input in Data-Through Mode

When operating in Data-Through mode, see Data-Through Mode on page 33, the GS1572 passes data from the parallel input bus to the serial output without performing any encoding or scrambling. The input data bus width is controlled by the setting of the 20bit/$\overline{10bit}$ pin.

4.2.4 Parallel Input Clock (PCLK)

The frequency of the PCLK input signal required by the GS1572 is determined by the input data format. Table 4-1 below lists the possible input signal formats and their corresponding parallel clock rates. Note that DVB-ASI input will only be in 10-bit format, when setting the 20bit/$\overline{10bit}$ pin LOW.

Table 4-1: Parallel Data Input Format

Input Data Format	DIN [19:10]	DIN [9:0]	PCLK	Control Signals			
				20bit/ $\overline{10bit}$	SD/ $\overline{HD}$	$\overline{SMPTE\_BYPASS}$	DVB_ASI
SMPTE MODE							
20-bit DEMULTIPLEXED SD	LUMA	CHROMA	13.5MHz	HIGH	HIGH	HIGH	LOW
10-bit MULTIPLEXED SD	LUMA/ CHROMA	HIGH IMPEDANCE	27MHz	LOW	HIGH	HIGH	LOW
20-bit DEMULTIPLEXED HD	LUMA	CHROMA	74.25 or 74.25/ 1.001MHz	HIGH	LOW	HIGH	LOW
10-bit MULTIPLEXED HD	LUMA/ CHROMA	HIGH IMPEDANCE	148.5 or 148.5/ 1.001MHz	LOW	LOW	HIGH	LOW
DVB-ASI MODE							
10-bit DVB-ASI	DVB-ASI DATA	HIGH IMPEDANCE	27MHz	LOW	HIGH	LOW	HIGH
				LOW	HIGH	LOW	HIGH
DATA-THROUGH MODE							
20-bit SD	DATA	DATA	13.5MHz	HIGH	HIGH	LOW	LOW
10-bit SD	DATA	HIGH IMPEDANCE	27MHz	LOW	HIGH	LOW	LOW
20-bit HD	DATA	DATA	74.25 or 74.25/ 1.001MHz	HIGH	LOW	LOW	LOW
10-bit HD	DATA	HIGH IMPEDANCE	148.5 or 148.5/ 1.001MHz	LOW	LOW	LOW	LOW