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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





HD/SD SDI Receiver, with Integrated Adaptive Cable Equalizer complete with SMPTE Video Processing

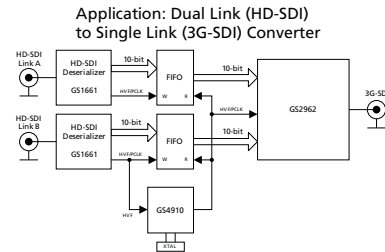
Key Features

- Operation at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE 292M, SMPTE 259M-C and DVB-ASI
- Integrated adaptive cable equalizer
- Typical equalized length of Belden 1694A cable:
 - ◆ 230m at 1.485Gb/s
 - ◆ 440m at 270Mb/s
- Integrated Reclocker with low phase noise, integrated VCO
- Serial digital reclocked, or non-reclocked output
- Ancillary data extraction
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 Timing Signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI Host Interface
- -20°C to +85°C operating temperature range
- Low power operation (typically 460mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and ROHS compliant

Errata

Refer to Errata document entitled **GS1660/GS1661 Errata** for this device (document number **53877**).

Applications



Description

The GS1661 is a multi-rate SDI integrated Receiver which includes complete SMPTE processing, as per SMPTE 292M and SMPTE 259M-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The GS1661 integrates Gennum's adaptive cable equalizer technology, achieving unprecedented cable lengths and jitter tolerance. It features DC restoration to compensate for the DC content of SMPTE pathological signals.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop-through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The serial digital output can be connected to an external cable driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode (the default operating mode), the GS1661 performs full SMPTE processing, and features a number of data integrity checks and measurement capabilities.

The device also supports ancillary data extraction, and can provide entire ancillary data packets through host-accessible registers. It also provides a variety of other

packet detection and error handling features. All of these processing features are optional, and may be individually enabled or disabled through register programming.

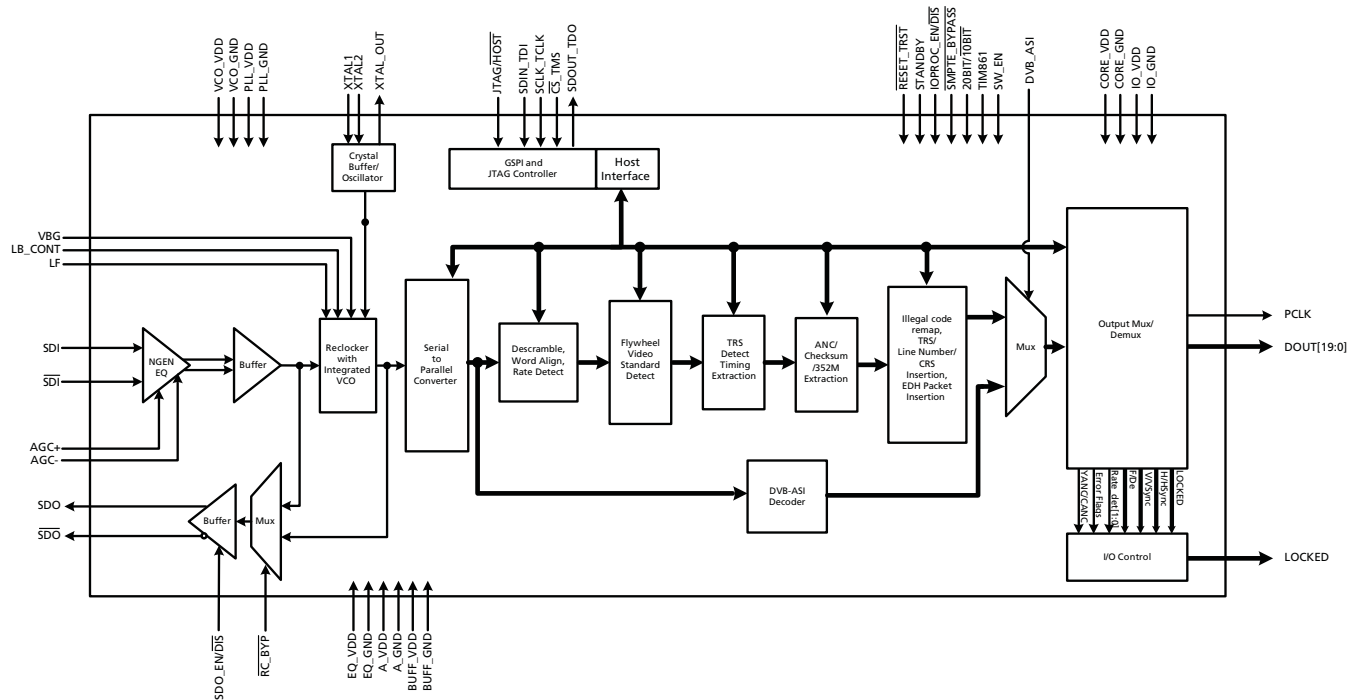
In DVB-ASI mode, sync word detection, alignment and 8b/10b decoding is applied to the received data stream.

In Data-Through mode all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

The device can also operate in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static.

Parallel data outputs are provided in 20-bit or 10-bit format for HD and SD video rates, with a variety of mapping options. As such, this parallel bus can interface directly with video processor ICs, and output data can be multiplexed onto 10 bits for a low pin count interface.

Functional Block Diagram



GS1661 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
3	158468	-	September 2012	Changes throughout the document.
2	153968	-	April 2010	Removed VCO Supply Voltage from Table 2-2: Recommended Operating Conditions , and revised VCO_VDD Pin Description in Table 1-1: Pin Descriptions .
1	153472	-	January 2010	Converted to Data Sheet.
0	152960	-	November 2009	New Document. Added reference to GS1660/GS1661 Errata (document number 53877).

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	A_VDD	PLL_VDD	RSV	VCO_GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	A_GND	PLL_VDD	PLL_VDD	STAT4	STAT5	RESET_TRST	DOUT12	DOUT14	DOUT13
D	SDI	A_GND	A_GND	PLL_GND	CORE_GND	CORE_VDD	SW_EN	JTAG/HOST	IO_GND	IO_VDD
E	EQ_VDD	EQ_GND	A_GND	PLL_GND	CORE_GND	CORE_VDD	SDOUT_TDO	SDIN_TDI	DOUT10	DOUT11
F	AGCP	RSV	A_GND	PLL_GND	CORE_GND	CORE_VDD	CS_TMS	SCLK_TCK	DOUT8	DOUT9
G	AGCN	A_GND	RC_BYP	CORE_GND	CORE_GND	CORE_VDD	SMPTE_BYPASS	DVB_ASI	IO_GND	IO_VDD
H	BUFF_VDD	BUFF_GND	CORE_GND	RSV	TIM_861	XTAL_OUT	20bit/10bit	IOPROC_EN/DIS	DOUT6	DOUT7
J	SDO	SDO_EN/DIS	RSV	RSV	RSV	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	SDO	STANDBY	RSV	RSV	RSV	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
A1	VBG		Analog Input	Band Gap voltage filter connection.
A2	LF		Analog Input	Loop Filter component connection.
A3	LB_CONT		Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD		Input Power	Power pin for the VCO. Connect to a 1.2V±5% analog supply, followed by a RC filter (see 5.3 Typical Application Circuit). A 105Ω 1% resistor must be used in the RC filter circuit. VCO_VDD is nominally 0.7V.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description																								
A5, A6, B5, B6, C5, C6	STAT[0:5]		Output	<p>MULTI-FUNCTIONAL OUTPUT PORT.</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Each of the STAT [0:5] pins can be configured individually to output one of the following signals:</p> <table border="1"> <thead> <tr> <th>Signal</th> <th>Default</th> </tr> </thead> <tbody> <tr> <td>H/HSYNC</td> <td>STAT0</td> </tr> <tr> <td>V/VSYNC</td> <td>STAT1</td> </tr> <tr> <td>F/DE</td> <td>STAT2</td> </tr> <tr> <td>LOCKED</td> <td>STAT3</td> </tr> <tr> <td>Y/1ANC</td> <td>STAT4</td> </tr> <tr> <td>C/2ANC</td> <td>–</td> </tr> <tr> <td>DATA ERROR</td> <td>STAT5</td> </tr> <tr> <td>VIDEO ERROR</td> <td>–</td> </tr> <tr> <td>EDH DETECTED</td> <td>–</td> </tr> <tr> <td>CARRIER DETECT</td> <td>–</td> </tr> <tr> <td>RATE_DET</td> <td>–</td> </tr> </tbody> </table>	Signal	Default	H/HSYNC	STAT0	V/VSYNC	STAT1	F/DE	STAT2	LOCKED	STAT3	Y/1ANC	STAT4	C/2ANC	–	DATA ERROR	STAT5	VIDEO ERROR	–	EDH DETECTED	–	CARRIER DETECT	–	RATE_DET	–
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Y/1ANC	STAT4																											
C/2ANC	–																											
DATA ERROR	STAT5																											
VIDEO ERROR	–																											
EDH DETECTED	–																											
CARRIER DETECT	–																											
RATE_DET	–																											
A7, D10, G10, K7	IO_VDD		Input Power	POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.																								
A8	PCLK		Output	<p>PARALLEL DATA BUS CLOCK</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <table border="1"> <tbody> <tr> <td>HD 10-bit mode</td> <td>PCLK @ 148.5 or 148.5/1.001MHz</td> </tr> <tr> <td>HD 20-bit mode</td> <td>PCLK @ 74.25 or 74.25/1.001MHz</td> </tr> <tr> <td>SD 10-bit mode</td> <td>PCLK @ 27MHz</td> </tr> <tr> <td>SD 20-bit mode</td> <td>PCLK @ 13.5MHz</td> </tr> </tbody> </table>	HD 10-bit mode	PCLK @ 148.5 or 148.5/1.001MHz	HD 20-bit mode	PCLK @ 74.25 or 74.25/1.001MHz	SD 10-bit mode	PCLK @ 27MHz	SD 20-bit mode	PCLK @ 13.5MHz																
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A9, A10, B8, B9, B10, C8, C9, C10, E9, E10	DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11		Output	<p>PARALLEL DATA BUS</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <table border="1"> <tbody> <tr> <td>20-bit mode 20bit/10bit = HIGH</td> <td> <p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}}$ = HIGH and DVB_ASI = LOW): Luma data output for SD and HD data rates</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = HIGH): Not defined</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output</p> </td> </tr> <tr> <td>10-bit mode 20bit/10bit = LOW</td> <td> <p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}}$ = HIGH and DVB_ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = HIGH): 8b/10b decoded DVB-ASI data</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output</p> </td> </tr> </tbody> </table>	20-bit mode 20bit/10bit = HIGH	<p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}}$ = HIGH and DVB_ASI = LOW): Luma data output for SD and HD data rates</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = HIGH): Not defined</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output</p>	10-bit mode 20bit/10bit = LOW	<p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}}$ = HIGH and DVB_ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = HIGH): 8b/10b decoded DVB-ASI data</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output</p>																				
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Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
B1	A_VDD		Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.
B2, C3, C4	PLL_VDD		Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.
B3, F2, H4, J3, J4, J5, K3, K4, K5	RSV			These pins must be left unconnected.
B4	VCO_GND		Input Power	GND pin for the VCO. Connect to analog GND.
B7, D9, G9, J7	IO_GND		Input Power	GND connection for digital I/O. Connect to digital GND.
C1, D1	SDI, $\overline{\text{SDI}}$		Analog Input	Serial Digital Differential Input.
C2, D2, D3, E3, F3, G2	A_GND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
C7	$\overline{\text{RESET_TRST}}$		Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to reset the internal operating conditions to default settings and to reset the JTAG sequence.</p> <p>Normal mode ($\text{JTAG}/\overline{\text{HOST}} = \text{LOW}$):</p> <p>When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance.</p> <p>When HIGH, normal operation of the device resumes.</p> <p>JTAG test mode ($\text{JTAG}/\overline{\text{HOST}} = \text{HIGH}$):</p> <p>When LOW, all functional blocks are set to default and the JTAG test sequence is reset.</p> <p>When HIGH, normal operation of the JTAG test sequence resumes after $\overline{\text{RESET_TRST}}$ is de-asserted.</p>
D4, E4, F4	PLL_GND		Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G4, G5, H3	CORE_GND		Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD		Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	SW_EN		Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to enable switch-line locking, as described in Section 4.9.1.</p>
D8	$\text{JTAG}/\overline{\text{HOST}}$		Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to select JTAG test mode or host interface mode.</p> <p>When $\text{JTAG}/\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test.</p> <p>When $\text{JTAG}/\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes.</p>
E1	EQ_VDD		Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	EQ_GND		Input Power	GND pin for SDI buffer. Connect to analog GND.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
E7	SDOUT_TDO		Output	<p>COMMUNICATION SIGNAL OUTPUT</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>GSPI serial data output/test data out.</p> <p>In JTAG mode ($JTAG/\overline{HOST} = \text{HIGH}$), this pin is used to shift test results from the device.</p> <p>In host interface mode, this pin is used to read status and configuration data from the device.</p> <p>Note: GSPI is slightly different than the SPI. For more details on GSPI, please refer to 4.18 GSPI - HOST Interface.</p>
E8	SDIN_TDI		Input	<p>COMMUNICATION SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>GSPI serial data in/test data in.</p> <p>In JTAG mode ($JTAG/\overline{HOST} = \text{HIGH}$), this pin is used to shift test data into the device.</p> <p>In host interface mode, this pin is used to write address and configuration data words into the device.</p>
F1, G1	AGCP, AGCN			Automatic Gain Control for the equalizer. Attach the AGC capacitor between these pins.
F7	$\overline{CS_TMS}$		Input	<p>COMMUNICATION SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Chip select / test mode start.</p> <p>In JTAG mode ($JTAG/\overline{HOST} = \text{HIGH}$), this pin is Test Mode Start, used to control the operation of the JTAG test.</p> <p>In host interface mode ($JTAG/\overline{HOST} = \text{LOW}$), this pin operates as the host interface chip select and is active LOW.</p>
F8	SCLK_TCK		Input	<p>COMMUNICATION SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Serial data clock signal.</p> <p>In JTAG mode ($JTAG/\overline{HOST} = \text{HIGH}$), this pin is the JTAG clock.</p> <p>In host interface mode ($JTAG/\overline{HOST} = \text{LOW}$), this pin is the host interface serial bit clock.</p> <p>All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.</p>

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
F9, F10, H9, H10, J8, J9, J10, K8, K9, K10	DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3		Output	<p>PARALLEL DATA BUS</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <hr/> <p>20-bit mode 20bit/10bit = HIGH</p> <p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}}$ = HIGH and DVB_ASI = LOW): Chroma data output for SD and HD data rates</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = HIGH): Not defined</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output</p> <hr/> <p>10-bit mode 20bit/10bit = LOW</p> <p>Forced LOW</p>
G3	$\overline{\text{RC_BYP}}$		Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.</p>
G7	$\overline{\text{SMPTE_BYPASS}}$		Input/Output	<p>CONTROL SIGNAL INPUT/OUTPUT</p> <p>Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Indicates the presence of valid SMPTE data.</p> <p>When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{\text{SMPTE_BYPASS}}$ is HIGH when the device locks to a SMPTE compliant input. $\overline{\text{SMPTE_BYPASS}}$ is LOW under all other conditions.</p> <p>When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is LOW, this pin is an INPUT:</p> <p>No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when $\overline{\text{SMPTE_BYPASS}}$ is set LOW.</p> <p>When $\overline{\text{SMPTE_BYPASS}}$ is set HIGH, the device carries out SMPTE scrambling and I/O processing.</p> <p>When $\overline{\text{SMPTE_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode.</p>

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G8	DVB_ASI		Input/Output	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to enable/disable DVB-ASI data extraction in manual mode.</p> <p>When the $\overline{\text{AUTO/MAN}}$ bit in the host interface is LOW, this pin is an input and when the DVB_ASI pin is set HIGH the device will carry out DVB_ASI data extraction and processing. The $\overline{\text{SMPTE_BYPASS}}$ pin must be set LOW. When $\overline{\text{SMPTE_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode.</p> <p>When the $\overline{\text{AUTO/MAN}}$ bit in the host interface is HIGH (default), DVB-ASI is configured as a status output (set LOW), and DVB-ASI input streams are not supported or recognized.</p>
H1	BUFF_VDD		Input Power	POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND		Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H5	TIM_861		Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to select CEA-861 timing mode.</p> <p>When TIM_861 is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSNC/DE) instead of H:V:F digital timing signals.</p>
H6	XTAL_OUT		Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.
H7	$\overline{20\text{bit}/10\text{bit}}$		Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to select the output bus width.</p> <p>HIGH = 20-bit, LOW = 10-bit.</p>
H8	$\overline{\text{IOPROC_EN/DIS}}$		Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to enable or disable video processing features. When IOPROC_EN is HIGH, the video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.</p>
J1, K1	SDO, $\overline{\text{SDO}}$		Output	<p>Serial Data Output Signal.</p> <p>50Ω CML buffer for interfacing to an external cable driver.</p> <p>Serial digital output signal operating at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.</p>

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
J2	SDO_EN/ $\overline{\text{DIS}}$		Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to enable/disable the serial digital output stage.</p> <p>When SDO_EN/$\overline{\text{DIS}}$ is LOW, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH.</p> <p>When SDO_EN/$\overline{\text{DIS}}$ is HIGH, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are enabled.</p>
J6, K6	XTAL2, XTAL1		Analog Input	Input connection for 27MHz crystal.
K2	STANDBY		Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down.</p> <p>In this mode, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH.</p>

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (EQ_VDD, BUFF_VDD, A_VDD)	-0.3V to +4.0V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Ambient Operating Temperature (T_A)	$-40^{\circ}\text{C} \leq T_A \leq 95^{\circ}\text{C}$
Storage Temperature (T_{STG})	$-40^{\circ}\text{C} \leq T_{STG} \leq 125^{\circ}\text{C}$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

NOTES:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	1
Supply Voltage, Serial Digital Input	EQ_VDD	–	3.13	3.3	3.47	V	–

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	1

NOTE:

1. The 3.3V supplies must track the 3.3V supply of an external CD.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I _{1V2}	10/20bit HD	–	160	200	mA	–
		10/20bit SD	–	130	170	mA	–
		DVB_ASI	–	130	170	mA	–
+1.8V Supply Current	I _{1V8}	10/20bit HD	–	15	21	mA	–
		10/20bit SD	–	4	7	mA	–
		DVB_ASI	–	4	6	mA	–
+3.3V Supply Current	I _{3V3}	10/20bit HD	–	110	135	mA	–
		10/20bit SD	–	90	100	mA	–
		DVB_ASI	–	90	95	mA	–
Total Device Power (IO_VDD = 1.8V)	P _{1D8}	10/20bit HD	–	460	560	mW	–
		10/20bit SD	–	410	490	mW	–
		DVB_ASI	–	410	490	mW	–
		Reset	–	390	–	mW	–
		Standby	–	23	45	mW	–
Total Device Power (IO_VDD = 3.3V)	P _{3D3}	10/20bit HD	–	550	700	mW	–
		10/20bit SD	–	440	540	mW	–
		DVB_ASI	–	440	530	mW	–
		Reset	–	410	–	mW	–
		Standby	–	23	45	mW	–
Digital I/O							
Input Logic LOW	V _{IL}	3.3V or 1.8V operation	IO_VSS -0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V _{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD +0.3	V	–
Output Logic LOW	V _{OL}	IOL = 5mA, 1.8V operation	–	–	0.2	V	–
		IOL = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V _{OH}	IOH = 5mA, 1.8V operation	1.4	–	–	V	–
		IOH = 8mA, 3.3V operation	2.4	–	–	V	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input							
Serial Input Common Mode Voltage	–	75Ω load	–	2.2	–	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD -(0.6/2)	BUFF_VDD -(0.45/2)	BUFF_VDD -(0.35/2)	V	–

Notes:

The output drive strength of the digital outputs can be programmed through the host interface. please see [Table 4-17: Configuration and Status Registers](#), register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency:		HD	44	–	48	PCLK	–
SMPTE mode, IOPROC_EN = 1	–	SD	46	–	53	PCLK	–
Device Latency:		HD	33	–	36	PCLK	–
SMPTE mode, IOPROC_EN = 0	–	SD	32	–	35	PCLK	–
Device Latency:		HD	6	–	9	PCLK	–
SMPTE bypass, IOPROC_EN = 0	–	SD	5	–	9	PCLK	–
Device Latency: DVB-ASI	–	SD	12	–	16	PCLK	–
Reset Pulse Width	t _{reset}	–	1	–	–	ms	–
Parallel Output							
Parallel Clock Frequency	f _{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC _{PCLK}	–	40	–	60	%	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes		
Output Data Hold Time (1.8V)	t_{oh}	HD 10-bit 6pF Load	DBUS	1.0	–	–	ns	1		
			STAT	1.0	–	–	ns	1		
		HD 20-bit 6pF Load	DBUS	1.0	–	–	ns	1		
			STAT	1.0	–	–	ns	1		
		SD 10-bit 6pF Load	DBUS	19.4	–	–	ns	1		
			STAT	19.4	–	–	ns	1		
		SD 20-bit 6pF Load	DBUS	38.0	–	–	ns	1		
			STAT	38.0	–	–	ns	1		
		Output Data Hold Time (3.3V)	t_{oh}	HD 10-bit 6pF Load	DBUS	1.0	–	–	ns	2
					STAT	1.0	–	–	ns	2
HD 20-bit 6pF Load	DBUS			1.0	–	–	ns	2		
	STAT			1.0	–	–	ns	2		
SD 10-bit 6pF Load	DBUS			19.4	–	–	ns	2		
	STAT			19.4	–	–	ns	2		
SD 20-bit 6pF Load	DBUS			38.0	–	–	ns	2		
	STAT			38.0	–	–	ns	2		
Output Data Delay Time (1.8V)	t_{od}			HD 10-bit 15pF Load	DBUS	–	–	3.7	ns	3
					STAT	–	–	4.4	ns	3
		HD 20-bit 15pF Load	DBUS	–	–	3.7	ns	3		
			STAT	–	–	4.4	ns	3		
		SD 10-bit 15pF Load	DBUS	–	–	22.2	ns	3		
			STAT	–	–	22.2	ns	3		
		SD 20-bit 15pF Load	DBUS	–	–	41.0	ns	3		
			STAT	–	–	41.0	ns	3		
		Output Data Delay Time (3.3V)	t_{od}	HD 10-bit 15pF Load	DBUS	–	–	3.7	ns	4
					STAT	–	–	4.1	ns	4
HD 20-bit 15pF Load	DBUS			–	–	3.7	ns	4		
	STAT			–	–	4.1	ns	4		
SD 10-bit 15pF Load	DBUS			–	–	22.2	ns	4		
	STAT			–	–	22.2	ns	4		
SD 20-bit 15pF Load	DBUS			–	–	41.0	ns	4		
	STAT			–	–	41.0	ns	4		

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
Output Data Rise/Fall Time (1.8V)	t_r/t_f	All modes 6pF Cload	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.4	ns	1
		All modes 15pF Cload	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.4	ns	3
Output Data Rise/Fall Time (3.3V)	t_r/t_f	All modes 6pF Cload	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
		All modes 15pF Cload	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.4	ns	4
Serial Digital Input								
Serial Input Data Rate	DR_{SDI}	–	0.27	–	1.485	Gb/s	–	
Serial Input Voltage Swing	ΔV_{SDI}	$T_A=25^\circ\text{C}$, differential, 270Mb/s & 1.485Gb/s	720	800	950	mV _{p-p}	6	
		$T_A=25^\circ\text{C}$, differential, 2.97Gb/s	720	800	880	mV _{p-p}	6	
Achievable Cable Length	–	Belden 1694A cable, HD	210	230	–	m	–	
		Belden 1694A cable, SD	400	440	–	m	–	
Input Return Loss	–	single-ended	15	21	–	dB	7	
Input Resistance	–	single-ended	–	1.52	–	k Ω	–	
Input Capacitance	–	single-ended	–	1	–	pF	–	
Serial Digital Output								
Serial Output Data Rate	DR_{SDO}	–	0.27	–	1.485	Gb/s	–	
Serial Output Swing	ΔV_{SDO}	Differential with 100 Ω load	320	–	600	mV _{p-p}	–	
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	–	–	–	180	ps	–	
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	–	–	–	180	ps	–	
Serial Output Jitter with loop-through mode	t_{OJ}	SMPTE colour bar HD, 210m	–	–	100	ps	–	
		SMPTE colour bar SD, 400m	–	–	470	ps	–	
Serial Output Duty Cycle Distortion	DCD_{SDO}	HD	–	10	–	ps	–	
		SD	–	20	–	ps	–	
Synchronous lock time	–	–	–	–	25	μs	–	
Asynchronous lock time	–	–	0.1	–	20	ms	–	

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Lock time from power-up	–	After 20 minutes at -20°C	–	–	5	s	–
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	60	MHz	5
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	5
GSPI Input Data Setup Time	–		1.5	–	–	ns	5
GSPI Input Data Hold Time	–		1.5	–	–	ns	5
GSPI Output Data Hold Time	–	–	1.5	–	–	ns	5
\overline{CS} low before SCLK rising edge	–	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	5
\overline{CS} high after SCLK falling edge	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	5

Notes:

1. 1.89V and 0°C.
2. 3.47V and 0°C.
3. 1.71V and 85°C
4. 3.13V and 85°C
5. Timing parameters defined in [Section 4.18.3](#)
6. 0m cable length
7. Tested on a GS1661 board from 5MHz to 1.485GHz.

3. Input/Output Circuits

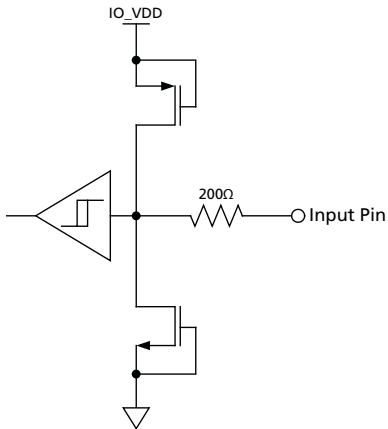


Figure 3-1: Digital Input Pin with Schmitt Trigger (20bit/10bit, $\overline{CS_TMS}$, SW_EN, IOPROC_EN/DIS, JTAG/HOST, $\overline{RC_BYP}$, $\overline{RESET_TRST}$, SCLK_TCK, SDIN_TDI, SDO_EN/DIS, STANDBY, TIM_861)

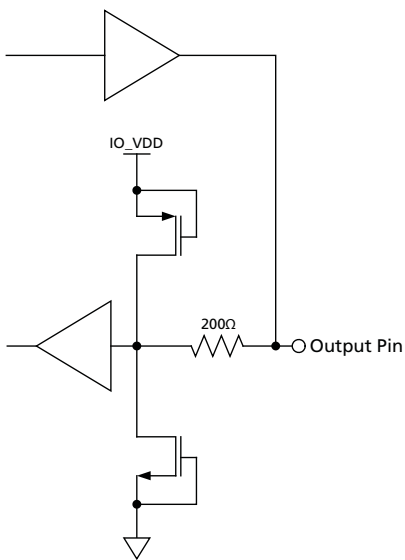


Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (DVB_ASI, $\overline{SMPTE_BYPASS}$)

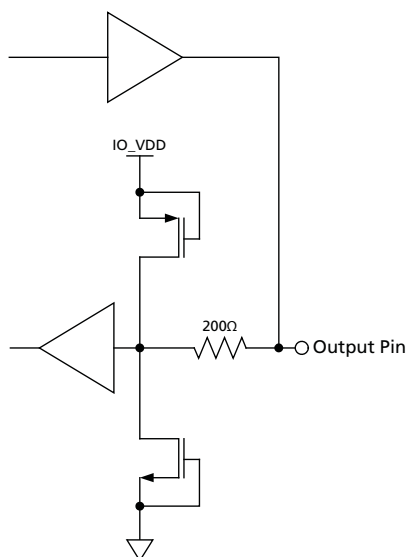


Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output unless in Reset Mode; in which case they are high-impedance. The drive strength can be set by writing to address 06Dh in the host interface register. (DOUT0, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, DOUT6, DOUT7, DOUT8, DOUT9, SDOUT_TDO, STAT0, STAT1, STAT2, STAT3, STAT4, STAT5, XTAL_OUT, DOUT10, DOUT11, DOUT12, DOUT13, DOUT14, DOUT15, DOUT16, DOUT17, DOUT18, DOUT19, PCLK)

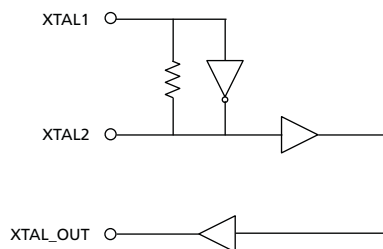


Figure 3-4: XTAL1/XTAL2/XTAL-OUT

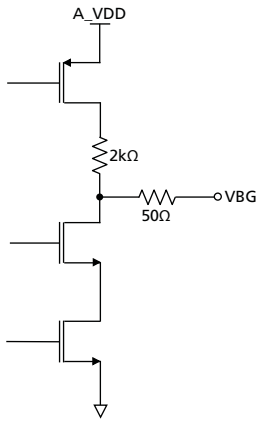


Figure 3-5: VBG

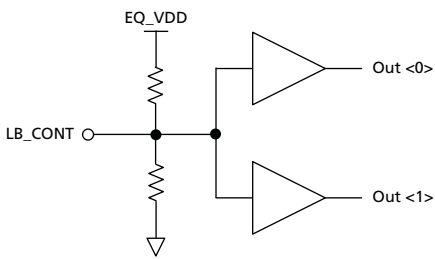


Figure 3-6: LB_CONT

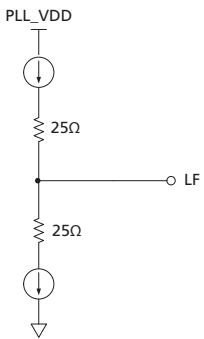


Figure 3-7: Loop Filter

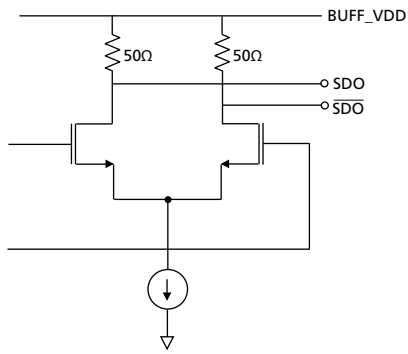


Figure 3-8: SDO/ $\overline{\text{SDO}}$

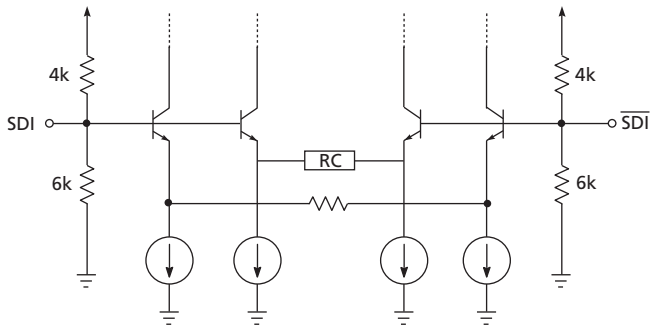


Figure 3-9: Equalizer Input Equivalent Circuit

4. Detailed Description

Refer to the document entitled **GS1660/GS1661 Errata** for this device (document number 53877).

4.1 Functional Overview

The GS1661 is a multi-rate SDI integrated Receiver which includes complete SMPTE processing, as per SMPTE 292M and SMPTE 259M-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The GS1661 integrates Gennum's adaptive cable equalizer technology, achieving unprecedented cable lengths and jitter tolerance. It features DC restoration to compensate for the DC content of SMPTE pathological signals.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The Serial Digital Output can be connected to an external Cable Driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode, the GS1661 performs SMPTE de-scrambling and NRZI to NRZ decoding and word alignment. Line-based CRC errors, line number errors, TRS errors and ancillary data check sum errors can all be detected. The GS1661 also provides ancillary data extraction. The entire ancillary data packet is extracted, and written to host-accessible registers. Other processing functions include H:V:F timing extraction, Luma and Chroma ancillary data indication, video standard detection, and SMPTE 352M packet detection and decoding. All of the processing features are optional, and may be enabled or disabled via the Host Interface.

In DVB-ASI mode, 8b/10b decoding is applied to the received data stream.

In Data-Through mode, all forms of SMPTE and DVB-ASI decoding are disabled, and the device can be used as a simple serial to parallel converter.

The device can also be placed in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static. Placing the Receiver in Standby mode will automatically place the integrated equalizer in power down mode as well.

Parallel data outputs are provided in 20-bit or 10-bit multiplexed format for HD and SD video rates. In all cases, this 20-bit parallel bus can be multiplexed onto 10 bits for a low pin count interface with downstream devices. The associated Parallel Clock input signal operates at 148.5 or 148.5/1.001MHz (for all HD 10-bit multiplexed modes), 74.25 or 74.25/1.001MHz (for HD 20-bit mode), 27MHz (for SD 10-bit mode) and 13.5MHz (for SD 20-bit mode).

4.2 Serial Digital Input

The GS1661 can accept serial digital inputs compliant with SMPTE 292 and SMPTE 259M-C.

4.2.1 Integrated Adaptive Cable Equalizer

The GS1661 integrates Gennum's adaptive cable equalizer technology.

The integrated adaptive equalizer can equalize HD and SD serial digital signals, and will typically equalize 230m of Belden 1694A cable at 1.485Gb/s and 440m at 270Mb/s. The integrated adaptive equalizer is powered from a single +3.3V power supply and consumes approximately 195mW of power.

The equalizer can be bypassed by programming register 073h through the GSPI interface.

4.2.1.1 Serial Digital Inputs

The Serial Data Signal may be connected to the input pins (SDI/ $\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

4.2.1.2 Cable Equalization

The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling.

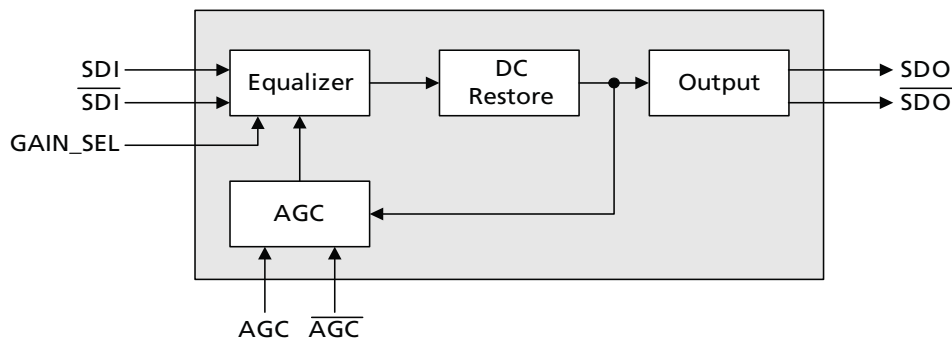


Figure 4-1: GS1661 Integrated EQ Block Diagram