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SEMTECH
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GS1662

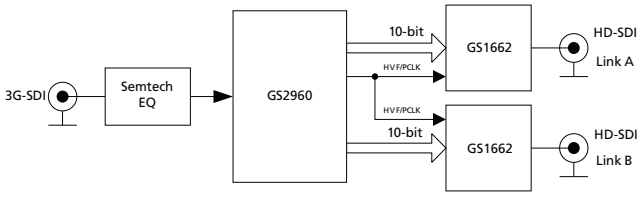
HD/SD-SDI Serializer with Complete SMPTE Video Support

Key Features

- Operation at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE ST 292, SMPTE ST 259-C and DVB-ASI
- Integrated Cable Driver
- Integrated, low-noise VCO
- Integrated ClockCleaner™
- Ancillary data insertion
- Parallel data bus selectable as either 20-bit or 10-bit
- SMPTE video processing including TRS calculation and insertion, line number calculation and insertion, line based CRC calculation and insertion, illegal code re-mapping, SMPTE ST 352 payload identifier generation and insertion
- GSPI host interface
- +1.2V digital core power supply, +1.2V and +3.3V analog power supplies, and selectable +1.8V or +3.3V I/O power supply
- -20°C to +85°C operating temperature range
- Low power operation (typically at 330mW, including Cable Driver)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

Applications

Application: Single Link (3G-SDI) to Dual Link (HD-SDI) Converter



Description

The GS1662 is a complete SDI Transmitter, generating a SMPTE ST 292, SMPTE ST 259-C or DVB-ASI compliant serial digital output signal.

The integrated ClockCleaner™ allows the device to accept parallel clocks with greater than 300ps input jitter and still provide a SMPTE compliant serial digital output.

The device can operate in four basic user selectable modes: SMPTE mode, DVB-ASI mode, Data-Through mode, or Standby mode.

In SMPTE mode, the GS1662 performs SMPTE scrambling and NRZ to NRZI coding. In addition, the device can insert TRS words, calculate and insert line numbers and line based CRC's, re-map illegal code words, map 8-bit TRS to 10-bit TRS, calculate and insert EDH CRC's and flags, and insert SMPTE ST 352 payload identifier packets. All of the processing features are optional, and may be disabled via external control pins and/or via the Host Interface.

The GS1662 provides ancillary data insertion in SMPTE mode as well. The entire ancillary packet is programmed into internal registers through the GSPI Host Interface, including the Ancillary Data Flag (ADF), Data Identification words (DID and SDID) and checksum. The GS1662 then recalculates the checksum and inserts the complete ancillary packet into the video stream.

In DVB-ASI mode, the device will perform 8b/10b encoding prior to transmission.

In Data-Through mode, all SMPTE and DVB-ASI processing is disabled, and the device can be used as a simple parallel to serial converter.

The device can also operate in a lower power Standby mode. In this mode, no signal is generated at the output.

Parallel data inputs must be provided in 20-bit or 10-bit multiplexed format for HD and SD video rates. The associated Parallel Clock input signal operates at 148.5 or 148.5/1.001MHz (HD 10-bit multiplexed format), 74.25 or 74.25/1.001MHz (for HD 20-bit format), 27MHz (for SD 10-bit format) and 13.5MHz (for SD 20-bit format).

The GS1662 includes an integrated Cable Driver fully compliant with SMPTE ST 259-C and SMPTE ST 292. It features automatic dual slew-rate selection, depending on HD or SD operational requirements.

Functional Block Diagram

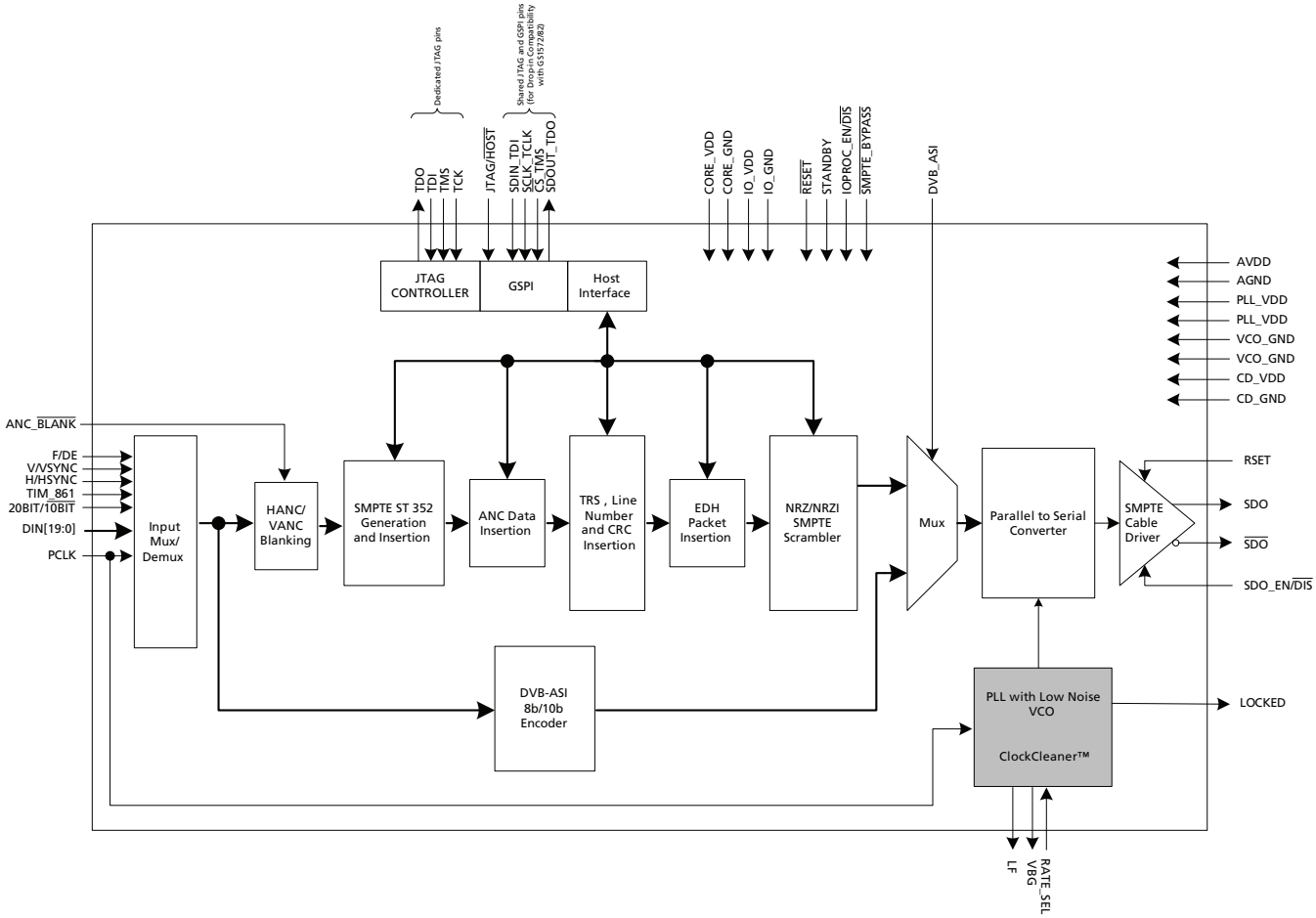


Figure A: GS1662 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
4	014806	–	September 2013	Updates throughout the document.
3	155080	56060	October 2010	Revised power rating in standby mode. Documented CSUM behaviour in Section 4.7, Section 4.8.3 and Configuration and Status Registers.
2	153743	–	March 2010	Correction to ANC Data Insertion addresses 040h - 13Fh in Table 4-16: Configuration and Status Registers. Changed Reset Pulse width from 10ms to 1ms in Table 2-4: AC Electrical Characteristics and 4.16 Device Reset. Changed Pin E4 to IO_GND.
1	153472	–	January 2010	Converted to Data Sheet.
0	153210	–	November 2009	Converted to Preliminary Data Sheet. Changed pin E4 to RSV in Pin Assignment, Pin Descriptions and Typical Application Circuit.
A	152910	–	October 2009	New Document.

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	DIN17	DIN18	F/DE	H/HSYNC	CORE_VDD	PLL_VDD	LF	VBG	RSV	A_VDD
B	DIN15	DIN16	DIN19	PCLK	CORE_GND	PLL_VDD	VCO_VDD	VCO_GND	A_GND	A_GND
C	DIN13	DIN14	DIN12	V/VSYNC	CORE_GND	PLL_GND	PLL_GND	PLL_GND	CD_GND	SDO
D	DIN11	DIN10	STANDBY	SDO_EN/$\overline{DIS}$	CORE_GND	RSV	RSV	RSV	CD_GND	$\overline{SDO}$
E	CORE_VDD	CORE_GND	RATE_SEL	IO_GND	CORE_GND	CORE_GND	TDI	TMS	CD_GND	CD_VDD
F	DIN9	DIN8	DETECT_TRS	CORE_GND	CORE_GND	CORE_GND	CORE_GND	TDO	CD_GND	RSET
G	IO_VDD	IO_GND	TIM_861	20bit/$\overline{10bit}$	DVB_ASI	$\overline{SMPTE\_BYPASS}$	IOPROC_EN/$\overline{DIS}$	$\overline{RESET}$	CORE_GND	CORE_VDD
H	DIN7	DIN6	$\overline{ANC\_BLANK}$	LOCKED	CORE_GND	CORE_GND	RSV	JTAG/$\overline{HOST}$	IO_GND	IO_VDD
J	DIN5	DIN4	DIN1	RSV	RSV	RSV	RSV	TCK	SDOUT_TDO	SCLK_TCK
K	DIN3	DIN2	DIN0	RSV	RSV	RSV	RSV	CORE_VDD	$\overline{CS}$_TMS	SDIN_TDI

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description	
B3, A2, A1, B2, B1, C2, C1, C3, D1, D2	DIN[19:10]		Input	PARALLEL DATA BUS Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.	
				20-bit mode 20BIT/$\overline{10BIT}$ = HIGH	Luma data input in SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{SMPTE\_BYPASS}$ = LOW)
				10-bit mode 20BIT/$\overline{10BIT}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{SMPTE\_BYPASS}$ = LOW) DVB-ASI data input in DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW) (DVB_ASI = HIGH)
A3	F/DE	Synch-ronous with PCLK	Input	PARALLEL DATA TIMING. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. TIM_861 = LOW: Used to indicate the ODD / EVEN field of the video signal when DETECT_TRS is set LOW. The device will set the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH (IOPROC_EN/$\overline{DIS}$ must also be HIGH). The F signal should be set HIGH for the entire period of field 2 and should be set LOW for all lines in field 1 and for all lines in progressive scan systems. The F signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The DE signal is used to indicate the active video period when DETECT_TRS is set LOW. DE is HIGH for active data and LOW for blanking. See Section 4.3 and Section 4.3.2 for timing details. The DE signal is ignored when DETECT_TRS = HIGH.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A4	H/HSYNC	Synch-ronous with PCLK	Input	PARALLEL DATA TIMING. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. TIM_861 is LOW: The H signal is used to indicate the portion of the video line containing active video data, when DETECT_TRS is set LOW. Active Line Blanking The H signal should be LOW for the active portion of the video line. The signal goes LOW at the first active pixel of the line, and then goes HIGH after the last active pixel of the line. The H signal should be set HIGH for the entire horizontal blanking period, including both EAV and SAV TRS words, and LOW otherwise. TRS Based Blanking (H_CONFIG = 1_h) The H signal should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise. TIM_861 = HIGH: The HSYNC signal indicates horizontal timing. See Section 4.3. When DETECT_TRS is HIGH, this pin is ignored at all times. If DETECT_TRS is set HIGH and TIM_861 is set HIGH, the DETECT_TRS feature will take priority.
A5, E1, G10, K8	CORE_VDD		Input Power	Power supply connection for digital core logic. Connect to +1.2V DC digital.
A6, B6	PLL_VDD		Input Power	Power supply pin for PLL. Connect to +1.2V DC analog.
A7	LF		Analog Output	Loop Filter component connection.
A8	VBG		Output	Bandgap voltage filter connection.
A9, D6, D7, D8, H7, J4, J5, J6, J7, K4, K5, K6, K7	RSV		–	These pins are reserved and should be left unconnected.
A10	A_VDD		Input Power	VDD for sensitive analog circuitry. Connect to +3.3VDC analog.
B4	PCLK		Input	PARALLEL DATA BUS CLOCK. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. HD 20-bit mode: PCLK @ 74.25MHz HD 10-bit mode: PCLK @ 148.5MHz SD 20-bit mode: PCLK @ 13.5MHz SD 10-bit mode: PCLK @ 27MHz DVB-ASI mode: PCLK @ 27MHz
B5, C5, D5, E2, E5, E6, F4, F5, F6, F7, G9, H5, H6	CORE_GND		Input Power	Reserved. Connect to CORE_GND.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
B7	VCO_VDD		Input Power	Power pin for VCO. Connect to +1.2V DC analog followed by an RC filter (see Typical Application Circuit on page 66). VCO_VDD is nominally 0.7V.
B8	VCO_GND		Input Power	Ground connection for VCO. Connect to analog GND.
B9, B10	A_GND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
C4	V/VSYNC	Synch-ronous with PCLK	Input	PARALLEL DATA TIMING. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. TIM_861 = LOW: The V signal is used to indicate the portion of the video field/frame that is used for vertical blanking, when DETECT_TRS is set LOW. The V signal should be set HIGH for the entire vertical blanking period and should be set LOW for all lines outside of the vertical blanking interval. The V signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The VSYNC signal indicates vertical timing. See Section 4.3 for timing details. The VSYNC signal is ignored when DETECT_TRS = HIGH.
C6, C7, C8	PLL_GND		Input Power	Ground connection for PLL. Connect to analog GND.
C9, D9, E9, F9	CD_GND		Input Power	Ground connection for the serial digital cable driver. Connect to analog GND.
C10, D10	SDO, $\overline{\text{SDO}}$		Output	Serial Data Output Signal. Serial digital output signal operating at 1.485Gb/s, 1.485 /1.001Gb/s or 270Mb/s. The slew rate of the output is automatically controlled to meet SMPTE ST 292 and ST 259 specifications according to the setting of the RATE_SEL pin.
D3	STANDBY		Input	Standby input. HIGH to place the device in Standby mode.
D4	SDO_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable or disable the serial digital output stage. When SDO_EN/$\overline{\text{DIS}}$ is LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When SDO_EN/$\overline{\text{DIS}}$ is HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
E3	RATE_SEL		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to configure the operating data rate. RATE_SEL: 0 → Data Rate: 1.485 or 1.485/1.001Gb/s RATE_SEL: 1 → Data Rate: 270Mb/s
E7	TDI		Input	COMMUNICATION SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Dedicated JTAG pin. Test data in. This pin is used to shift JTAG test data into the device when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
E8	TMS		Input	COMMUNICATION SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Dedicated JTAG pin. Test mode start. This pin is JTAG Test Mode Start, used to control the operation of the JTAG test when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
E10	CD_VDD		Input Power	Power for the serial digital cable driver. Connect to +3.3V DC analog.
F1, F2, H1, H2, J1, J2, K1, K2, J3, K3	DIN[9:0]		Input	PARALLEL DATA BUS. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. In 10-bit mode, these pins are not used. 20-bit mode (20BIT/$\overline{\text{10BIT}}$ = HIGH): Chroma data input in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH, DVB_ASI = LOW); Data input in data through mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW, DVB_ASI = LOW); Not Used in DVB-ASI mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW, DVB_ASI = HIGH) 10-bit mode (20BIT/$\overline{\text{10BIT}}$ = LOW): Not used.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
F3	DETECT_TRS		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select external HVF timing mode or TRS extraction timing mode. When DETECT_TRS is LOW, the device extracts all internal timing from the supplied H:V:F or CEA-861 timing signals, dependent on the status of the TIM861 pin. When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.
F8	TDO		Output	COMMUNICATION SIGNAL OUTPUT. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Dedicated JTAG pin. JTAG Test Data Output. This pin is used to shift results from the device when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
F10	RSET		Input	An external 1% resistor connected to this input is used to set the SDO/$\overline{\text{SDO}}$ output signal amplitude.
G1, H10	IO_VDD		Input Power	Power connection for digital I/O. Connect to +3.3V or +1.8V DC digital.
E4, G2, H9	IO_GND		Input Power	Ground connection for digital I/O. Connect to digital GND.
G3	TIM_861		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select external CEA-861 timing mode. When DETECT_TRS is LOW and TIM-861 is LOW, the device extracts all internal timing from the supplied H:V:F timing signals. When DETECT_TRS is LOW and TIM-861 is HIGH, the device extracts all internal timing from the supplied HSYNC, VSYNC, DE timing signals. When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.
G4	20bit/$\overline{\text{10bit}}$		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select the input bus width.
G5	DVB_ASI		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable/disable the DVB-ASI data transmission. When DVB_ASI is set HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is set LOW, then the device will carry out DVB-ASI word alignment, I/O processing and transmission. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in data-through mode.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G6	$\overline{\text{SMPTE\_BYPASS}}$		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable / disable all forms of encoding / decoding, scrambling and EDH insertion. When set LOW, the device operates in data through mode (DVB_ASI= LOW), or in DVB-ASI mode (DVB_ASI = HIGH). No SMPTE scrambling takes place and none of the I/O processing features of the device are available when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW. When set HIGH, the device carries out SMPTE scrambling and I/O processing.
G7	IOPROC_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable or disable the I/O processing features. When IOPROC_EN/$\overline{\text{DIS}}$ is HIGH, the I/O processing features of the device are enabled. When IOPROC_EN/$\overline{\text{DIS}}$ is LOW, the I/O processing features of the device are disabled. Only applicable in SMPTE mode.
G8	$\overline{\text{RESET}}$		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG/$\overline{\text{HOST}}$ = LOW). When LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG/$\overline{\text{HOST}}$ = HIGH). When LOW, all functional blocks will be set to default and the JTAG test sequence will be reset. When HIGH, normal operation of the JTAG test sequence resumes.
H3	$\overline{\text{ANC\_BLANK}}$		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. When $\overline{\text{ANC\_BLANK}}$ is LOW, the Luma and Chroma input data is set to the appropriate blanking levels during the H and V blanking intervals. When $\overline{\text{ANC\_BLANK}}$ is HIGH, the blanking function is disabled. Only applicable in SMPTE mode.
H4	LOCKED		Output	STATUS SIGNAL OUTPUT. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. PLL lock indication. HIGH indicates PLL is locked. LOW indicates PLL is not locked.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H8	JTAG/$\overline{\text{HOST}}$		Input	CONTROL SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select JTAG test mode or host interface mode. When JTAG/$\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/$\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes and the separate JTAG pins become the JTAG port.
J8	TCK		Input	COMMUNICATION SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. JTAG Serial Data Clock Signal. This pin is the JTAG clock when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
J9	SDOUT_TDO		Output	COMMUNICATION SIGNAL OUTPUT. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Shared JTAG/$\overline{\text{HOST}}$ pin. Provided for compatibility with the GS1582. Serial Data Output/Test Data Output. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) This pin operates as the host interface serial output, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is used to shift test results and operates as the JTAG test data output, TDO (for new designs, use the dedicated JTAG port). **Note:** If the host interface is not being used leave this pin unconnected. IO_VDD = +3.3V Drive Strength = 12mA IO_VDD = +1.8V Drive Strength = 4mA
J10	SCLK_TCK		Input	COMMUNICATION SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Shared JTAG/HOST pin. Provided for pin compatibility with GS1582. Serial data clock signal. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is the TEST MODE START pin, used to control the operation of the JTAG test clock, TCK (for new designs, use the dedicated JTAG port). **Note:** If the host interface is not being used, tie this pin HIGH.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
K9	$\overline{CS}$_TMS		Input	COMMUNICATION SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Chip select / test mode start. JTAG Test mode (JTAG/$\overline{HOST}$ = HIGH) $\overline{CS}$_TMS operates as the JTAG test mode start, TMS, used to control the operation of the JTAG test, and is active HIGH (for new designs, use the dedicated JTAG port). Host mode (JTAG/$\overline{HOST}$ = LOW), $\overline{CS}$_TMS operates as the host interface Chip Select, $\overline{CS}$, and is active LOW.
K10	SDIN_TDI		Input	COMMUNICATION SIGNAL INPUT. Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Shared JTAG/HOST pin. Provided for pin compatibility with GS1582. Serial data in/test data in. In JTAG mode, this pin is used to shift test data into the device (for new designs, use the dedicated JTAG port). In host interface mode, this pin is used to write address and configuration data words into the device.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +3.6V
Supply Voltage, Analog +1.2V (PLL_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog +3.3V (CD_VDD, A_VDD)	-0.3V to +3.6V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Operating Temperature Range	-20°C to +85°C
Functional Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in Table 2-1 is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	+1.8V mode	1.71	1.8	1.89	V	–
		+3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	–
Supply Voltage, CD	CD_VDD	–	3.13	3.3	3.47	V	–
Operating Temperature Range	–	–	-20	–	85	°C	2
Functional Temperature Range	–	–	-40	–	85	°C	2

Notes:

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor. See Typical Application Circuit on page 66.
2. Operating Temperature Range guarantees the parameters given in the DC Electrical Characteristics and AC Electrical Characteristics. Functional Temperature Range guarantees a device start-up.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

V_{CC} = +3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10/20bit HD	–	90	150	mA	–
		10/20bit SD	–	75	120	mA	–
		DVB_ASI	–	75	120	mA	–
+1.8V Supply Current	I_{1V8}	10/20bit HD	–	10	25	mA	–
		10/20bit SD	–	3	10	mA	–
		DVB_ASI	–	3	10	mA	–
+3.3V Supply Current	I_{3V3}	10/20bit HD	–	80	100	mA	–
		10/20bit SD	–	70	90	mA	–
		DVB_ASI	–	70	90	mA	–
Total Device Power (IO_VDD = +1.8V)	P_{1D8}	10/20bit HD	–	330	490	mW	–
		10/20bit SD	–	300	450	mW	–
		DVB_ASI	–	300	410	mW	–
		Reset	–	200	–	mW	–
		Standby	–	100	180	mW	1
Total Device Power (IO_VDD = +3.3V)	P_{3D3}	10/20bit HD	–	370	500	mW	–
		10/20bit SD	–	320	450	mW	–
		DVB_ASI	–	320	450	mW	–
		Reset	–	230	–	mW	–
		Standby	–	110	180	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	+3.3V or +1.8V operation	IO_VSS-0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	+3.3V or +1.8V operation	0.7 x IO_VDD	–	IO_VDD+0.3	V	–
Output Logic LOW	V_{OL}	IOL=5mA, +1.8V operation	–	–	0.2	V	–
		IOL=8mA, +3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOH=-5mA, +1.8V operation	1.4	–	–	V	–
		IOH=-8mA, +3.3V operation	2.4	–	–	V	–
Serial Output							
Serial Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET = 750Ω SD and HD mode	–	CD_VDD - (V_{SDD}/2)	–	V	–

Notes:

1. Devices manufactured prior to April 1, 2011 consume 150mW of power in Standby mode.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

V_{CC} = +3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency	–	HD bypass (PCLK = 74.25MHz)	–	54	–	PCLK	–
	–	HD SMPTE (PCLK = 74.25MHz)	–	95	–	PCLK	–
	–	SD bypass (PCLK = 27MHz)	–	54		PCLK	–
	–	SD SMPTE (PCLK = 27MHz)	–	112		PCLK	–
	–	DVB-ASI	–	52	–	PCLK	–
Reset Pulse Width	t_{reset}	–	1	–	–	ms	–
Parallel Input							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Input Data Setup Time	t_{su}	50% levels; +3.3V or +1.8V operation	1.2	–	–	ns	1
Input Data Hold Time	t_{ih}		0.8	–	–	ns	1
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	–	1.485	–	Gb/s	–
		–	–	1.485/1.001	–	Gb/s	–
		–	–	270	–	Mb/s	–
Serial Output Swing	V_{SDD}	RSET = 750Ω 75Ω load	750	800	850	mV_{pp}	–
Serial Output Rise/Fall Time 20% ~ 80%	trf_{SDO}	HD mode	–	120	135	ps	–
	trf_{SDO}	SD mode	400	660	800	ps	–
Mismatch in rise/fall time	Δt_r , Δt_f	–	–	–	35	ps	–
Duty Cycle Distortion	–	–	–	–	5	%	2
Overshoot	–	HD mode	–	5	10	%	2
	–	SD mode	–	3	8	%	2
Output Return Loss	ORL	5 MHz - 1.485 GHz	–	-18	–	dB	3
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and SMPTE Colour Bars HD signal	–	50	95	ps	4, 6
	t_{OJ}	Pseudorandom and SMPTE Colour Bars SD signal	–	200	400	ps	5
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels +3.3V or +1.8V operation	–	–	80	MHz	–
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	–
GSPI Input Data Setup Time	–		1.5	–	–	ns	–
GSPI Input Data Hold Time	–		1.5	–	–	ns	–

Table 2-4: AC Electrical Characteristics (Continued)

V_{CC} = +3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
GSPI Output Data Hold Time	–	15pF load	1.5	–	–	ns	–
$\overline{CS}$ low before SCLK rising edge	t_0	50% levels +3.3V or +1.8V operation	1.5	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	t_4	50% levels +3.3V or +1.8V operation	PCLK (MHz): unlocked / 13.5 / 27.0 / 74.25 / 148.5 — ns: 445 / 74.2 / 37.1 / 13.5 / 6.7	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	t_5	50% levels +3.3V or +1.8V operation	PCLK (MHz): unlocked / 13.5 / 27.0 / 74.25 / 148.5 — ns: 1187 / 297 / 148.4 / 53.9 / 27	–	–	ns	–
$\overline{CS}$ high after SCLK falling edge	t_7	50% levels +3.3V or +1.8V operation	PCLK (MHz): unlocked / 13.5 / 27.0 / 74.25 / 148.5 — ns: 445 / 74.2 / 37.1 / 13.5 / 6.7	–	–	ns	–

Notes:

1. Input setup and hold time is dependent on the rise and fall time on the parallel input. Parallel clock and data with rise time or fall time greater than 500ps require larger setup and hold times.
2. Single Ended into 75Ω external load.
3. ORL depends on board design.
4. Alignment Jitter = measured from 100kHz to serial data rate/10.
5. Alignment Jitter = measured from 1kHz to 27MHz.
6. This is the maximum jitter for a BER of 10-12. The equivalent jitter value as per RP184 is 40ps max.

3. Input/Output Circuits

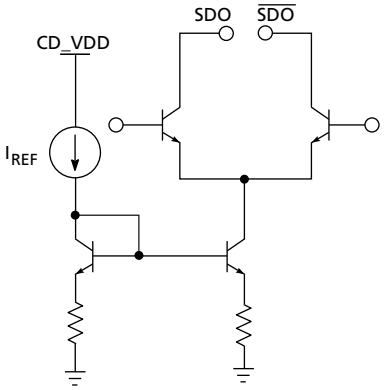

Figure 3-1: Differential Output Stage (SDO/SDO)

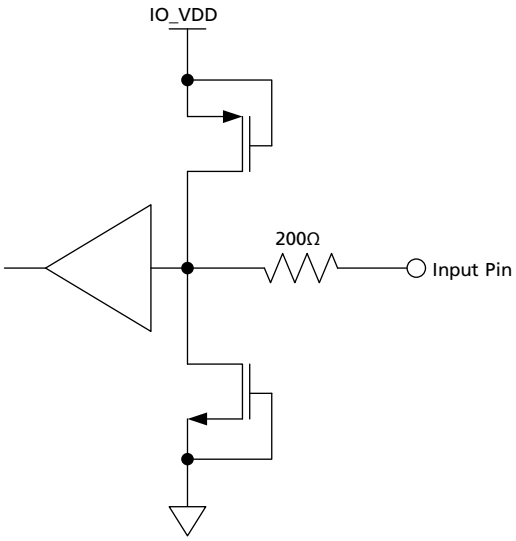

Figure 3-2: Digital Input Pin (20bit/10bit, ANC_BLANK, DETECT_TRS, DVB_ASI, RATE_SEL, SMPTE_BYPASS, TIM_861, F/DE, H/HSYNC, PCLK, V/VSYNC)

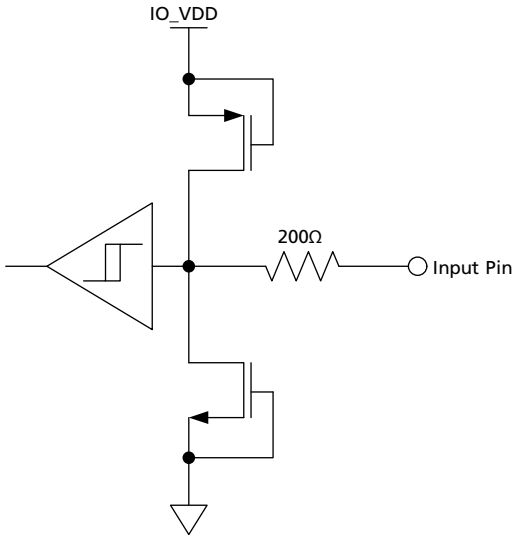

Figure 3-3: Digital Input Pin with Schmitt Trigger ($\overline{\text{RESET}}$)

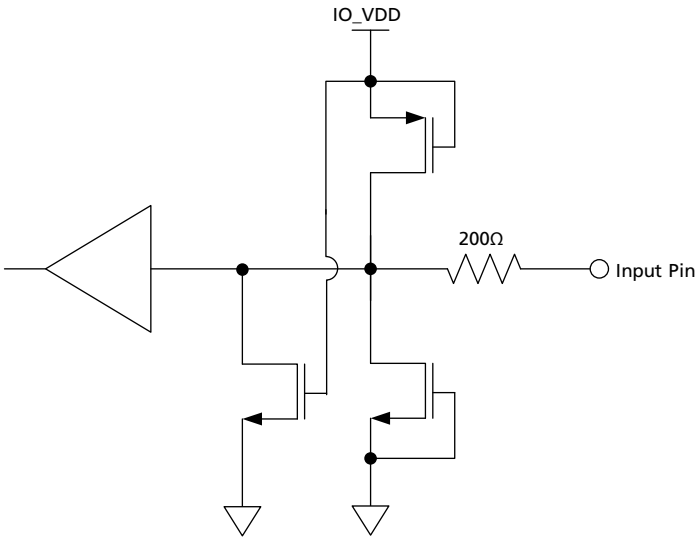

Figure 3-4: Digital Input Pin with weak pull-down - maximum pull-down current <110µA (JTAG/$\overline{\text{HOST}}$, STANDBY, SCLK_TCK, SDIN_TDI, TCK, TDI)

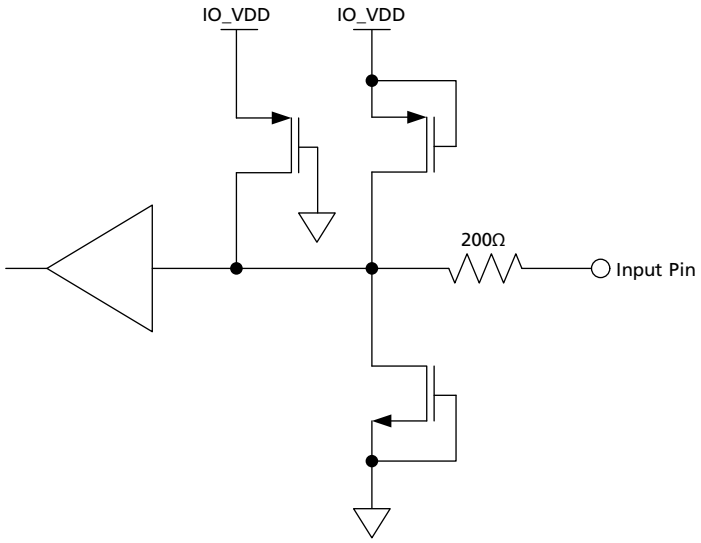

Figure 3-5: Digital Input Pin with weak pull-up - maximum pull-up current <110µA ($\overline{CS}$_TMS, SDO_EN/$\overline{DIS}$, TMS)

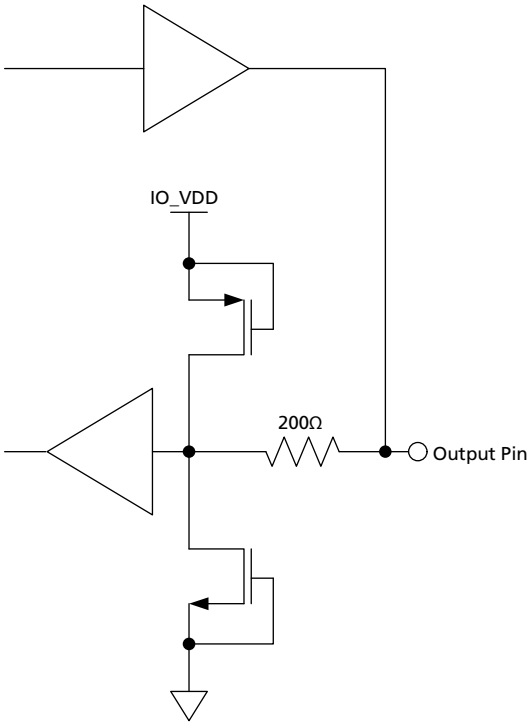

Figure 3-6: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to input at all times except in test mode. (DIN0, DIN2, DIN3, DIN4, DIN5, DIN6, DIN7, DIN8, DIN9, DIN10, DIN11, DIN12, DIN13, DIN14, DIN15, DIN16, DIN17, DIN18, DIN19, DIN1)

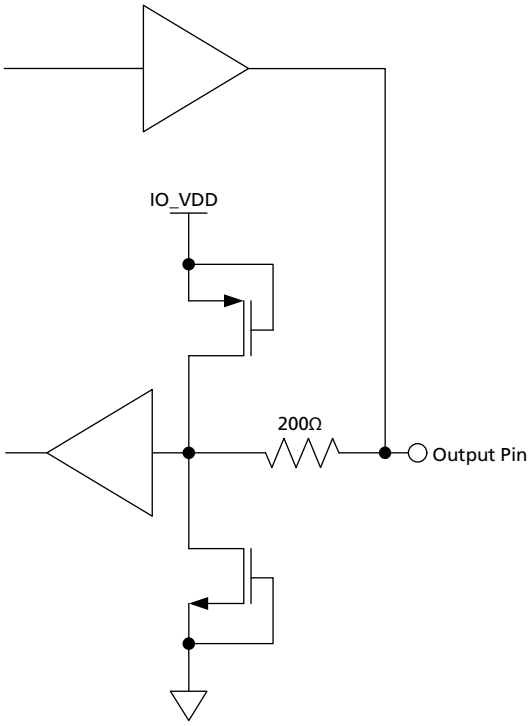

Figure 3-7: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output at all times except in reset mode. (LOCKED, SDOUT_TDO, TDO)

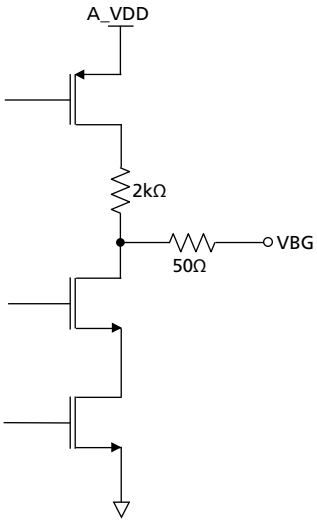

Figure 3-8: VBG

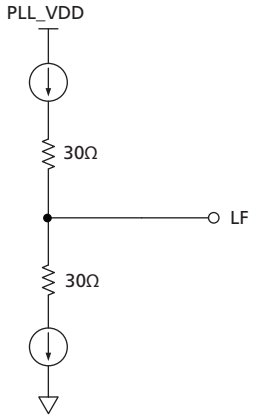

Figure 3-9: Loop Filter

4. Detailed Description

4.1 Functional Overview

The GS1662 is a multi-rate Transmitter with integrated SMPTE digital video processing and an integrated Cable Driver. It provides a complete transmit solution at 1.485Gb/s, 1.485/1.001Gb/s or 270Mb/s.

The device has four basic modes of operation that must be set through external device pins: SMPTE mode, DVB-ASI mode, Data-Through mode and Standby mode.

In SMPTE mode, the device will accept 10-bit multiplexed or 20-bit demultiplexed SMPTE compliant data. By default, the device's additional processing features will be enabled in this mode.

In DVB-ASI mode, the GS1662 will accept an 8-bit parallel DVB-ASI compliant transport stream on DIN[17:10]. The serial output data stream will be 8b/10b encoded with stuffing characters added as per the standard.

Data-Through mode allows for the serializing of data not conforming to SMPTE or DVB-ASI streams. No additional processing will be done in this mode.

In addition, the device may be put into Standby, to reduce power consumption.

The serial digital output features a high-impedance mode and adjustable signal swing. The output slew rate is automatically set by the RATE_SEL pin setting.

The GS1662 provides several data processing functions; including generic ANC insertion, SMPTE ST 352 and EDH data packet generation and insertion, automatic video standards detection, and TRS, CRC, ANC data checksum, and line number calculation and insertion. These features are all enabled/disabled collectively using the external I/O processing pin, but may be individually disabled via internal registers accessible through the GSPI host interface.

Finally, the GS1662 contains a JTAG interface for boundary scan test implementations.

4.2 Parallel Data Inputs

Data signal inputs enter the device on the rising edge of PCLK, as shown in Figure 4-1.

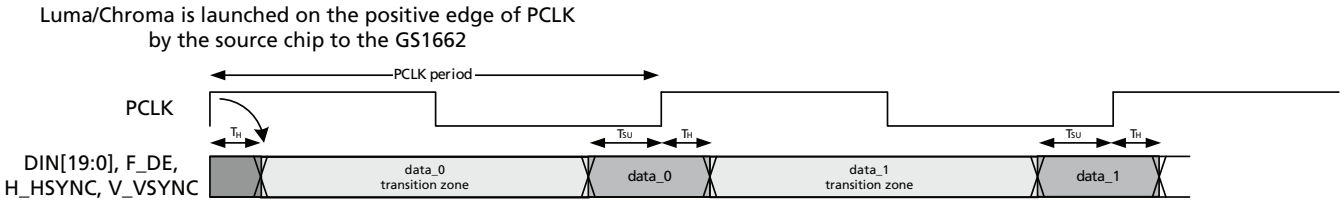

Figure 4-1: GS1662 Video Host Interface Timing Diagrams