Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SEMTECH
GENNUM PRODUCTS

GS1670

HD/SD SDI Receiver Complete with SMPTE Audio and Video Processing

Key Features

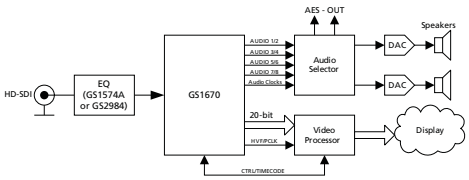
- Operation at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE 292, SMPTE 259M-C and DVB-ASI
- Integrated Reclocker with low phase noise, integrated VCO
- Serial digital reclocked, or non-reclocked loop-through output
- Integrated audio de-embedder for 8 channels of 48kHz audio
- Integrated audio clock generator
- Ancillary data extraction
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 timing signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI host interface
- -20°C to +85°C operating temperature range
- Low power operation (typically 300mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

Errata

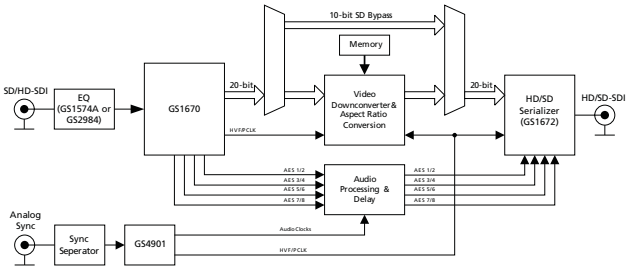
Refer to Errata document entitled **GS1670/GS1671 Errata** for this device (document number **53878**).

Applications

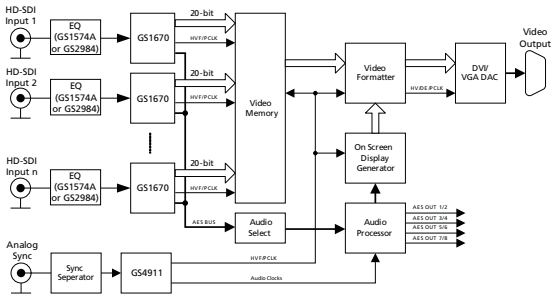
Application: 1080p30 or 720p60 Monitor



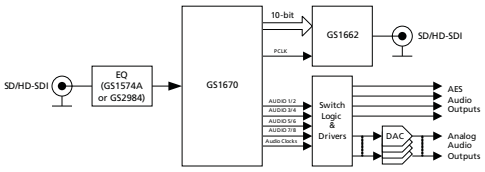
Application: Multi-format Downconverter



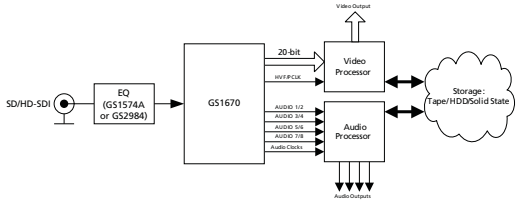
Application: Multi-input Video Monitoring System



Application: Multi-format Audio De-embedder Module



Application: Multi-format Digital VTR/Video Server



Description

The GS1670 is a multi-rate SDI Receiver which includes complete SMPTE processing, as per SMPTE 292 and SMPTE 259M-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop-through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The serial digital output can be connected to an external cable driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode, the GS1670 performs SMPTE de-scrambling and NRZI to NRZ decoding and word alignment. Line-based CRC errors, line number errors, TRS errors and ancillary data check sum errors can all be detected. The GS1670 also provides ancillary data extraction. The entire ancillary data packet is extracted, and written to host-accessible registers. Other processing functions include H:V:F timing extraction, Luma and Chroma ancillary data indication, video standard detection, and SMPTE 352M packet detection and decoding. All of the processing features are optional, and may be enabled or disabled via the Host Interface.

In DVB-ASI mode, 8b/10b decoding is applied to the received data stream.

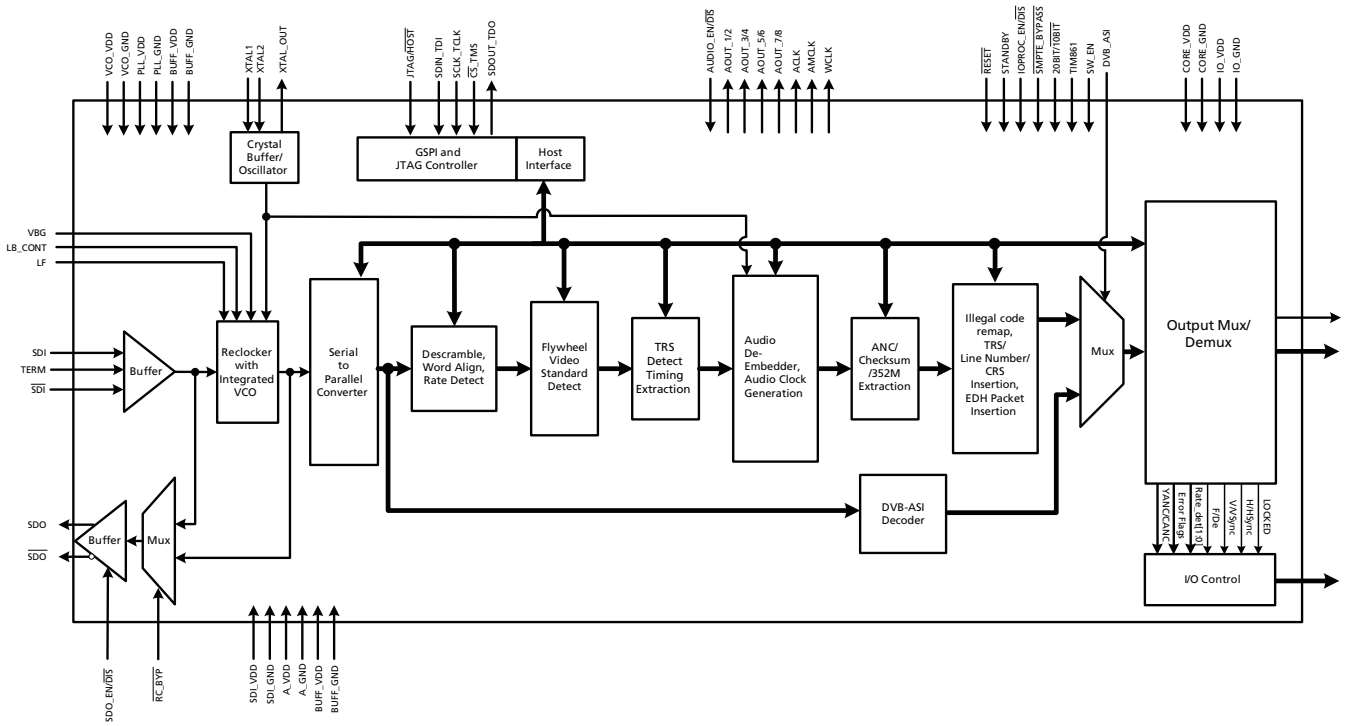
In Data-Through mode all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

The device can also operate in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static.

Parallel data outputs are provided in 20-bit or 10-bit multiplexed format for HD and SD video rates. The associated Parallel Clock input signal operates at 148.5 or 148.5/1.001MHz (HD 10-bit multiplexed modes), 74.25 or 74.25/1.001MHz (for HD 20-bit mode), 27MHz (for SD 10-bit mode) and 13.5MHz (for SD 20-bit mode).

Up to eight channels, in two groups, of serial digital audio may be extracted from the video data stream, in accordance with SMPTE 272M and SMPTE 299M. The output signal formats supported by the device include AES/EBU and three other industry standard serial digital formats. 16, 20 and 24-bit audio formats are supported at 48kHz synchronous for SD modes and 48kHz synchronous or asynchronous in HD mode. Additional audio processing features include group selection, channel swapping, ECC error detection and correction (HD mode only), and audio channel status extraction. Audio clock and control signals provided by the device include Word Clock (fs), Serial Clock (64fs), and Audio Master Clock at user-selectable rates of 128fs, 256fs or 512fs.

Functional Block Diagram



GS1670 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
2	158468	–	September 2012	Changes throughout the document.
1	153472	–	January 2010	Converted to Data Sheet.
0	153078	–	November 2009	New Document. Added reference to GS1670/GS1671 Errata (document number 53878).

Contents

List of Figures

List of Tables

1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_ VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	A_VDD	PLL_ VDD	RSV	VCO_ GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	A_GND	PLL_ VDD	PLL_ VDD	STAT4	STAT5	$\overline{\text{RESET}}$ _TRST	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	A_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SW_EN	JTAG/ $\overline{\text{HOST}}$	IO_GND	IO_VDD
E	SDI_VDD	SDI_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SDOUT_ TDO	SDIN_ TDI	DOUT10	DOUT11
F	TERM	RSV	A_GND	PLL_ GND	CORE _GND	CORE _VDD	$\overline{\text{CS}}$_ TMS	SCLK_ TCK	DOUT8	DOUT9
G	RSV	RSV	$\overline{\text{RC\_BYP}}$	RSV	CORE _GND	CORE _VDD	$\overline{\text{SMPTE}}$_ $\overline{\text{BYPASS}}$	DVB_ASI	IO_GND	IO_VDD
H	BUFF_ VDD	BUFF_ GND	AUDIO_ EN/$\overline{\text{DIS}}$	WCLK	TIM_861	XTAL_ OUT	20bit/ 10bit	IOPROC_ EN/$\overline{\text{DIS}}$	DOUT6	DOUT7
J	SDO	SDO_ EN/$\overline{\text{DIS}}$	AOUT_1/2	ACLK	AOUT_5/6	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STANDBY	AOUT_3/4	AMCLK	AOUT_7/8	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1:Pin Descriptions

Pin Number	Name	Timing	Type	Description
A1	VBG		Analog Input	Band Gap voltage filter connection.
A2	LF		Analog Input	Loop Filter component connection.
A3	LB_CONT		Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD		Input Power	POWER pin for the VCO. Connect to a 1.2V±5% analog supply followed by a RC filter (see 5. Application Reference Design). A 105Ω 1% resistor must be used in the RC filter circuit. VCO_VDD is nominally 0.7V.

Table 1-1:Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A5, A6, B5, B6, C5, C6	STAT[0:5]		Output	MULTI-FUNCTIONAL OUTPUT PORT. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Each of the STAT [0:5] pins can be configured individually to output one of the following signals:
				Signal — Default H/HSYNC — STAT0 V/VSYNC — STAT1 F/DE — STAT2 LOCKED — STAT3 Y/1ANC — STAT4 C/2ANC — – $\overline{\text{DATA ERROR}}$ — STAT5 $\overline{\text{VIDEO ERROR}}$ — – $\overline{\text{AUDIO ERROR}}$ — – EDH DETECTED — – CARRIER DETECT — – RATE_DET — –
A7, D10, G10, K7	IO_VDD		Input Power	POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.
A8	PCLK		Output	PARALLEL DATA BUS CLOCK Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
				HD 10-bit mode — PCLK @ 148.5 or 148.5/1.001MHz HD 20-bit mode — PCLK @ 74.25 or 74.25/1.001MHz SD 10-bit mode — PCLK @ 27MHz SD 20-bit mode — PCLK @ 13.5MHz

Table 1-1:Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
A9, A10, B8, B9, B10,C8, C9, C10, E9, E10	DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11		Output	PARALLEL DATA BUS Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.	
				20-bit mode 20bit/$\overline{10bit}$ = HIGH	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Luma data output for SD and HD data rates. DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
				10-bit mode 20bit/$\overline{10bit}$ = LOW	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates. DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): 8b/10b decoded DVB-ASI data Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
B1	A_VDD		Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.	
B2, C3, C4	PLL_VDD		Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.	
B3, F2, G1, G2, G4	RSV			These pins must be left unconnected.	
B4	VCO_GND		Input Power	GND pin for the VCO. Connect to analog GND.	
B7, D9, G9, J7	IO_GND		Input Power	GND connection for digital I/O. Connect to digital GND.	
C1, D1	SDI, $\overline{SDI}$		Analog Input	Serial Digital Differential Input.	
C2, D2, D3, E3, F3	A_GND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.	
C7	$\overline{RESET\_TRST}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG/$\overline{HOST}$ = LOW): When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG/$\overline{HOST}$ = HIGH): When LOW, all functional blocks are set to default and the JTAG test sequence is reset. When HIGH, normal operation of the JTAG test sequence resumes after $\overline{RESET\_TRST}$ is de-asserted.	

Table 1-1:Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
D4, E4, F4	PLL_GND		Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G5	CORE_GND		Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD		Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	SW_EN		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable switch-line locking, as described in Section 4.9.1.
D8	JTAG/$\overline{\text{HOST}}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select JTAG test mode or host interface mode. When JTAG/$\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/$\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes.
E1	SDI_VDD		Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	SDI_GND		Input Power	GND pin for SDI buffer. Connect to analog GND.
E7	SDOUT_TDO		Output	COMMUNICATION SIGNAL OUTPUT Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. GSPI serial data output/test data out. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test results from the device. In host interface mode, this pin is used to read status and configuration data from the device. **Note:** GSPI is slightly different than the SPI. For more details on GSPI, please refer to 4.19 GSPI - HOST Interface.
E8	SDIN_TDI		Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. GSPI serial data in/test data in. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test data into the device. In host interface mode, this pin is used to write address and configuration data words into the device.
F1	TERM		Analog Input	Decoupling for internal SDI termination resistors.

Table 1-1:Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
F7	$\overline{CS}$_TMS		Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Chip select / test mode start. In JTAG mode (JTAG/$\overline{HOST}$ = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test. In host interface mode (JTAG/$\overline{HOST}$ = LOW), this pin operates as the host interface chip select and is active LOW.
F8	SCLK_TCK		Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Serial data clock signal. In JTAG mode (JTAG/$\overline{HOST}$ = HIGH), this pin is the JTAG clock. In host interface mode (JTAG/$\overline{HOST}$ = LOW), this pin is the host interface serial bit clock. All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.
F9, F10, H9, H10, J8, J9, J10, K8, K9, K10	DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3		Output	PARALLEL DATA BUS Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. 20-bit mode (20bit/$\overline{10bit}$ = HIGH): SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Chroma data output for SD and HD data rates. DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output 10-bit mode (20bit/$\overline{10bit}$ = LOW): Forced LOW
G3	$\overline{RC\_BYP}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.

Table 1-1:Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G7	$\overline{\text{SMPTE\_BYPASS}}$		Input/Output	CONTROL SIGNAL INPUT/OUTPUT Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Indicates the presence of valid SMPTE data. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{\text{SMPTE\_BYPASS}}$ is HIGH when the device locks to a SMPTE compliant input. $\overline{\text{SMPTE\_BYPASS}}$ is LOW under all other conditions. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is LOW, this pin is an INPUT: No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ is set HIGH, the device carries out SMPTE scrambling and I/O processing. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode.
G8	DVB_ASI		Input/Output	CONTROL SIGNAL INPUT Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable/disable DVB-ASI data extraction in manual mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is LOW, this pin is an input and when the DVB_ASI pin is set HIGH the device will carry out DVB_ASI data extraction and processing. The $\overline{\text{SMPTE\_BYPASS}}$ pin must be set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is HIGH (default), DVB-ASI is configured as a status output (set LOW), and DVB-ASI input streams are not supported or recognized.
H1	BUFF_VDD		Input Power	POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND		Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H3	AUDIO_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Enables or disables audio extraction.
H4	WCLK		Output	48kHz word clock for Audio.
H5	TIM_861		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select CEA-861 timing mode. When TIM_861 is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.
H6	XTAL_OUT		Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.

Table 1-1:Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H7	20bit/$\overline{10bit}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select the output bus width. HIGH = 20-bit, LOW = 10-bit.
H8	IOPROC_EN/$\overline{DIS}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable or disable audio and video processing features. When IOPROC_EN is HIGH, the audio and video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.
J1, K1	SDO, $\overline{SDO}$		Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN/$\overline{DIS}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable/disable the serial digital output stage. When SDO_EN/$\overline{DIS}$ is LOW, the serial digital output signals, SDO and $\overline{SDO}$, are both pulled HIGH. When SDO_EN/$\overline{DIS}$ is HIGH, the serial digital output signals, SDO and $\overline{SDO}$, are enabled.
J3	AOUT_1/2		Output	Serial Audio Output; Channels 1 and 2.
J4	ACLK		Output	64fs sample clock for audio.
J5	AOUT_5/6		Output	Serial Audio Output; Channels 5 and 6.
J6, K6	XTAL2, XTAL1		Analog Input	Input connection for 27MHz crystal.
K2	STANDBY		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and $\overline{SDO}$, are both pulled HIGH.
K3	AOUT_3/4		Output	Serial Audio Output; Channels 3 and 4.
K4	AMCLK		Output	Oversampled master clock for audio (128fs, 256fs, 512fs selectable).
K5	AOUT_7/8		Output	Serial Audio Output; Channels 7 and 8.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1:Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (SDI_VDD, BUFF_VDD, A_VDD)	-0.3V to +4.0V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Ambient Operating Temperature (T_A)	$-40°C \leq T_A \leq 95°C$
Storage Temperature (T_{STG})	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

NOTES:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2:Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	2
Supply Voltage, Serial Digital Input	SDI_VDD	–	3.13	3.3	3.47	V	2
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	2

NOTES

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor. See Typical Application Circuit on page 121.
2. The 3.3V supplies must track the 3.3V supply of an external EQ and external CD.

2.3 DC Electrical Characteristics

Table 2-3:DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10/20bit HD	–	175	215	mA	–
		10/20bit SD	–	145	180	mA	–
		DVB_ASI	–	135	165	mA	–
+1.8V Supply Current	I_{1V8}	10/20bit HD	–	20	21	mA	–
		10/20bit SD	–	6	7	mA	–
		DVB_ASI	–	6	7	mA	–
+3.3V Supply Current	I_{3V3}	10/20bit HD	–	65	75	mA	–
		10/20bit SD	–	35	45	mA	–
		DVB_ASI	–	35	45	mA	–
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10/20bit HD	–	300	360	mW	–
		10/20bit SD	–	235	305	mW	–
		DVB_ASI	–	235	305	mW	–
		Reset	–	200	–	mW	–
		Standby	–	16	44	mW	–
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10/20bit HD	–	430	530	mW	–
		10/20bit SD	–	290	370	mW	–
		DVB_ASI	–	290	370	mW	–
		Reset	–	220	–	mW	–
		Standby	–	16	44	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VSS -0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD +0.3	V	–
Output Logic LOW	V_{OL}	IOL = 5mA, 1.8V operation	–	–	0.2	V	–
		IOL = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOH = 5mA, 1.8V operation	1.4	–	–	V	–
		IOH = 8mA, 3.3V operation	2.4	–	–	V	–
Serial Input							
Serial Input Common Mode Voltage	–	50Ω load	2.5	SDI_VDD -(0.75/2)	SDI_VDD -(0.55/2)	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD -(0.6/2)	BUFF_VDD -(0.45/2)	BUFF_VDD -(0.35/2)	V	–

Table 2-3:DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes

Notes:

The output drive strength of the digital outputs can be programmed through the host interface. please see Table 4-28: Video Core Configuration and Status Registers, register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4:AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
System								
Device Latency: AUDIO_EN = 1, SMPTE mode, IOPROC_EN = 1	–	HD		79	–	83	PCLK	–
		SD		50	–	59	PCLK	–
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 1	–	HD		44	–	48	PCLK	–
		SD		44	–	48	PCLK	–
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 0	–	HD		33	–	36	PCLK	–
		SD		32	–	35	PCLK	–
Device Latency: AUDIO_EN = 0, SMPTE bypass, IOPROC_EN = 0	–	HD		6	–	9	PCLK	–
		SD		5	–	9	PCLK	–
Device Latency: DVB-ASI	–	SD		12	–	16	PCLK	–
Reset Pulse Width	t_{reset}	–		1	–	–	ms	–
Parallel Output								
Parallel Clock Frequency	f_{PCLK}	–		13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–		40	–	60	%	–
Output Data Hold Time (1.8V)	t_{oh}	HD 10-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		HD 20-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		SD 10-bit 6pF Cload	DBUS	19.4	–	–	ns	1
			STAT	19.4	–	–	ns	1
		SD 20-bit 6pF Cload	DBUS	38.0	–	–	ns	1
			STAT	38.0	–	–	ns	1

Table 2-4:AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Hold Time (3.3V)	t_{oh}	HD 10-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		HD 20-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		SD 10-bit 6pF Cload	DBUS	19.4	–	–	ns	2
			STAT	19.4	–	–	ns	2
		SD 20-bit 6pF Cload	DBUS	38.0	–	–	ns	2
			STAT	38.0	–	–	ns	2
Output Data Delay Time (1.8V)	t_{od}	HD 10-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		HD 20-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		SD 10-bit 15pF Cload	DBUS	–	–	22.2	ns	3
			STAT	–	–	22.2	ns	3
		SD 20-bit 15pF Cload	DBUS	–	–	41.0	ns	3
			STAT	–	–	41.0	ns	3
Output Data Delay Time (3.3V)	t_{od}	HD 10-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		HD 20-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		SD 10-bit 15pF Cload	DBUS	–	–	22.2	ns	4
			STAT	–	–	22.2	ns	4
		SD 20-bit 15pF Cload	DBUS	–	–	41.0	ns	4
			STAT	–	–	41.0	ns	4
Output Data Rise/Fall Time (1.8V)	t_r/t_f	All modes 6pF Cload	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.4	ns	1
			AUDIO	–	–	0.6	ns	1
		All modes 15pF Cload	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.4	ns	3
			AUDIO	–	–	2.3	ns	3

Table 2-4:AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Rise/Fall Time (3.3V)	t_r/t_f	All modes 6pF Cload	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
			AUDIO	–	–	0.6	ns	2
		All modes 15pF Cload	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.4	ns	4
			AUDIO	–	–	2.2	ns	4
Serial Digital Input								
Serial Input Data Rate	DR_{SDI}	–		0.27	–	1.485	Gb/s	–
Serial Input Swing	ΔV_{SDI}	Differential with 100Ω load		500	800	1100	mVp-p	–
Serial Input Jitter Tolerance	IJT	Nominal loop bandwidth	Square wave mod.	0.7	0.8	–	UI	–
Serial Digital Output								
Serial Output Data Rate	DR_{SDO}	–		0.27	–	1.485	Gb/s	–
Serial Output Swing	ΔV_{SDO}	Differential with 100Ω load		350	–	600	mVp-p	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	–		–	–	180	ps	–
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	–		–	–	180	ps	–
Serial Output Intrinsic Jitter	t_{OJ}	SMPTE colour bar HD signal		–	–	100	ps	–
		SMPTE colour bar SD signal		–	–	400	ps	–
Serial Output Duty Cycle Distortion	DCD_{SDD}	HD		–	10	–	ps	–
		SD		–	20	–	ps	–
Synchronous lock time	–	–		–	–	25	µs	–
Asynchronous lock time	–	–		100	–	350	µs	–
Lock time from power-up	–	After 20 minutes at -20°C		–	–		ms	–

Table 2-4:AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	60	MHz	5
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	5
GSPI Input Data Setup Time	–		1.5	–	–	ns	5
GSPI Input Data Hold Time	–		1.5	–	–	ns	5
GSPI Output Data Hold Time	–	–	1.5	–	–	ns	5
$\overline{CS}$ low before SCLK rising edge	–	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	5
$\overline{CS}$ high after SCLK falling edge	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	5

Notes:

1. 1.89V and 0°C.
2. 3.47V and 0°C.
3. 1.71V and 85°C
4. 3.13V and 85°C
5. Timing parameters defined in Section 4.19.3

3. Input/Output Circuits

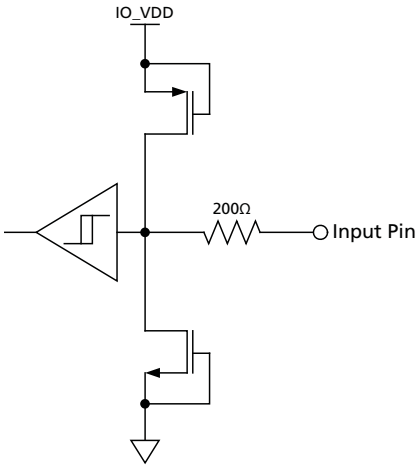


Figure 3-1: Digital Input Pin with Schmitt Trigger (20bit/$\overline{10bit}$, AUDIO_EN/$\overline{DIS}$, $\overline{CS}$_TMS, SW_EN, IOPROC_EN/$\overline{DIS}$, JTAG/$\overline{HOST}$, $\overline{RC\_BYP}$, $\overline{RESET\_TRST}$, SCLK_TCK, SDIN_TDI, SDO_EN/$\overline{DIS}$, STANDBY, TIM_861)

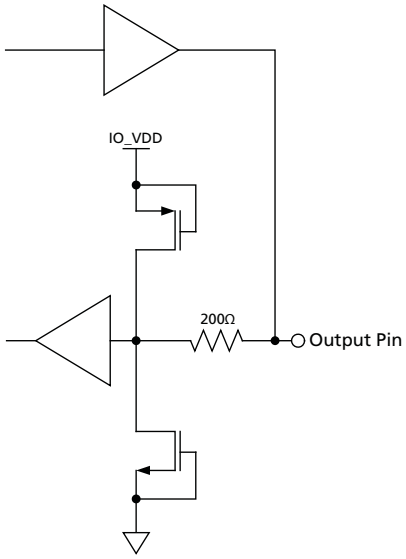


Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (ACLK, AMCLK, AOUT_1/2, AOUT_3/4, AOUT_5/6, AOUT_7/8, DVB_ASI, $\overline{SMPTE\_BYPASS}$, WCLK)

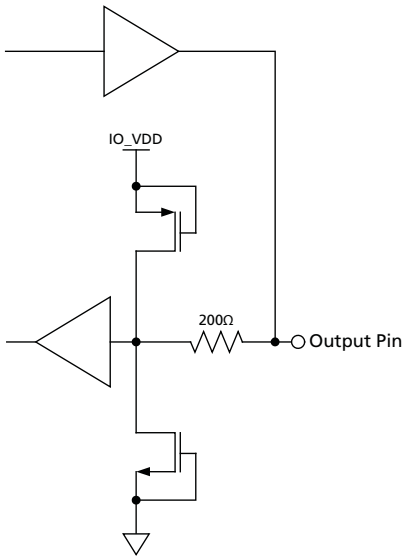


Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output unless in Reset Mode; in which case they are high-impedance. The drive strength can be set by writing to address 06Dh in the host interface register. (DOUT0, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, DOUT6, DOUT7, DOUT8, DOUT9, SDOUT_TDO, STAT0, STAT1, STAT2, STAT3, STAT4, STAT5, XTAL_OUT, DOUT10, DOUT11, DOUT12, DOUT13, DOUT14, DOUT15, DOUT16, DOUT17, DOUT18, DOUT19, PCLK)

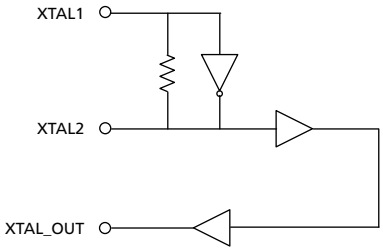


Figure 3-4: XTAL1/XTAL2/XTAL-OUT

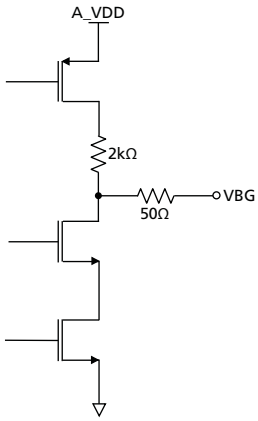


Figure 3-5: VBG

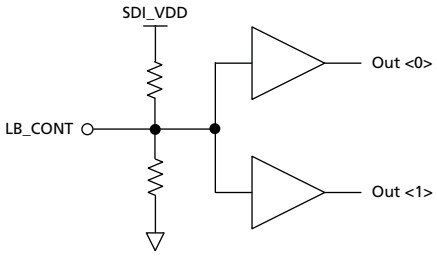


Figure 3-6: LB_CONT

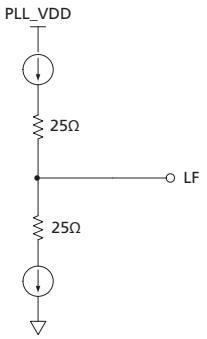


Figure 3-7: Loop Filter

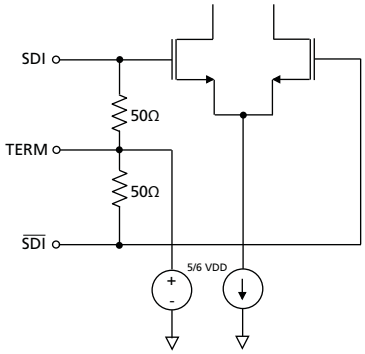


Figure 3-8: SDI/$\overline{\text{SDI}}$ and TERM

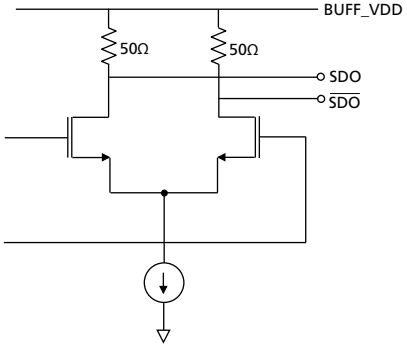


Figure 3-9: SDO/$\overline{\text{SDO}}$

4. Detailed Description

Refer to the document entitled **GS1670/GS1671 Errata** for this device (document number **53878**).

4.1 Functional Overview

The GS1670 is a multi-rate, multi-standard receiver with integrated SMPTE video processing as well as an integrated audio de-embedder, compliant with SMPTE 292 and SMPTE 259M-C signals.

The GS1670 includes an integrated reclocker, serial data loop through output, robust serial-to-parallel conversion, integrated SMPTE video processing, and additional processing functions such as audio extraction, ancillary data extraction, EDH support, and DVB-ASI decoding.

The device supports four distinct modes of operation that can be set through external device pins or by programming internal registers through the host interface; SMPTE mode, Data-Through mode, DVB-ASI mode and Standby mode.

In SMPTE mode, all video processing features, ancillary data extraction, and audio de-embedding features are enabled by default.

In DVB-ASI mode, the GS1670 carries out 8b/10b decoding and generates 10-bit parallel DVB-ASI compliant data.

In Data-Through mode, the device operates as a simple serial to parallel converter. No additional processing features are enabled.

Standby mode is the low power consumption mode of the device. In this mode, the internal reclocker will unlock, and the internal configuration registers will not be accessible through the host interface.

The GS1670 includes a JTAG interface for boundary scan testing.

4.2 Serial Digital Input

The GS1670 can accept serial digital inputs compliant with SMPTE 292 and SMPTE 259M-C. The serial digital input buffer features 50Ω input termination and can be DC-coupled to Gennum's SD/HD-capable equalizers.

4.3 Serial Digital Loop-Through Output

The GS1670 contains a 100Ω differential serial output buffer which can be configured to output either a retimed or a buffered version of the serial digital input. The SDO and $\overline{\text{SDO}}$ outputs of this buffer can interface directly to a SD/HD-capable, SMPTE compliant Gennum cable driver. See 5.1 Typical Application Circuit on page 121.

When the $\overline{\text{RC\_BYP}}$ pin is set HIGH, the serial digital output is the re-timed version of the serial input.