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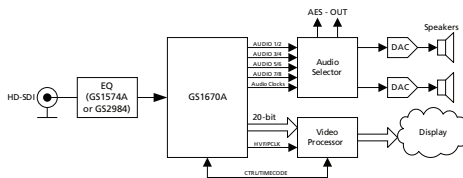
## HD/SD SDI Receiver Complete with SMPTE Audio and Video Processing

### Key Features

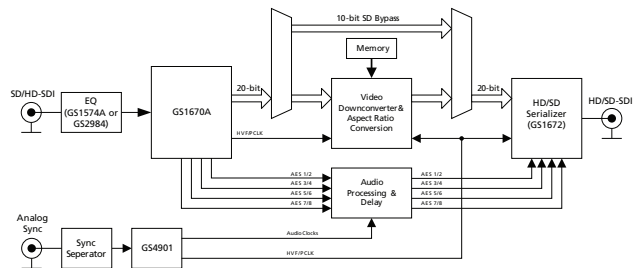
- Operation at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE ST 292, SMPTE ST 259-C and DVB-ASI
- Integrated Reclocker with low phase noise, integrated VCO
- Serial digital reclocked, or non-reclocked loop-through output
- Integrated audio de-embedder for 8 channels of 48kHz audio
- Integrated audio clock generator
- Ancillary data extraction
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 timing signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI host interface
- Wide temperature range of -40°C to +85°C
- Low power operation (typically 300mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

### Applications

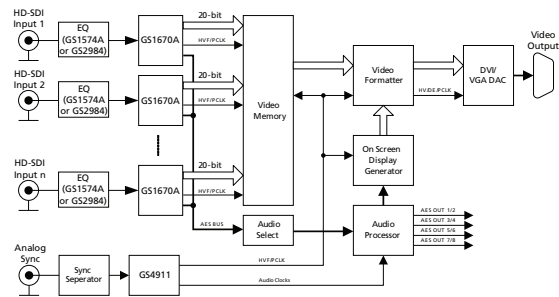
Application: 1080p30 or 720p60 Monitor



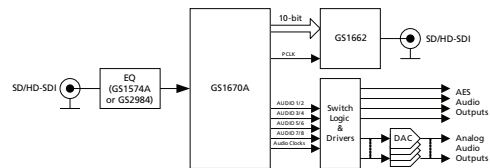
Application: Multi-format Downconverter



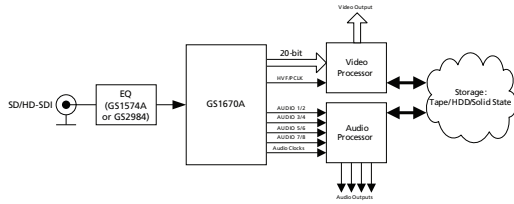
Application: Multi-input Video Monitoring System



Application: Multi-format Audio De-embedder Module



Application: Multi-format Digital VTR/Video Server



## Description

The GS1670A is a multi-rate SDI Receiver which includes complete SMPTE processing, as per SMPTE ST 292 and SMPTE ST 259-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop-through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The serial digital output can be connected to an external cable driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode, the GS1670A performs SMPTE de-scrambling and NRZI to NRZ decoding and word alignment. Line-based CRC errors, line number errors, TRS errors and ancillary data check sum errors can all be detected. The GS1670A also provides ancillary data extraction. The entire ancillary data packet is extracted, and written to host-accessible registers. Other processing functions include H:V:F timing extraction, Luma and Chroma ancillary data indication, video standard detection, and SMPTE ST 352 packet detection and decoding. All of the processing features are optional, and may be enabled or disabled via the Host Interface.

In DVB-ASI mode, 8b/10b decoding is applied to the received data stream.

In Data-Through mode all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

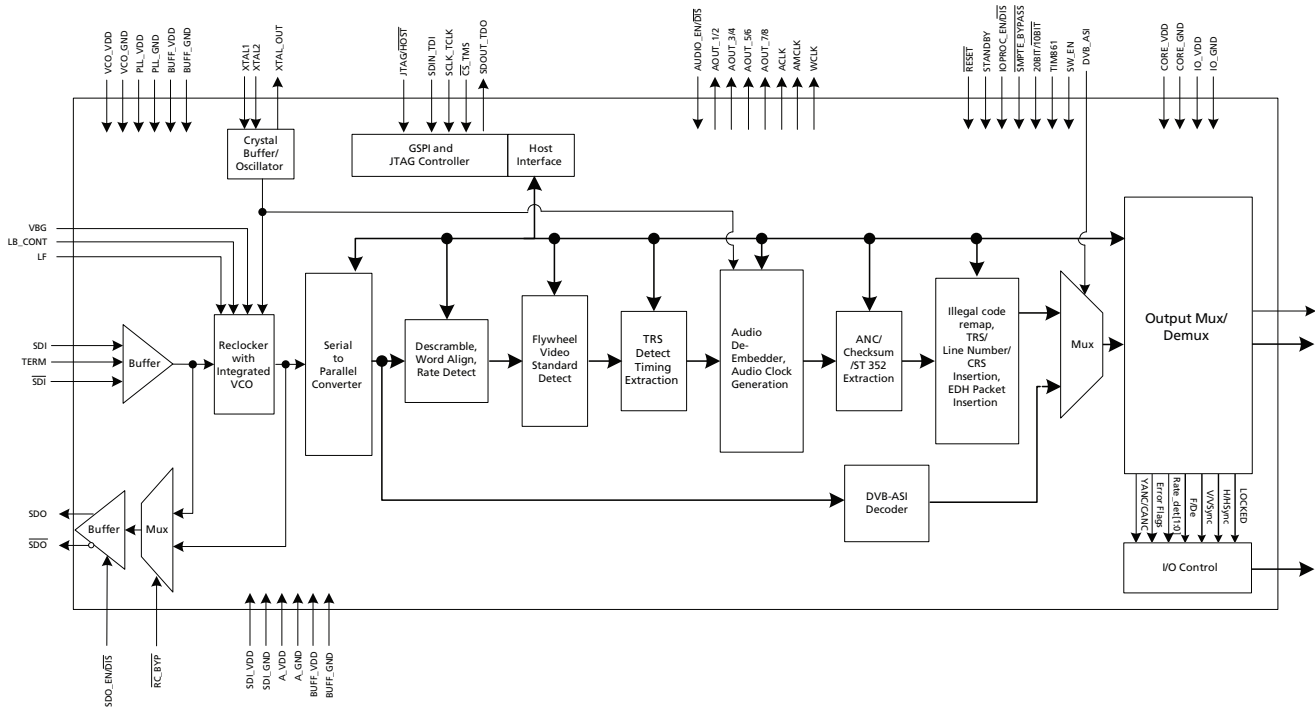
The device can also operate in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static.

Parallel data outputs are provided in 20-bit or 10-bit multiplexed format for HD and SD video rates. The associated Parallel Clock input signal operates at 148.5 or 148.5/1.001MHz (HD 10-bit multiplexed modes), 74.25 or 74.25/1.001MHz (for HD 20-bit mode), 27MHz (for SD 10-bit mode) and 13.5MHz (for SD 20-bit mode).

Up to eight channels, in two groups, of serial digital audio may be extracted from the video data stream, in accordance with SMPTE ST 272 and SMPTE ST 299. The output signal formats supported by the device include AES/EBU and three other industry standard serial digital formats. 16, 20 and 24-bit audio formats are supported at 48kHz synchronous for SD modes and 48kHz synchronous or asynchronous in HD mode. Additional audio processing features include group selection, channel swapping, ECC error detection and correction (HD mode only), and audio channel status extraction. Audio clock and control signals provided by the device include Word Clock (fs), Serial Clock (64fs), and Audio Master Clock at user-selectable rates of 128fs, 256fs or 512fs.



# Functional Block Diagram



GS1670A Functional Block Diagram

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# 1. Pin Out

## 1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	A_VDD	PLL_VDD	RSV	VCO_GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	A_GND	PLL_VDD	PLL_VDD	STAT4	STAT5	$\overline{\text{RESET\_TRST}}$	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	A_GND	A_GND	PLL_GND	CORE_GND	CORE_VDD	SW_EN	JTAG/HOST	IO_GND	IO_VDD
E	SDI_VDD	SDI_GND	A_GND	PLL_GND	CORE_GND	CORE_VDD	SDOUT_TDO	SDIN_TDI	DOUT10	DOUT11
F	TERM	RSV	A_GND	PLL_GND	CORE_GND	CORE_VDD	$\overline{\text{CS\_TMS}}$	SCLK_TCK	DOUT8	DOUT9
G	RSV	RSV	$\overline{\text{RC\_BYP}}$	RSV	CORE_GND	CORE_VDD	$\overline{\text{SMPTE\_BYPASS}}$	DVB_ASI	IO_GND	IO_VDD
H	BUFF_VDD	BUFF_GND	AUDIO_EN/DIS	WCLK	TIM_861	XTAL_OUT	20bit/10bit	IOPROC_EN/DIS	DOUT6	DOUT7
J	SDO	$\overline{\text{SDO\_EN/DIS}}$	AOUT_1/2	ACLK	AOUT_5/6	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STANDBY	AOUT_3/4	AMCLK	AOUT_7/8	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

## 1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
A1	VBG	Analog Input	Band Gap voltage filter connection.
A2	LF	Analog Input	Loop Filter component connection.
A3	LB_CONT	Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD	Input Power	POWER pin for the VCO. Connect to a 1.2V±5% analog supply followed by a RC filter (see 5.1 Typical Application Circuit). A 105Ω 1% resistor must be used in the RC filter circuit. VCO_VDD is nominally 0.7V.

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Type	Description	
A5, A6, B5, B6, C5, C6	STAT[0:5]	Output	MULTI-FUNCTIONAL OUTPUT PORT. Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility. Each of the STAT[0:5] pins can be configured individually to output one of the following signals:	
			Signal	Default
			H/HSYNC	STAT0
			V/VSYNC	STAT1
			F/DE	STAT2
			LOCKED	STAT3
			Y/1ANC	STAT4
			C/2ANC	–
			<u>DATA ERROR</u>	STAT5
			<u>VIDEO ERROR</u>	–
			<u>AUDIO ERROR</u>	–
			EDH DETECTED	–
CARRIER DETECT	–			
RATE_DET	–			
A7, D10, G10, K7	IO_VDD	Input Power	POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.	
A8	PCLK	Output	PARALLEL DATA BUS CLOCK Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.	
			HD 10-bit mode	PCLK @ 148.5 or 148.5/1.001MHz
			HD 20-bit mode	PCLK @ 74.25 or 74.25/1.001MHz
			SD 10-bit mode	PCLK @ 27MHz
			SD 20-bit mode	PCLK @ 13.5MHz

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Type	Description
			<p>PARALLEL DATA BUS</p> <p>Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p>
A9, A10, B8, B9, B10, C8, C9, C10, E9, E10	DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11	Output	<p>SMPTE mode (<math>\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}</math> and <math>\text{DVB\_ASI} = \text{LOW}</math>): Luma data output for SD and HD data rates.</p>
			<p>20-bit mode <math>20\text{bit}/10\text{bit} = \text{HIGH}</math></p> <p>DVB-ASI mode (<math>\overline{\text{SMPTE\_BYPASS}} = \text{LOW}</math> and <math>\text{DVB\_ASI} = \text{HIGH}</math>): Not defined</p> <p>Data-Through mode (<math>\overline{\text{SMPTE\_BYPASS}} = \text{LOW}</math> and <math>\text{DVB\_ASI} = \text{LOW}</math>): Data output</p>
			<p>10-bit mode <math>20\text{bit}/10\text{bit} = \text{LOW}</math></p> <p>SMPTE mode (<math>\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}</math> and <math>\text{DVB\_ASI} = \text{LOW}</math>): Multiplexed Luma/Chroma data output for SD and HD data rates.</p> <p>DVB-ASI mode (<math>\overline{\text{SMPTE\_BYPASS}} = \text{LOW}</math> and <math>\text{DVB\_ASI} = \text{HIGH}</math>): 8b/10b decoded DVB-ASI data</p> <p>Data-Through mode (<math>\overline{\text{SMPTE\_BYPASS}} = \text{LOW}</math> and <math>\text{DVB\_ASI} = \text{LOW}</math>): Data output</p>
B1	A_VDD	Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.
B2, C3, C4	PLL_VDD	Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.
B3, F2, G1, G2, G4	RSV		These pins must be left unconnected.
B4	VCO_GND	Input Power	GND pin for the VCO. Connect to analog GND.
B7, D9, G9, J7	IO_GND	Input Power	GND connection for digital I/O. Connect to digital GND.
C1, D1	SDI, $\overline{\text{SDI}}$	Analog Input	Serial Digital Differential Input.
C2, D2, D3, E3, F3	A_GND	Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
			<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to reset the internal operating conditions to default settings and to reset the JTAG sequence.</p> <p>Normal mode (<math>\text{JTAG}/\overline{\text{HOST}} = \text{LOW}</math>):</p> <p>When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance.</p> <p>When HIGH, normal operation of the device resumes.</p> <p>JTAG test mode (<math>\text{JTAG}/\overline{\text{HOST}} = \text{HIGH}</math>):</p> <p>When LOW, all functional blocks are set to default and the JTAG test sequence is reset.</p> <p>When HIGH, normal operation of the JTAG test sequence resumes after <math>\overline{\text{RESET\_TRST}}</math> is de-asserted.</p>
C7	$\overline{\text{RESET\_TRST}}$	Input	

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Type	Description
D4, E4, F4	PLL_GND	Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G5	CORE_GND	Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD	Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	SW_EN	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility. Used to enable switch-line locking, as described in <a href="#">Section 4.9.1</a> .
D8	JTAG/ $\overline{\text{HOST}}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility. Used to select JTAG test mode or host interface mode. When JTAG/ $\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/ $\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes.
E1	SDI_VDD	Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	SDI_GND	Input Power	GND pin for SDI buffer. Connect to analog GND.
E7	SDOUT_TDO	Output	COMMUNICATION SIGNAL OUTPUT Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility. GSPI serial data output/test data out. In JTAG mode (JTAG/ $\overline{\text{HOST}}$ = HIGH), this pin is used to shift test results from the device. In host interface mode, this pin is used to read status and configuration data from the device. <b>Note:</b> GSPI is slightly different than the SPI. For more details on GSPI, please refer to <a href="#">4.19 GSPI - HOST Interface</a> .
E8	SDIN_TDI	Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility. GSPI serial data in/test data in. In JTAG mode (JTAG/ $\overline{\text{HOST}}$ = HIGH), this pin is used to shift test data into the device. In host interface mode, this pin is used to write address and configuration data words into the device.
F1	TERM	Analog Input	Decoupling for internal SDI termination resistors.

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Type	Description
F7	$\overline{\text{CS\_TMS}}$	Input	<p>COMMUNICATION SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Chip select / test mode start.</p> <p>In JTAG mode (<math>\text{JTAG}/\overline{\text{HOST}} = \text{HIGH}</math>), this pin is Test Mode Start, used to control the operation of the JTAG test.</p> <p>In host interface mode (<math>\text{JTAG}/\overline{\text{HOST}} = \text{LOW}</math>), this pin operates as the host interface chip select and is active LOW.</p>
F8	SCLK_TCK	Input	<p>COMMUNICATION SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Serial data clock signal.</p> <p>In JTAG mode (<math>\text{JTAG}/\overline{\text{HOST}} = \text{HIGH}</math>), this pin is the JTAG clock.</p> <p>In host interface mode (<math>\text{JTAG}/\overline{\text{HOST}} = \text{LOW}</math>), this pin is the host interface serial bit clock.</p> <p>All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.</p>
F9, F10, H9, H10, J8, J9, J10, K8, K9, K10	DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3	Output	<p>PARALLEL DATA BUS</p> <p>Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <hr/> <p>SMPTE mode (<math>\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}</math> and <math>\text{DVB\_ASI} = \text{LOW}</math>): Chroma data output for SD and HD data rates.</p> <p>DVB-ASI mode (<math>\overline{\text{SMPTE\_BYPASS}} = \text{LOW}</math> and <math>\text{DVB\_ASI} = \text{HIGH}</math>): Not defined</p> <p>Data-Through mode (<math>\overline{\text{SMPTE\_BYPASS}} = \text{LOW}</math> and <math>\text{DVB\_ASI} = \text{LOW}</math>): Data output</p> <hr/> <p>10-bit mode <math>20\text{bit}/\overline{10\text{bit}} = \text{LOW}</math></p> <p>Forced LOW</p>
G3	$\overline{\text{RC\_BYP}}$	Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.</p>



**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Type	Description
G7	$\overline{\text{SMPTE\_BYPASS}}$	Input/Output	<p>CONTROL SIGNAL INPUT/OUTPUT</p> <p>Please refer to the Input/Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Indicates the presence of valid SMPTE data.</p> <p>When the <math>\overline{\text{AUTO/MAN}}</math> bit in the host interface register is HIGH (Default), this pin is an OUTPUT. <math>\overline{\text{SMPTE\_BYPASS}}</math> is HIGH when the device locks to a SMPTE compliant input. <math>\overline{\text{SMPTE\_BYPASS}}</math> is LOW under all other conditions.</p> <p>When the <math>\overline{\text{AUTO/MAN}}</math> bit in the host interface register is LOW, this pin is an INPUT:</p> <p>No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when <math>\overline{\text{SMPTE\_BYPASS}}</math> is set LOW.</p> <p>When <math>\overline{\text{SMPTE\_BYPASS}}</math> is set HIGH, the device carries out SMPTE scrambling and I/O processing.</p> <p>When <math>\overline{\text{SMPTE\_BYPASS}}</math> and <math>\overline{\text{DVB\_ASI}}</math> are both set LOW, the device operates in Data-Through mode.</p>
G8	DVB_ASI	Input/Output	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input/Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to enable/disable DVB-ASI data extraction in manual mode.</p> <p>When the <math>\overline{\text{AUTO/MAN}}</math> bit in the host interface is LOW, this pin is an input and when the DVB_ASI pin is set HIGH the device will carry out DVB_ASI data extraction and processing. The <math>\overline{\text{SMPTE\_BYPASS}}</math> pin must be set LOW. When <math>\overline{\text{SMPTE\_BYPASS}}</math> and DVB_ASI are both set LOW, the device operates in Data-Through mode.</p> <p>When the <math>\overline{\text{AUTO/MAN}}</math> bit in the host interface is HIGH (default), DVB-ASI is configured as a status output (set LOW), and DVB-ASI input streams are not supported or recognized.</p>
H1	BUFF_VDD	Input Power	POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND	Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H3	AUDIO_EN/ $\overline{\text{DIS}}$	Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Enables or disables audio extraction.</p>
H4	WCLK	Output	<p>48kHz word clock for Audio.</p> <p>Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p>
H5	TIM_861	Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to select CEA-861 timing mode.</p> <p>When TIM_861 is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.</p>
H6	XTAL_OUT	Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Type	Description
H7	20bit/10bit	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility. Used to select the output bus width. HIGH = 20-bit, LOW = 10-bit.
H8	IOPROC_EN/DIS	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility. Used to enable or disable audio and video processing features. When IOPROC_EN is HIGH, the audio and video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.
J1, K1	SDO, SDO	Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN/DIS	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility. Used to enable/disable the serial digital output stage. When SDO_EN/DIS is LOW, the serial digital output signals, SDO and SDO, are both pulled HIGH. When SDO_EN/DIS is HIGH, the serial digital output signals, SDO and SDO, are enabled.
J3	AOUT_1/2	Output	Serial Audio Output; Channels 1 and 2. Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.
J4	ACLK	Output	64fs sample clock for audio. Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.
J5	AOUT_5/6	Output	Serial Audio Output; Channels 5 and 6. Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.
J6, K6	XTAL2, XTAL1	Analog Input	Input connection for 27MHz crystal.
K2	STANDBY	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and SDO, are both pulled HIGH.
K3	AOUT_3/4	Output	Serial Audio Output; Channels 3 and 4. Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Type	Description
K4	AMCLK	Output	Oversampled master clock for audio (128fs, 256fs, 512fs selectable). Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.
K5	AOUT_7/8	Output	Serial Audio Output; Channels 7 and 8. Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.

## 2. Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (SDI_VDD, BUFF_VDD, A_VDD)	-0.3V to +4.0V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Operating Temperature Range	-20°C to +85°C
Functional Temperature Range	-40°C to +85°C
Storage Temperature Range	-50°C to +125°C
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

**Note:**

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

### 2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

T<sub>A</sub> = -20°C to + 85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	1
Supply Voltage, Serial Digital Input	SDI_VDD	–	3.13	3.3	3.47	V	1
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	1

**Note:**

1. The 3.3V supplies must track the 3.3V supply of an external EQ and external CD.

## 2.3 DC Electrical Characteristics

**Table 2-3: DC Electrical Characteristics**

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>System</b>						
+1.2V Supply Current	I <sub>1V2</sub>	10/20bit HD	–	175	215	mA
		10/20bit SD	–	145	180	mA
		DVB_ASI	–	135	165	mA
+1.8V Supply Current	I <sub>1V8</sub>	10/20bit HD	–	20	21	mA
		10/20bit SD	–	6	7	mA
		DVB_ASI	–	6	7	mA
+3.3V Supply Current	I <sub>3V3</sub>	10/20bit HD	–	65	75	mA
		10/20bit SD	–	35	45	mA
		DVB_ASI	–	35	45	mA
Total Device Power (IO_VDD = 1.8V)	P <sub>1D8</sub>	10/20bit HD	–	300	360	mW
		10/20bit SD	–	235	305	mW
		DVB_ASI	–	235	305	mW
		Reset	–	200	–	mW
		Standby	–	16	44	mW
Total Device Power (IO_VDD = 3.3V)	P <sub>3D3</sub>	10/20bit HD	–	430	530	mW
		10/20bit SD	–	290	370	mW
		DVB_ASI	–	290	370	mW
		Reset	–	220	–	mW
		Standby	–	16	44	mW
<b>Digital I/O</b>						
Input Logic LOW	V <sub>IL</sub>	3.3V or 1.8V operation	IO_VSS -0.3	–	0.3 x IO_VDD	V
Input Logic HIGH	V <sub>IH</sub>	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD +0.3	V
Output Logic LOW	V <sub>OL</sub>	IOL = 5mA, 1.8V operation	–	–	0.2	V
		IOL = 8mA, 3.3V operation	–	–	0.4	V
Output Logic HIGH	V <sub>OH</sub>	IOH = 5mA, 1.8V operation	1.4	–	–	V
		IOH = 8mA, 3.3V operation	2.4	–	–	V
<b>Serial Input</b>						
Serial Input Common Mode Voltage	–	50Ω load	2.5	SDI_VDD -(0.75/2)	SDI_VDD -(0.55/2)	V
<b>Serial Output</b>						
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD -(0.6/2)	BUFF_VDD -(0.45/2)	BUFF_VDD -(0.35/2)	V

**Note:**

The output drive strength of the digital outputs can be programmed through the host interface. please see [Table 4-28: Video Core Configuration and Status Registers](#), register 06Dh for details.



## 2.4 AC Electrical Characteristics

**Table 2-4: AC Electrical Characteristics**

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
<b>System</b>								
Device Latency: AUDIO_EN = 1, SMPTE mode, IOPROC_EN = 1	-	HD	79	-	83	PCLK	-	
		SD	50	-	59	PCLK	-	
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 1	-	HD	44	-	48	PCLK	-	
		SD	44	-	48	PCLK	-	
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 0	-	HD	33	-	36	PCLK	-	
		SD	32	-	35	PCLK	-	
Device Latency: AUDIO_EN = 0, SMPTE bypass, IOPROC_EN = 0	-	HD	6	-	9	PCLK	-	
		SD	5	-	9	PCLK	-	
Device Latency: DVB-ASI	-	SD	12	-	16	PCLK	-	
Reset Pulse Width	t <sub>reset</sub>	-	1	-	-	ms	-	
<b>Parallel Output</b>								
Parallel Clock Frequency	f <sub>PCLK</sub>	-	13.5	-	148.5	MHz	-	
Parallel Clock Duty Cycle	DC <sub>PCLK</sub>	-	40	-	60	%	-	
Output Data Hold Time (1.8V)	t <sub>oh</sub>	HD 10-bit 6pF C <sub>LOAD</sub>	DBUS	1.0	-	-	ns	1
			STAT	1.0	-	-	ns	1
		HD 20-bit 6pF C <sub>LOAD</sub>	DBUS	1.0	-	-	ns	1
			STAT	1.0	-	-	ns	1
		SD 10-bit 6pF C <sub>LOAD</sub>	DBUS	19.4	-	-	ns	1
			STAT	19.4	-	-	ns	1
		SD 20-bit 6pF C <sub>LOAD</sub>	DBUS	38.0	-	-	ns	1
			STAT	38.0	-	-	ns	1

**Table 2-4: AC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes			
Output Data Hold Time (3.3V)	$t_{oh}$	HD 10-bit 6pF $C_{LOAD}$	DBUS	1.0	–	–	ns	2		
			STAT	1.0	–	–	ns	2		
		HD 20-bit 6pF $C_{LOAD}$	DBUS	1.0	–	–	ns	2		
			STAT	1.0	–	–	ns	2		
		SD 10-bit 6pF $C_{LOAD}$	DBUS	19.4	–	–	ns	2		
			STAT	19.4	–	–	ns	2		
		SD 20-bit 6pF $C_{LOAD}$	DBUS	38.0	–	–	ns	2		
			STAT	38.0	–	–	ns	2		
		Output Data Delay Time (1.8V)	$t_{od}$	HD 10-bit 15pF $C_{LOAD}$	DBUS	–	–	3.7	ns	3
					STAT	–	–	4.4	ns	3
HD 20-bit 15pF $C_{LOAD}$	DBUS			–	–	3.7	ns	3		
	STAT			–	–	4.4	ns	3		
SD 10-bit 15pF $C_{LOAD}$	DBUS			–	–	22.2	ns	3		
	STAT			–	–	22.2	ns	3		
SD 20-bit 15pF $C_{LOAD}$	DBUS			–	–	41.0	ns	3		
	STAT			–	–	41.0	ns	3		
Output Data Delay Time (3.3V)	$t_{od}$			HD 10-bit 15pF $C_{LOAD}$	DBUS	–	–	3.7	ns	4
					STAT	–	–	4.1	ns	4
		HD 20-bit 15pF $C_{LOAD}$	DBUS	–	–	3.7	ns	4		
			STAT	–	–	4.1	ns	4		
		SD 10-bit 15pF $C_{LOAD}$	DBUS	–	–	22.2	ns	4		
			STAT	–	–	22.2	ns	4		
		SD 20-bit 15pF $C_{LOAD}$	DBUS	–	–	41.0	ns	4		
			STAT	–	–	41.0	ns	4		
		Output Data Rise/Fall Time (1.8V)	$t_r/t_f$	All modes 6pF $C_{LOAD}$	STAT	–	–	0.4	ns	1
					DBUS	–	–	0.4	ns	1
AUDIO	–				–	0.6	ns	1		
All modes 15pF $C_{LOAD}$	STAT			–	–	1.5	ns	3		
	DBUS			–	–	1.4	ns	3		
	AUDIO			–	–	2.3	ns	3		

**Table 2-4: AC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
Output Data Rise/Fall Time (3.3V)	$t_r/t_f$	All modes 6pF $C_{LOAD}$	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
			AUDIO	–	–	0.6	ns	2
		All modes 15pF $C_{LOAD}$	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.4	ns	4
			AUDIO	–	–	2.2	ns	4
<b>Serial Digital Input</b>								
Serial Input Data Rate	$DR_{SDI}$	–	0.27	–	1.485	Gb/s	–	
Serial Input Swing	$\Delta V_{SDI}$	Differential with 100 $\Omega$ load	500	800	1100	mVp-p	–	
Serial Input Jitter Tolerance	IJT	Nominal loop bandwidth	Square wave mod.	0.7	0.8	–	UI	–
<b>Serial Digital Output</b>								
Serial Output Data Rate	$DR_{SDO}$	–	0.27	–	1.485	Gb/s	–	
Serial Output Swing	$\Delta V_{SDO}$	Differential with 100 $\Omega$ load	350	–	600	mVp-p	–	
Serial Output Rise Time 20% ~ 80%	$tr_{SDO}$	–	–	–	180	ps	–	
Serial Output Fall Time 20% ~ 80%	$tf_{SDO}$	–	–	–	180	ps	–	
Serial Output Intrinsic Jitter	$t_{OJ}$	SMPTE colour bar HD signal	–	–	100	ps	–	
		SMPTE colour bar SD signal	–	–	400	ps	–	
Serial Output Duty Cycle Distortion	$DCD_{SDD}$	HD	–	10	–	ps	–	
		SD	–	20	–	ps	–	
Synchronous lock time	–	–	–	–	25	$\mu$ s	–	

**Table 2-4: AC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Asynchronous lock time	–	Manual mode, noise immunity disabled	100	–	350	μs	5
		Auto mode, noise immunity disabled	100	–	600	μs	5
		Noise immunity enabled	100	–	1200	μs	5
Lock time from power-up	–	After 20 minutes at -20°C	–	325		ms	5
<b>GSPI</b>							
GSPI Input Clock Frequency	$f_{SCLK}$		–	–	60	MHz	5
GSPI Input Clock Duty Cycle	$DC_{SCLK}$		40	50	60	%	5
GSPI Input Data Setup Time	–		1.5	–	–	ns	5
GSPI Input Data Hold Time	–		1.5	–	–	ns	5
GSPI Output Data Hold Time	–		1.5	–	–	ns	5
$\overline{CS}$ low before SCLK rising edge	–		1.5	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–		148.4	–	–	ns	5
$\overline{CS}$ high after SCLK falling edge	–		37.1	–	–	ns	5

**Notes:**

1. 1.89V and 0°C.
2. 3.47V and 0°C.
3. 1.71V and 85°C
4. 3.13V and 85°C
5. Timing parameters defined in [Section 4.19.3](#)

### 3. Input/Output Circuits

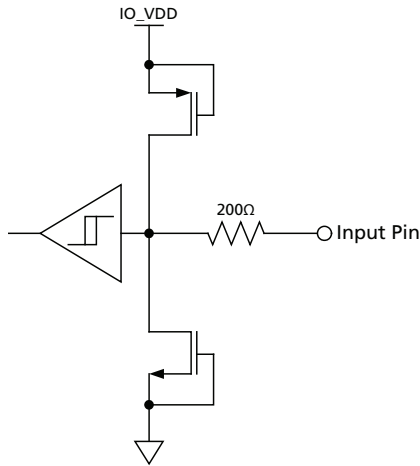


Figure 3-1: Digital Input Pin with Schmitt Trigger (20bit/ $\overline{10}$ bit,  $\overline{\text{AUDIO\_EN/DIS}}$ ,  $\overline{\text{CS\_TMS}}$ ,  $\overline{\text{SW\_EN}}$ ,  $\overline{\text{IOPROC\_EN/DIS}}$ ,  $\overline{\text{JTAG/HOST}}$ ,  $\overline{\text{RC\_BYP}}$ ,  $\overline{\text{RESET\_TRST}}$ ,  $\overline{\text{SCLK\_TCK}}$ ,  $\overline{\text{SDIN\_TDI}}$ ,  $\overline{\text{SDO\_EN/DIS}}$ ,  $\overline{\text{STANDBY}}$ ,  $\overline{\text{TIM\_861}}$ )

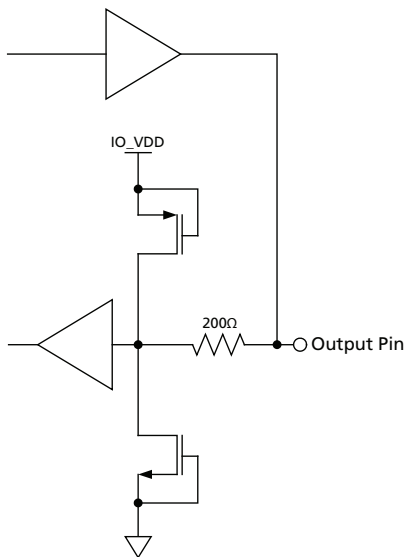


Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (ACLK, AMCLK, AOUT\_1/2, AOUT\_3/4, AOUT\_5/6, AOUT\_7/8, DVB\_ASI,  $\overline{\text{SMPTE\_BYPASS}}$ , WCLK)



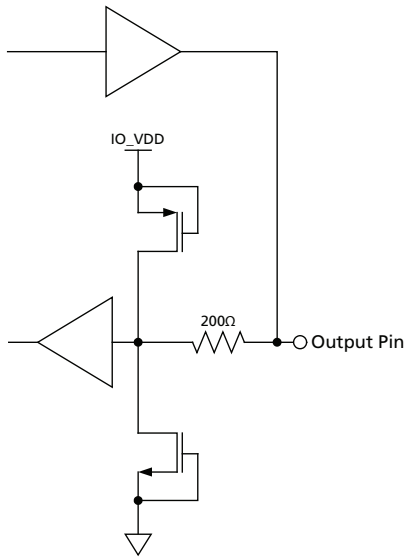


Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output unless in Reset Mode; in which case they are high-impedance. The drive strength can be set by writing to address 06Dh in the host interface register. (DOUT0, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, DOUT6, DOUT7, DOUT8, DOUT9, SDOUT\_TDO, STAT0, STAT1, STAT2, STAT3, STAT4, STAT5, XTAL\_OUT, DOUT10, DOUT11, DOUT12, DOUT13, DOUT14, DOUT15, DOUT16, DOUT17, DOUT18, DOUT19, PCLK)

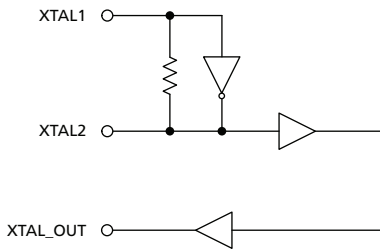


Figure 3-4: XTAL1/XTAL2/XTAL\_OUT

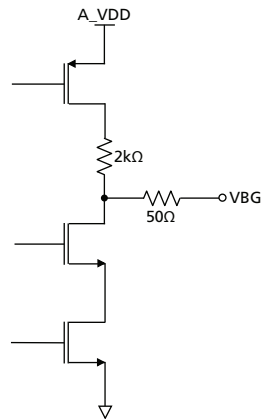


Figure 3-5: VBG

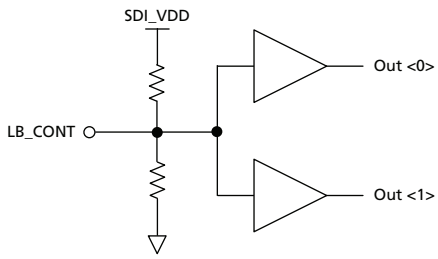


Figure 3-6: LB\_CONT

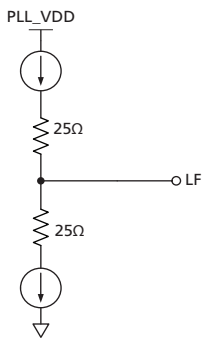


Figure 3-7: Loop Filter

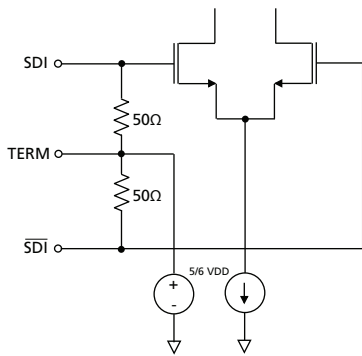


Figure 3-8: SDI/ $\overline{\text{SDI}}$  and TERM

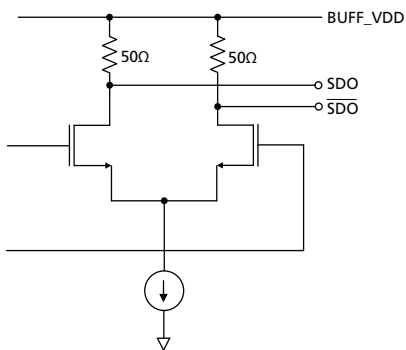


Figure 3-9: SDO/ $\overline{\text{SDO}}$

## 4. Detailed Description

### 4.1 Functional Overview

The GS1670A is a multi-rate, multi-standard receiver with integrated SMPTE video processing as well as an integrated audio de-embedder, compliant with SMPTE ST 292 and SMPTE ST 259-C signals.

The GS1670A includes an integrated reclocker, serial data loop through output, robust serial-to-parallel conversion, integrated SMPTE video processing, and additional processing functions such as audio extraction, ancillary data extraction, EDH support, and DVB-ASI decoding.

The device supports four distinct modes of operation that can be set through external device pins or by programming internal registers through the host interface; SMPTE mode, Data-Through mode, DVB-ASI mode and Standby mode.

In SMPTE mode, all video processing features, ancillary data extraction, and audio de-embedding features are enabled by default.

In DVB-ASI mode, the GS1670A carries out 8b/10b decoding and generates 10-bit parallel DVB-ASI compliant data.

In Data-Through mode, the device operates as a simple serial to parallel converter. No additional processing features are enabled.

Standby mode is the low power consumption mode of the device. In this mode, the internal reclocker will unlock, and the internal configuration registers will not be accessible through the host interface.

The GS1670A includes a JTAG interface for boundary scan testing.

### 4.2 Serial Digital Input

The GS1670A can accept serial digital inputs compliant with SMPTE ST 292 and SMPTE ST 259-C. The serial digital input buffer features 50 $\Omega$  input termination and can be DC-coupled to Semtech's SD/HD-capable equalizers.

### 4.3 Serial Digital Loop-Through Output

The GS1670A contains a 100 $\Omega$  differential serial output buffer which can be configured to output either a retimed or a buffered version of the serial digital input. The SDO and  $\overline{\text{SDO}}$  outputs of this buffer can interface directly to a SD/HD-capable, SMPTE compliant Semtech cable driver. See [5.1 Typical Application Circuit](#) on [page 124](#).

When the  $\overline{\text{RC\_BYP}}$  pin is set HIGH, the serial digital output is the re-timed version of the serial input.

When the  $\overline{\text{RC\_BYP}}$  pin is set LOW, the serial digital output is simply the buffered version of the serial input, bypassing the internal reclocker.