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GS2960A

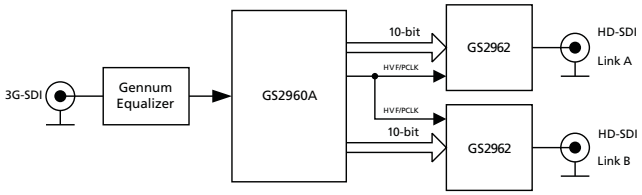
3Gb/s, HD, SD SDI Receiver Complete with SMPTE Video Processing

Key Features

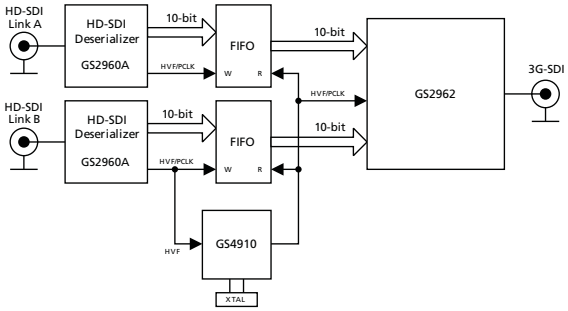
- Operation at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE 425M (Level A and Level B), SMPTE 424M, SMPTE 292, SMPTE 259M-C and DVB-ASI
- Integrated Reclocker
- Integrated low phase noise VCO
- Serial digital reclocked, or non-reclocked loop-through output
- Ancillary data extraction
- Optional conversion from SMPTE 425M Level B to Level A for 1080p 50/60 4:2:2 10-bit inputs
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 Timing Signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI Host Interface
- Wide temperature range of -40°C to +85°C
- Low power operation (typically 350 mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

Applications

Application: Single Link (3G-SDI) to Dual Link (HD-SDI) Converter



Application: Dual Link (HD-SDI) to Single Link (3G-SDI) Converter



Description

The GS2960A is a multi-rate SDI Receiver which includes complete SMPTE processing, as per SMPTE 425M, 292 and SMPTE 259M-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The device features an integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The Serial Digital Output can be connected to an external Cable Driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode, the GS2960A performs SMPTE de-scrambling and NRZI to NRZ decoding and word alignment. Line-based CRC errors, line number errors, TRS errors and ancillary data check sum errors can all be detected. The GS2960A also provides ancillary data extraction. The entire ancillary data packet is extracted, and written to host-accessible registers. Other processing functions include H:V:F timing extraction, Luma and Chroma ancillary data indication, video standard detection, and SMPTE 352M packet detection and decoding. All of the processing features are optional and may be enabled or disabled via the Host Interface.

Both SMPTE 425M Level A and Level B inputs are supported. The GS2960A also provides user-selectable conversion from Level B to Level A for 1080p 50/60 4:2:2 10-bit formats only.

In DVB-ASI mode, sync word detection, alignment and 8b/10b decoding is applied to the received data stream.

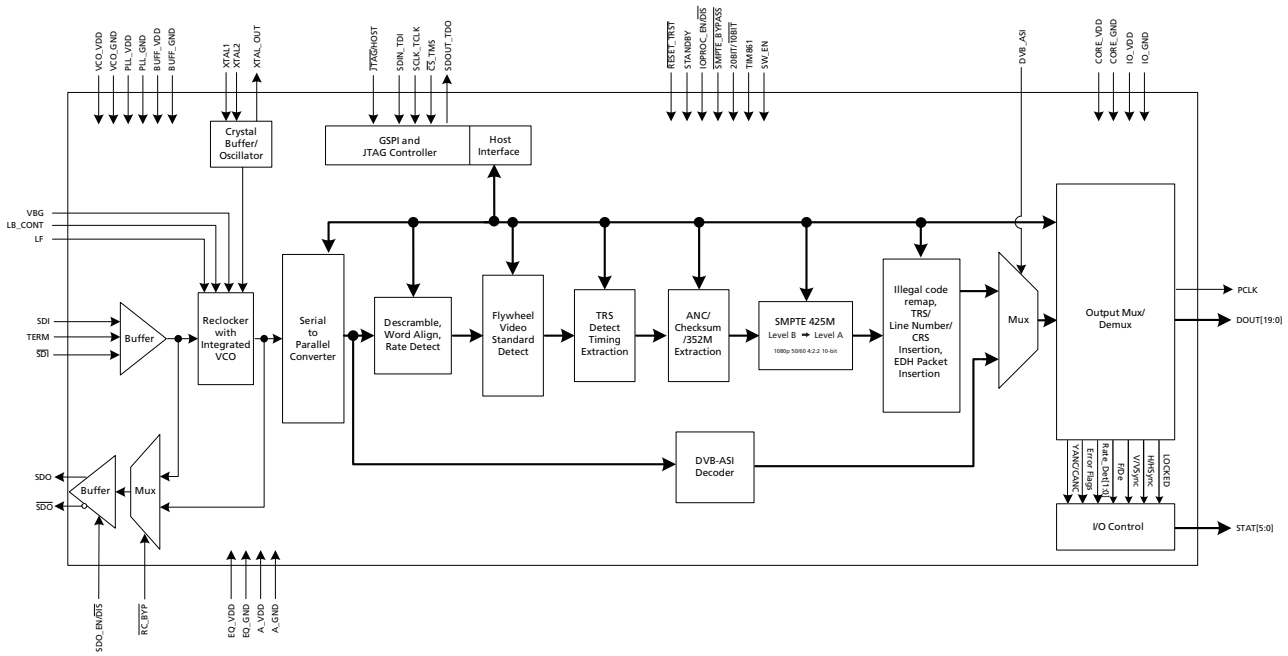
In Data-Through mode all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

The device can also be placed in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static.

Parallel data outputs are provided in 20-bit or 10-bit multiplexed format for 3Gb/s, HD and SD video rates. For 1080p 50/60 4:2:2 10-bit, the parallel data is output on the 20-bit parallel bus as Y on 10 bits and Cb/Cr on the other 10 bits. As such, this parallel bus can interface directly with video processor ICs. For other SMPTE 425M mapping structures, the video data is mapped to a 20-bit virtual interface as described in SMPTE 425M. In all cases this 20-bit parallel bus can be multiplexed onto 10 bits for a low pin count interface with downstream devices. The associated Parallel Clock input signal operates at 148.5 or 148.5/1.001MHz (for all 3Gb/s HD 10-bit multiplexed modes), 74.25 or 74.25/1.001MHz (for HD 20-bit mode), 27MHz (for SD 10-bit mode) and 13.5MHz (for SD 20-bit mode).

Note: for 3Gb/s 10-bit mode the device operates in Dual Data Rate (DDR) mode, where the data is sampled at both the rising and falling edges of the clock. This reduces the I/O speed requirements of the downstream devices.

Functional Block Diagram



GS2960A Functional Block Diagram

Contents

Key Features 1
Applications 1
Description 1
Functional Block Diagram 2
1. Pin Out 7
1.1 Pin Assignment 7
1.2 Pin Descriptions 7
2. Electrical Characteristics 14
2.1 Absolute Maximum Ratings 14
2.2 Recommended Operating Conditions 14
2.3 DC Electrical Characteristics 15
2.4 AC Electrical Characteristics 17
3. Input/Output Circuits 22
4. Detailed Description 25
4.1 Functional Overview 25
4.2 SMPTE 425M Mapping - 3G Level A and Level B Formats 25
4.2.1 Level A Mapping 25
4.2.2 Level B Mapping 26
4.3 Serial Digital Input 26
4.4 Serial Digital Loop-Through Output 26
4.5 Serial Digital Reclocker 27
4.5.1 PLL Loop Bandwidth 27
4.6 External Crystal/Reference Clock 28
4.7 Lock Detect 29
4.7.1 Asynchronous Lock 30
4.7.2 Signal Interruption 31
4.8 SMPTE Functionality 31
4.8.1 Descrambling and Word Alignment 31
4.9 Parallel Data Outputs 32
4.9.1 Parallel Data Bus Buffers 32
4.9.2 Parallel Output in SMPTE Mode 35
4.9.3 Output Data Format in DVB-ASI Mode 35
4.9.4 Parallel Output in Data-Through Mode 36
4.9.5 Parallel Output Clock (PCLK) 36
4.9.6 DDR Parallel Clock Timing 37
4.10 Timing Signal Generator 39
4.10.1 Manual Switch Line Lock Handling 40
4.10.2 Automatic Switch Line Lock Handling 41
4.10.3 Switch Line Lock Handling During Level B to Level A Conversion 41
4.11 Programmable Multi-function Outputs 43
4.12 H:V:F Timing Signal Generation 44
4.12.1 CEA-861 Timing Generation 46
4.13 Automatic Video Standards Detection 52
4.13.1 2K Support 56

4.14 Data Format Detection & Indication 56
4.15 EDH Detection 57
4.15.1 EDH Packet Detection 57
4.15.2 EDH Flag Detection 58
4.16 Video Signal Error Detection & Indication 58
4.16.1 TRS Error Detection 60
4.16.2 Line Based CRC Error Detection 60
4.16.3 EDH CRC Error Detection 61
4.16.4 HD & 3G Line Number Error Detection 61
4.17 Ancillary Data Detection & Indication 61
4.17.1 Programmable Ancillary Data Detection 63
4.17.2 SMPTE 352M Payload Identifier 64
4.17.3 Ancillary Data Checksum Error 65
4.17.4 Video Standard Error 66
4.18 Signal Processing 66
4.18.1 TRS Correction & Insertion 67
4.18.2 Line Based CRC Correction & Insertion 68
4.18.3 Line Number Error Correction & Insertion 68
4.18.4 ANC Data Checksum Error Correction & Insertion 68
4.18.5 EDH CRC Correction & Insertion 68
4.18.6 Illegal Word Re-mapping 69
4.18.7 TRS and Ancillary Data Preamble Remapping 69
4.18.8 Ancillary Data Extraction 69
4.18.9 Level B to Level A Conversion 73
4.19 GSPI - HOST Interface 74
4.19.1 Command Word Description 75
4.19.2 Data Read or Write Access 75
4.19.3 GSPI Timing 76
4.20 Host Interface Register Maps 78
4.21 JTAG Test Operation 92
4.22 Device Power-up 93
4.23 Device Reset 93
4.24 Standby Mode 93
5. Application Reference Design 94
5.1 Typical Application Circuit 94
6. References & Relevant Standards 95
7. Package & Ordering Information 96
7.1 Package Dimensions 96
7.2 Packaging Data 97
7.3 Marking Diagram 97
7.4 Solder Reflow Profiles 98
7.5 Ordering Information 98
Revision History 98

List of Figures

Figure 3-1: Digital Input Pin with Schmitt Trigger 22
Figure 3-2: Bidirectional Digital Input/Output Pin 22
Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength 23
Figure 3-4: XTAL1/XTAL2/XTAL-OUT 23
Figure 3-5: VBG 23
Figure 3-6: LB_CONT 24
Figure 3-7: Loop Filter 24
Figure 3-8: SDI/$\overline{\text{SDI}}$ and TERM 24
Figure 3-9: SDO/$\overline{\text{SDO}}$ 24
Figure 4-1: Level A Mapping 25
Figure 4-2: Level B Mapping 26
Figure 4-3: 27MHz Clock Sources 29
Figure 4-4: PCLK to Data and Control Signal Output Timing - SDR Mode 1 32
Figure 4-5: PCLK to Data and Control Signal Output Timing - SDR Mode 2 33
Figure 4-6: PCLK to Data and Control Signal Output Timing - DDR Mode 34
Figure 4-7: DDR Video Interface - 3G Level A 37
Figure 4-8: DDR Video Interface - 3G Level B 38
Figure 4-9: Delay Adjustment Ranges 39
Figure 4-10: Switch Line Locking on a Non-Standard Switch Line 40
Figure 4-11: H:V:F Output Timing - 3G Level A and HDTV 20-bit Mode 44
Figure 4-12: H:V:F Output Timing - 3G Level A and HDTV 10-bit Mode
3G Level B 20-bit Mode, each 10-bit stream 44
Figure 4-13: H:V:F Output Timing - 3G Level B 10-bit Mode 45
Figure 4-14: H:V:F Output Timing - HD 20-bit Output Mode 45
Figure 4-15: H:V:F Output Timing - HD 10-bit Output Mode 45
Figure 4-16: H:V:F Output Timing - SD 20-bit Output Mode 45
Figure 4-17: H:V:F Output Timing - SD 10-bit Output Mode 45
Figure 4-18: H:V:DE Output Timing 1280 x 720p @ 59.94/60 (Format 4) 47
Figure 4-19: H:V:DE Output Timing 1920 x 1080i @ 59.94/60 (Format 5) 47
Figure 4-20: H:V:DE Output Timing 720 (1440) x 480i @ 59.94/60 (Format 6&7) 48
Figure 4-21: H:V:DE Output Timing 1280 x 720p @ 50 (Format 19) 48
Figure 4-22: H:V:DE Output Timing 1920 x 1080i @ 50 (Format 20) 49
Figure 4-23: H:V:DE Output Timing 720 (1440) x 576 @ 50 (Format 21 & 22) 50
Figure 4-24: H:V:DE Output Timing 1920 x 1080p @ 59.94/60 (Format 16) 50
Figure 4-25: H:V:DE Output Timing 1920 x 1080p @ 50 (Format 31) 51
Figure 4-26: H:V:DE Output Timing 1920 x 1080p @ 23.94/24 (Format 32) 51
Figure 4-27: H:V:DE Output Timing 1920 x 1080p @ 25 (Format 33) 52
Figure 4-28: H:V:DE Output Timing 1920 x 1080p @ 29.97/30 (Format 34) 52
Figure 4-29: 2K Feature Enhancement 56
Figure 4-30: Y/1ANC and C/2ANC Signal Timing 63
Figure 4-31: Ancillary Data Extraction - Step A 70
Figure 4-32: Ancillary Data Extraction - Step B 71
Figure 4-33: Ancillary Data Extraction - Step C 71
Figure 4-34: Ancillary Data Extraction - Step D 72
Figure 4-35: GSPI Application Interface Connection 74
Figure 4-36: Command Word Format 75
Figure 4-37: Data Word Format 76
Figure 4-38: Write Mode 76
Figure 4-39: Read Mode 76
Figure 4-40: GSPI Time Delay 76
Figure 4-41: In-Circuit JTAG 92
Figure 4-42: System JTAG 92
Figure 4-43: Reset Pulse 93
Figure 7-1: Pb-free Solder Reflow Profile 98

List of Tables

Table 1-1: Pin Descriptions 7
Table 2-1: Absolute Maximum Ratings 14
Table 2-2: Recommended Operating Conditions 14
Table 2-3: DC Electrical Characteristics 15
Table 2-4: AC Electrical Characteristics 17
Table 4-1: Serial Digital Output 27
Table 4-2: PLL Loop Bandwidth 27
Table 4-3: Input Clock Requirements 29
Table 4-4: Lock Detect Conditions 30
Table 4-5: GS2960A Output Video Data Format Selections 34
Table 4-6: GS2960A PCLK Output Rates 36
Table 4-7: Switch Line Position for Digital Systems 42
Table 4-8: Output Signals Available on Programmable Multi-Function Pins 43
Table 4-9: Supported CEA-861 Formats 46
Table 4-10: Supported Video Standard Codes 53
Table 4-11: Data Format Register Codes 57
Table 4-12: Error Status Register and Error Mask Register 59
Table 4-13: SMPTE 352M Packet Data 65
Table 4-14: IOPROC_DISABLE Register Bits 67
Table 4-15: GSPI Time Delay 76
Table 4-16: GSPI Timing Parameters (50% levels; 3.3V or 1.8V operation) 77
Table 4-17: Configuration and Status Registers 78
Table 4-18: ANC Extraction FIFO Access Registers 91
Table 7-1: Packaging Data 97

1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_ VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	A_VDD	PLL_ VDD	RSV	VCO_ GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	A_GND	PLL_ VDD	PLL_ VDD	STAT4	STAT5	$\overline{\text{RESET}}$ _TRST	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	A_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SW_EN	JTAG/ $\overline{\text{HOST}}$	IO_GND	IO_VDD
E	SDI_VDD	SDI_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SDOUT_ TDO	SDIN_ TDI	DOUT10	DOUT11
F	TERM	RSV	A_GND	PLL_ GND	CORE _GND	CORE _VDD	$\overline{\text{CS}}$_ TMS	SCLK_ TCK	DOUT8	DOUT9
G	RSV	RSV	$\overline{\text{RC\_BYP}}$	CORE _GND	CORE _GND	CORE _VDD	$\overline{\text{SMPTE\_ BYPASS}}$	DVB_ASI	IO_GND	IO_VDD
H	BUFF_ VDD	BUFF_ GND	RSV	RSV	TIM_861	XTAL_ OUT	20bit/ $\overline{\text{10bit}}$	IOPROC_ EN/$\overline{\text{DIS}}$	DOUT6	DOUT7
J	SDO	SDO_ EN/$\overline{\text{DIS}}$	RSV	RSV	RSV	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STANDBY	RSV	RSV	RSV	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
A1	VBG		Analog Input	Band Gap voltage filter connection.
A2	LF		Analog Input	Loop Filter component connection.
A3	LB_CONT		Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD		Input Power	POWER pin for the VCO. Connect to a 1.2V±5% analog supply followed by a RC filter (see 5.1 Typical Application Circuit). A 105Ω 1% resistor must be used in the RC filter circuit. VCO_VDD is nominally 0.7V.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A5, A6, B5, B6, C5, C6	STAT[0:5]		Output	MULTI-FUNCTIONAL OUTPUT PORT. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Each of the STAT [0:5] pins can be configured individually to output one of the following signals:
				Signal — Default H/HSYNC — STAT0 V/VSYNC — STAT1 F/DE — STAT2 LOCKED — STAT3 Y/1ANC — STAT4 C/2ANC — – $\overline{\text{DATA ERROR}}$ — STAT5 $\overline{\text{VIDEO ERROR}}$ — – EDH DETECTED — – CARRIER DETECT — – RATE_DET0 — – RATE_DET1 — –
A7, D10, G10, K7	IO_VDD		Input Power	POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.
A8	PCLK		Output	PARALLEL DATA BUS CLOCK Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
				3G 10-bit or 20-bit mode — PCLK @ 148.5 or 148.5/1.001MHz HD 10-bit mode — PCLK @ 148.5 or 148.5/1.001MHz HD 20-bit mode — PCLK @ 74.25 or 74.25/1.001MHz SD 10-bit mode — PCLK @ 27MHz SD 20-bit mode — PCLK @ 13.5MHz

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
A9, A10, B8, B9, B10,C8, C9, C10, E9, E10	DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11		Output	PARALLEL DATA BUS Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.	
				20-bit mode 20bit/$\overline{10bit}$ = HIGH	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Luma data output for SD and HD data rates; Data Stream 1 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
				10-bit mode 20bit/$\overline{10bit}$ = LOW	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1&2 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): 8b/10b decoded DVB-ASI data Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
B1	A_VDD		Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.	
B2, C3, C4	PLL_VDD		Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.	
B3, F2, G1, G2	RSV			These pins must be left unconnected.	
B4	VCO_GND		Input Power	GND pin for the VCO. Connect to analog GND.	
B7, D9, G9, J7	IO_GND		Input Power	GND connection for digital I/O. Connect to digital GND.	
C1, D1	SDI, $\overline{SDI}$		Analog Input	Serial Digital Differential Input.	
C2, D2, D3, E3, F3	A_GND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
C7	$\overline{\text{RESET\_TRST}}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG/$\overline{\text{HOST}}$ = LOW): When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG/$\overline{\text{HOST}}$ = HIGH): When LOW, all functional blocks are set to default and the JTAG test sequence is reset. When HIGH, normal operation of the JTAG test sequence resumes after $\overline{\text{RESET\_TRST}}$ is de-asserted.
D4, E4, F4	PLL_GND		Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G4, G5	CORE_GND		Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD		Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	SW_EN		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable switch-line locking, as described in Section 4.10.1.
D8	JTAG/$\overline{\text{HOST}}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select JTAG test mode or host interface mode. When JTAG/$\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/$\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes.
E1	SDI_VDD		Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	SDI_GND		Input Power	GND pin for SDI buffer. Connect to analog GND.
E7	SDOUT_TDO		Output	COMMUNICATION SIGNAL OUTPUT Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. GSPI serial data output/test data out. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test results from the device. In host interface mode, this pin is used to read status and configuration data from the device. **Note:** GSPI is slightly different than the SPI. For more details on GSPI, please refer to 4.19 GSPI - HOST Interface.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
E8	SDIN_TDI		Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. GSPI serial data in/test data in. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test data into the device. In host interface mode, this pin is used to write address and configuration data words into the device.
F1	TERM		Analog Input	Decoupling for internal SDI termination resistors.
F7	$\overline{\text{CS}}$_TMS		Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Chip select / test mode start. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test. In host interface mode (JTAG/$\overline{\text{HOST}}$ = LOW), this pin operates as the host interface chip select and is active LOW.
F8	SCLK_TCK		Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Serial data clock signal. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is the JTAG clock. In host interface mode (JTAG/$\overline{\text{HOST}}$ = LOW), this pin is the host interface serial bit clock. All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.
F9, F10, H9, H10, J8, J9, J10, K8, K9, K10	DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3		Output	PARALLEL DATA BUS Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. **20-bit mode (20bit/$\overline{\text{10bit}}$ = HIGH)** SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB_ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for 3G data rate DVB-ASI mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output **10-bit mode (20bit/$\overline{\text{10bit}}$ = LOW)** Forced LOW
G3	$\overline{\text{RC\_BYP}}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G7	$\overline{\text{SMPTE\_BYPASS}}$		Input/Output	CONTROL SIGNAL INPUT/OUTPUT Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Indicates the presence of valid SMPTE data. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{\text{SMPTE\_BYPASS}}$ is HIGH when the device locks to a SMPTE compliant input. $\overline{\text{SMPTE\_BYPASS}}$ is LOW under all other conditions. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is LOW, this pin is an INPUT: No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ is set HIGH, the device carries out SMPTE scrambling and I/O processing. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode.
G8	DVB_ASI		Input/Output	CONTROL SIGNAL INPUT Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable/disable DVB-ASI data extraction in manual mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is LOW, this pin is an input and when the DVB_ASI pin is set HIGH the device carries out DVB_ASI data extraction and processing. The $\overline{\text{SMPTE\_BYPASS}}$ pin must be set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is HIGH (Default), DVB-ASI is configured as a status output (set LOW), and DVB-ASI input streams are not supported or recognized.
H1	BUFF_VDD		Input Power	POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND		Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H3, H4, J3, J4, J5, K3, K5	RSV			These pins must be connected to CORE_GND.
H5	TIM_861		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select CEA-861 timing mode. When TIM_861 is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.
H6	XTAL_OUT		Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H7	20bit/$\overline{10bit}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select the output bus width. HIGH = 20-bit, LOW = 10-bit.
H8	IOPROC_EN/$\overline{DIS}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable or disable video processing features. When IOPROC_EN is HIGH, the video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.
J1, K1	SDO, $\overline{SDO}$		Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN/$\overline{DIS}$		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable/disable the serial digital output stage. When SDO_EN/$\overline{DIS}$ is LOW, the serial digital output signals, SDO and $\overline{SDO}$, are both pulled HIGH. When SDO_EN/$\overline{DIS}$ is HIGH, the serial digital output signals, SDO and $\overline{SDO}$, are enabled.
J6, K6	XTAL2, XTAL1		Analog Input	Input connection for 27MHz crystal.
K2	STANDBY		Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and $\overline{SDO}$, are both pulled HIGH.
K4	RSV			This pin must be left unconnected.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (SDI_VDD, BUFF_VDD, A_VDD)	-0.3V to +4.0V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Operating Temperature Range	-20°C to +85°C
Functional Temperature Range	-40°C to +85°C
Storage Temperature Range	-50°C to +125°C
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

NOTES:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

T_A = -20°C to + 85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	1
Supply Voltage, Serial Digital Input	SDI_VDD	–	3.13	3.3	3.47	V	1
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	1

NOTES:

1. The 3.3V supplies must track the 3.3V supply of an external EQ and external CD.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10bit 3G	–	200	235	mA	–
		20bit 3G	–	195	235	mA	–
		10/20bit HD	–	160	210	mA	–
		10/20bit SD	–	135	165	mA	–
		DVB_ASI	–	135	165	mA	–
+1.8V Supply Current	I_{1V8}	10bit 3G	–	32	34	mA	–
		20bit 3G	–	31	34	mA	–
		10/20bit HD	–	20	21	mA	–
		10/20bit SD	–	6	7	mA	–
		DVB_ASI	–	6	7	mA	–
+3.3V Supply Current	I_{3V3}	10bit 3G	–	95	105	mA	–
		20bit 3G	–	95	105	mA	–
		10/20bit HD	–	65	75	mA	–
		10/20bit SD	–	35	45	mA	–
		DVB_ASI	–	35	45	mA	–
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10bit 3G	–	350	430	mW	–
		20bit 3G	–	320	400	mW	–
		10/20bit HD	–	280	335	mW	–
		10/20bit SD	–	240	305	mW	–
		DVB_ASI	–	240	305	mW	–
		Reset	–	200	–	mW	–
		Standby	–	16	44	mW	–
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10bit 3G	–	550	665	mW	–
		20bit 3G	–	520	665	mW	–
		10/20bit HD	–	400	505	mW	–
		10/20bit SD	–	280	370	mW	–
		DVB_ASI	–	280	370	mW	–
		Reset	–	220	–	mW	–
		Standby	–	16	44	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VSS -0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD +0.3	V	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output Logic LOW	V_{OL}	IOL = 5mA, 1.8V operation	–	–	0.2	V	–
		IOL = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOH = 5mA, 1.8V operation	1.4	–	–	V	–
		IOH = 8mA, 3.3V operation	2.4	–	–	V	–
Serial Input							
Serial Input Common Mode Voltage	–	50Ω load	2.5	SDI_VDD -(0.75/2)	SDI_VDD -(0.55/2)	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD -(0.6/2)	BUFF_VDD -(0.45/2)	BUFF_VDD -(0.35/2)	V	–

NOTES:

1. The output drive strength of the digital outputs can be programmed through the host interface. Please see Table 4-17: Configuration and Status Registers, register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
System								
Device Latency: SMPTE mode, IOPROC_EN = 1	–	3G (Level A)		44	–	48	PCLK	–
		3G (Level B)		108	–	116	PCLK	–
		HD		44	–	48	PCLK	–
		SD		44	–	48	PCLK	–
Device Latency: SMPTE mode, IOPROC_EN = 0	–	3G (Level A)		33	–	36	PCLK	–
		HD		33	–	36	PCLK	–
		SD		32	–	35	PCLK	–
Device Latency: SMPTE bypass, IOPROC_EN = 0	–	3G (Level A)		6	–	9	PCLK	–
		HD		6	–	9	PCLK	–
		SD		5	–	9	PCLK	–
Device Latency: DVB-ASI	–	SD		12	–	16	PCLK	–
Reset Pulse Width	t_{reset}	–		1	–	–	ms	–
Parallel Output								
Parallel Clock Frequency	f_{PCLK}	–		13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–		45	–	55	%	–
Output Data Hold Time (1.8V)	t_{oh}	3G 10-bit 6pF Cload	SPI	1.5	–	–	ns	1
			DBUS	0.3	–	–	ns	1
			STAT	0.3	–	–	ns	1
		3G 20-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		HD 10-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		HD 20-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		SD 10-bit 6pF Cload	DBUS	19.4	–	–	ns	1
			STAT	19.4	–	–	ns	1
		SD 20-bit 6pF Cload	DBUS	38.0	–	–	ns	1
			STAT	38.0	–	–	ns	1

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Hold Time (3.3V)	t_{oh}	3G 10-bit 6pF Cload	SPI	1.5	–	–	ns	2
			DBUS	0.3	–	–	ns	2
			STAT	0.3	–	–	ns	2
		3G 20-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		HD 10-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		HD 20-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		SD 10-bit 6pF Cload	DBUS	19.4	–	–	ns	2
			STAT	19.4	–	–	ns	2
		SD 20-bit 6pF Cload	DBUS	38.0	–	–	ns	2
			STAT	38.0	–	–	ns	2
Output Data Delay Time (1.8V)	t_{od}	3G 10-bit 15pF Cload	SPI	–	–	14.0	ns	3
			DBUS	–	–	1.8	ns	3
			STAT	–	–	2.5	ns	3
		3G 20-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		HD 10-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		HD 20-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		SD 10-bit 15pF Cload	DBUS	–	–	22.2	ns	3
			STAT	–	–	22.2	ns	3
		SD 20-bit 15pF Cload	DBUS	–	–	41.0	ns	3
			STAT	–	–	41.0	ns	3

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Delay Time (3.3V)	t_{od}	3G 10-bit 15pF Cload	SPI	–	–	14.0	ns	4
			DBUS	–	–	1.9	ns	4
			STAT	–	–	2.2	ns	4
		3G 20-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		HD 10-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		HD 20-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		SD 10-bit 15pF Cload	DBUS	–	–	22.2	ns	4
			STAT	–	–	22.2	ns	4
		SD 20-bit 15pF Cload	DBUS	–	–	41.0	ns	4
			STAT	–	–	41.0	ns	4
Output Data Rise/Fall Time (1.8V)	t_r/t_f	3G 10-bit 6pF Cload	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.3	ns	1
		All other modes 6pF Cload	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.4	ns	1
		3G 10-bit 15pF Cload	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.1	ns	3
		All other modes 15pF Cload	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.4	ns	3
Output Data Rise/Fall Time (3.3V)	t_r/t_f	3G 10-bit 6pF Cload	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
		All other modes 6pF Cload	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
		3G 10-bit 15pF Cload	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.5	ns	4
		All other modes 15pF Cload	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.4	ns	4
Serial Digital Input								
Serial Input Data Rate	DR_{SDI}	–		0.27	–	2.97	Gb/s	–
Serial Input Swing	ΔV_{SDI}	Differential with 100Ω load		500	800	1100	mVp-p	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Jitter Tolerance	IJT	Nominal loop bandwidth Square wave mod.	0.7	0.8	–	UI	–
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	0.27	–	2.97	Gb/s	–
Serial Output Swing	ΔV_{SDO}	Differential with 100Ω load	350	–	600	mVp-p	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	–	–	–	180	ps	–
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	–	–	–	180	ps	–
Serial Output Intrinsic Jitter	t_{OJ}	SMPTE colour bar 3G signal	–	–	100	ps	–
		SMPTE colour bar HD signal	–	–	100	ps	–
		SMPTE colour bar SD signal	–	–	400	ps	–
Serial Output Duty Cycle Distortion	DCD_{SDD}	3G	–	10	–	ps	–
		HD	–	10	–	ps	–
		SD	–	20	–	ps	–
Synchronous lock time	–	–	–	–	25	µs	–
Asynchronous lock time	–	Manual mode, noise immunity disabled	100	–	350	µs	–
		Auto mode, noise immunity disabled	100	–	600	µs	5
		Noise immunity enabled	100	–	1200	µs	5
Lock time from power-up	–	After 20 minutes at -20°C	–	325		ms	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	60	MHz	6
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	6
GSPI Input Data Setup Time	–		1.5	–	–	ns	6
GSPI Input Data Hold Time	–		1.5	–	–	ns	6
GSPI Output Data Hold Time	–		1.5	–	–	ns	6
$\overline{CS}$ low before SCLK rising edge	–		1.5	–	–	ns	6
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–		37.1	–	–	ns	6
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–		148.4	–	–	ns	6
$\overline{CS}$ high after SCLK falling edge	–		37.1	–	–	ns	6

NOTES:

1. 1.89V and 0°C.
2. 3.47V and 0°C.
3. 1.71V and 85°C
4. 3.13V and 85°C
5. 720_24p format requires a longer lock time
6. Timing parameters defined in Section 4.19.3

3. Input/Output Circuits

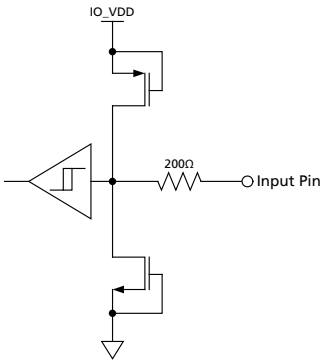


Figure 3-1: Digital Input Pin with Schmitt Trigger (20BIT/$\overline{10BIT}$, $\overline{CS}$_TMS, SW_EN, IOPROC_EN/$\overline{DIS}$, JTAG/$\overline{HOST}$, $\overline{RC\_BYP}$, $\overline{RESET\_TRST}$, SCLK_TCK, SDIN_TDI, SDO_EN/$\overline{DIS}$, STANDBY, TIM_861)

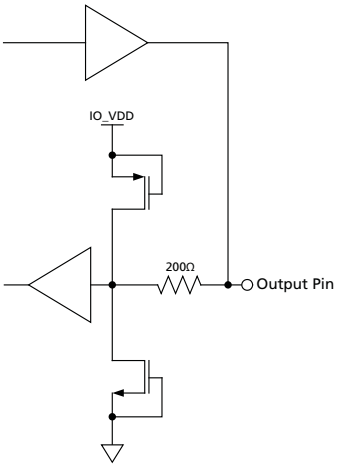


Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (DVB_ASI, $\overline{SMPTE\_BYPASS}$)

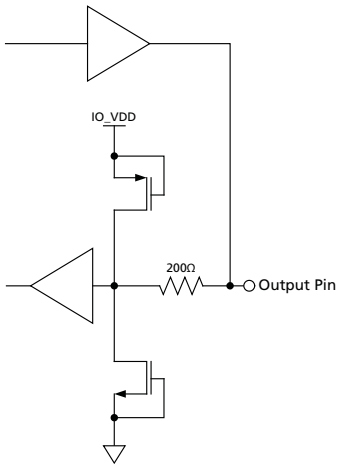


Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output unless in Reset Mode; in which case they are high-impedance. The drive strength can be set by writing to address 06Dh in the host interface register. (DOUT0, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, DOUT6, DOUT7, DOUT8, DOUT9, SDOUT_TDO, STAT0, STAT1, STAT2, STAT3, STAT4, STAT5, XTAL_OUT, DOUT10, DOUT11, DOUT12, DOUT13, DOUT14, DOUT15, DOUT16, DOUT17, DOUT18, DOUT19, PCLK)

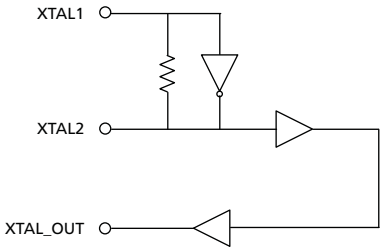


Figure 3-4: XTAL1/XTAL2/XTAL-OUT

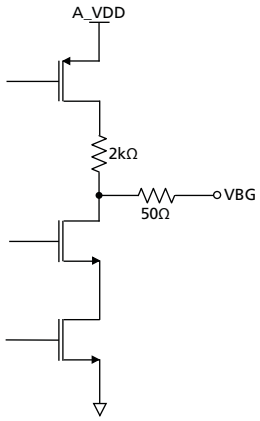


Figure 3-5: VBG

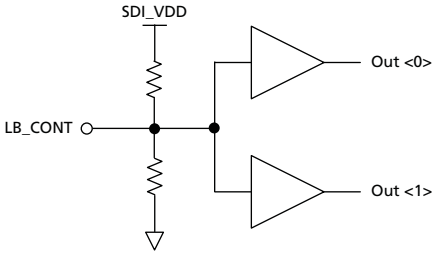


Figure 3-6: LB_CONT

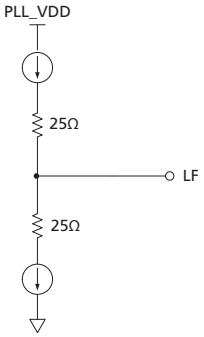


Figure 3-7: Loop Filter

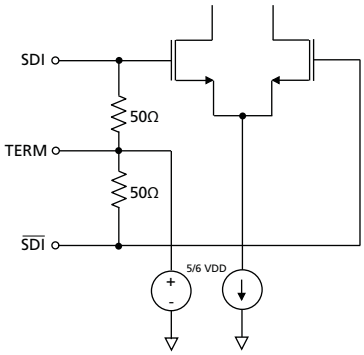


Figure 3-8: SDI/$\overline{\text{SDI}}$ and TERM

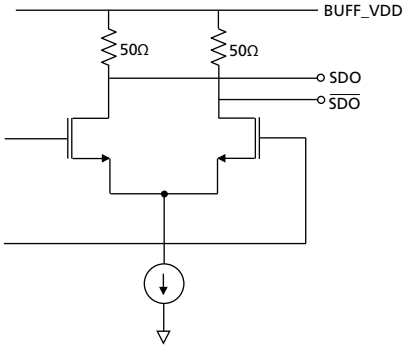


Figure 3-9: SDO/$\overline{\text{SDO}}$

4. Detailed Description

4.1 Functional Overview

The GS2960A is a multi-rate, multi-standard receiver with integrated SMPTE video processing, compliant with SMPTE 425M, SMPTE 424M, SMPTE 292 and SMPTE 259M-C signals. When used in conjunction with Gennum's 3Gb/s-capable equalizers, a complete receive solution that supports full bandwidth 1080p video at 2.97Gb/s can be realized.

The GS2960A includes an integrated reclocker, serial data loop through output, robust serial-to-parallel conversion, integrated SMPTE video processing, and additional processing functions such as ancillary data extraction, EDH support, and DVB-ASI decoding.

The device supports four distinct modes of operation that can be set through external device pins or by programming internal registers through the host interface; SMPTE mode, Data-Through mode, DVB-ASI mode and Standby mode.

In SMPTE mode, all video processing features are enabled by default.

In DVB-ASI mode, the GS2960A carries out 8b/10b decoding and generates 10-bit parallel DVB-ASI compliant data.

In Data-Through mode, the device operates as a simple serial to parallel converter. No additional processing features are enabled.

Standby mode is the low power consumption mode of the device. In this mode, the internal reclocker unlocks, and the internal configuration registers are not accessible through the host interface.

The GS2960A includes a JTAG interface for boundary scan testing.

4.2 SMPTE 425M Mapping - 3G Level A and Level B Formats

4.2.1 Level A Mapping

Direct image format mapping - the mapping structure used to define 1080p/50/59.94/60 4:2:2 YCbCr 10 bit data, as supported by the GS2960A. See Figure 4-1:

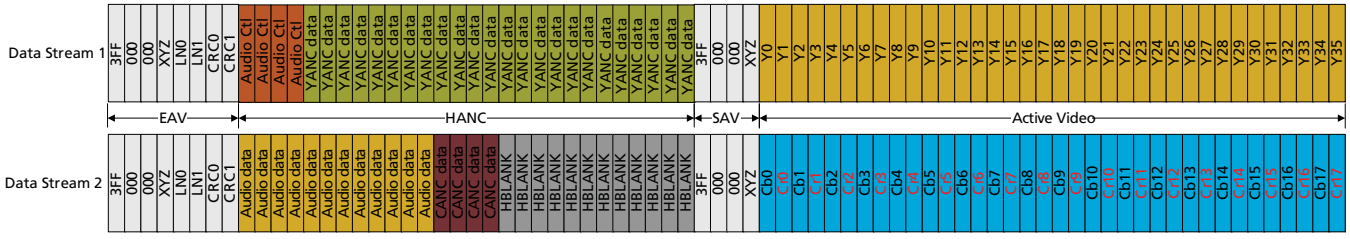


Figure 4-1: Level A Mapping