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GS2961 3Gb/s, HD, SD SDI Receiver, with Integrated Adaptive Cable Equalizer complete with SMPTE Video Processing

Key Features

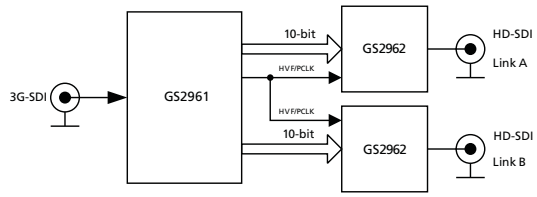
- Operation at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE 425M (Level A and Level B), SMPTE 424M, SMPTE 292M, SMPTE 259M-C and DVB-ASI
- Integrated adaptive cable equalizer
- Typical equalized length of Belden 1694A cable:
  - 150m at 2.97Gb/s
  - 250m at 1.485Gb/s
  - 480m at 270Mb/s
- Integrated Reclocker with low phase noise, integrated VCO
- Serial digital reclocked, or non-reclocked output
- Ancillary data extraction
- Optional conversion from SMPTE 425M Level B to Level A for 1080p 50/60 4:2:2 10-bit
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 Timing Signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI Host Interface
- -20°C to +85°C operating temperature range
- Low power operation (typically 515mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and ROHS compliant

Errata

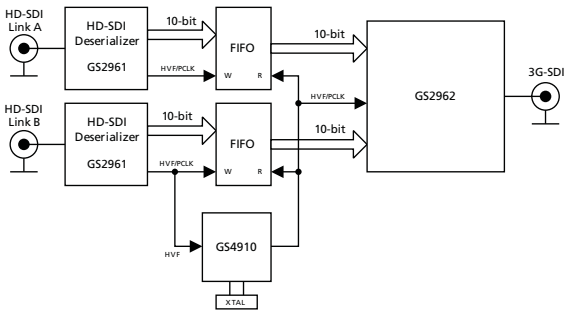
Refer to Errata document entitled **GS2960/GS2961 Errata** for this device (document number **53117**).

Applications

Application: Single Link (3G-SDI) to Dual Link (HD-SDI) Converter



Application: Dual Link (HD-SDI) to Single Link (3G-SDI) Converter



Description

The GS2961 is a multi-rate SDI integrated Receiver which includes complete SMPTE processing, as per SMPTE 425M, 292M and SMPTE 259M-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The GS2961 integrates Gennum's adaptive cable equalizer technology, achieving unprecedented cable lengths and jitter tolerance. It features DC restoration to compensate for the DC content of SMPTE pathological signals.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop-through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The serial digital output can be connected to an external cable driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode (the default operating mode), the GS2961 performs full SMPTE processing, and features a number of data integrity checks and measurement capabilities.

The device also supports ancillary data extraction, and can provide entire ancillary data packets through host-accessible registers. It also provides a variety of other packet detection and error handling features. All of these processing features are optional, and may be individually enabled or disabled through register programming.

Both SMPTE 425M Level A and Level B inputs are supported with optional conversion from Level B to Level A for 1080p 50/59.94/60 4:2:2 10-bit inputs.

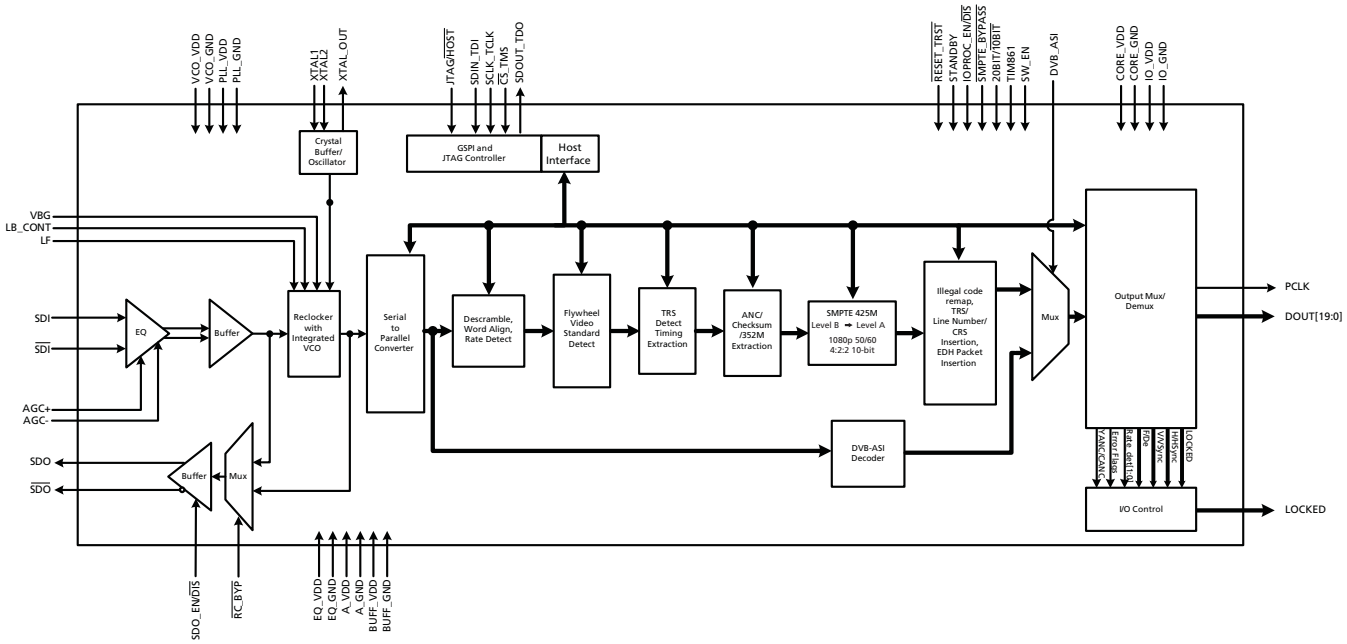
In DVB-ASI mode, sync word detection, alignment and 8b/10b decoding is applied to the received data stream.

In Data-Through mode all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

The device can also operate in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static.

Parallel data outputs are provided in 20-bit or 10-bit format for 3Gb/s, HD and SD video rates, with a variety of mapping options. As such, this parallel bus can interface directly with video processor ICs, and output data can be multiplexed onto 10 bits for a low pin count interface.

Functional Block Diagram



GS2961 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
2	153143	53865	November 2009	Added reference to GS2960/GS2961 Errata (document number 53117). Converted to Data Sheet.
1	152698	–	October 2009	Updated Power numbers in Table 2-3: DC Electrical Characteristics.
0	151888	–	June 2009	Conversion to Preliminary Data Sheet. Corrections to Timing Diagrams in Figure 4-5, Figure 4-6 and Figure 4-7. Clarification to Section 4.18.8. Updates to all sections.
C	151697	–	April 2009	Updated equalized cable lengths and power numbers in Key Features, Table 2-4: AC Electrical Characteristics and Section 4.3.1.
B	151504	–	March 2009	Changed pin H3 from 'RSV' to 'CORE_GND' in 1.1 Pin Assignment, 1.2 Pin Descriptions and 5.3 Typical Application Circuit.
A	151219	–	February 2009	New Document.

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_ VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	A_VDD	PLL_ VDD	RSV	VCO_ GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	A_GND	PLL_ VDD	PLL_ VDD	STAT4	STAT5	$\overline{\text{RESET}}$ _$\overline{\text{TRST}}$	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	A_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SW_EN	JTAG/ $\overline{\text{HOST}}$	IO_GND	IO_VDD
E	EQ_VDD	EQ_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SDOUT_ TDO	SDIN_ TDI	DOUT10	DOUT11
F	AGCP	RSV	A_GND	PLL_ GND	CORE _GND	CORE _VDD	$\overline{\text{CS}}$_ TMS	SCLK_ TCK	DOUT8	DOUT9
G	AGCN	A_GND	$\overline{\text{RC\_BYP}}$	CORE _GND	CORE _GND	CORE _VDD	$\overline{\text{SMPTE}}$_ $\overline{\text{BYPASS}}$	DVB_ASI	IO_GND	IO_VDD
H	BUFF_ VDD	BUFF_ GND	CORE _GND	RSV	TIM_861	XTAL_ OUT	20bit/ $\overline{\text{10bit}}$	IOPROC_ EN/$\overline{\text{DIS}}$	DOUT6	DOUT7
J	SDO	SDO_ EN/$\overline{\text{DIS}}$	RSV	RSV	RSV	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STANDBY	RSV	RSV	RSV	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
A1	VBG		Analog Input	Band Gap voltage filter connection.
A2	LF		Analog Input	Loop Filter component connection.
A3	LB_CONT		Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD		Input Power	POWER pin for the VCO. Connect to 1.2V DC analog through an RC filter (see 5. Application Reference Design). VCO_VDD is nominally 0.7V. (Do not connect directly to 0.7V).

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A5, A6, B5, B6, C5, C6	STAT[0:5]		Output	MULTI-FUNCTIONAL OUTPUT PORT. Signal levels are LVCMOS/LVTTL compatible. Each of the STAT [0:5] pins can be configured individually to output one of the following signals:

Signal	Default
H/HSYNC	STAT0
V/VSYNC	STAT1
F/DE	STAT2
LOCKED	STAT3
Y/1ANC	STAT4
C/2ANC	–
DATA ERROR	STAT5
EDH DETECTED	–
CARRIER DETECT	–
RATE_DET0	–
RATE_DET1	–

A7, D10, G10, K7	IO_VDD		Input Power	POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.
A8	PCLK		Output	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS/LVTTL compatible.

3G 10-bit or 20-bit mode	PCLK @ 148.5 or 148.5/1.001MHz
HD 10-bit mode	PCLK @ 148.5 or 148.5/1.001MHz
HD 20-bit mode	PCLK @ 74.25 or 74.25/1.001MHz
SD 10-bit mode	PCLK @ 27MHz
SD 20-bit mode	PCLK @ 13.5MHz

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
A9, A10, B8, B9, B10,C8, C9, C10, E9, E10	DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11		Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible.	
				20-bit mode 20bit/$\overline{10bit}$ = HIGH	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Luma data output for SD and HD data rates; Data Stream 1 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
				10-bit mode 20bit/$\overline{10bit}$ = LOW	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1&2 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): 8b/10b decoded DVB-ASI data Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
B1	A_VDD		Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.	
B2, C3, C4	PLL_VDD		Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.	
B3, F2, H4, J3, J4, J5, K3, K4, K5	RSV			These pins must be left unconnected.	
B4	VCO_GND		Input Power	GND pin for the VCO. Connect to analog GND.	
B7, D9, G9, J7	IO_GND		Input Power	GND connection for digital I/O. Connect to digital GND.	
C1, D1	SDI, $\overline{SDI}$		Analog Input	Serial Digital Differential Input.	
C2, D2, D3, E3, F3, G2	A_GND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
C7	$\overline{\text{RESET\_TRST}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG/$\overline{\text{HOST}}$ = LOW): When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG/$\overline{\text{HOST}}$ = HIGH): When LOW, all functional blocks are set to default and the JTAG test sequence is reset. When HIGH, normal operation of the JTAG test sequence resumes after $\overline{\text{RESET\_TRST}}$ is de-asserted.
D4, E4, F4	PLL_GND		Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G4, G5, H3	CORE_GND		Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD		Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	SW_EN		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable switch-line locking, as described in Section 4.10.1.
D8	JTAG/$\overline{\text{HOST}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG test mode or host interface mode. When JTAG/$\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/$\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes.
E1	EQ_VDD		Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	EQ_GND		Input Power	GND pin for SDI buffer. Connect to analog GND.
E7	SDOUT_TDO		Output	COMMUNICATION SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. GSPI serial data output/test data out. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test results from the device. In host interface mode, this pin is used to read status and configuration data from the device.
E8	SDIN_TDI		Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. GSPI serial data in/test data in. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test data into the device. In host interface mode, this pin is used to write address and configuration data words into the device.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
F1, G1	AGCP, AGCN			Automatic Gain Control for the equalizer. Attach the AGC capacitor between these pins.	
F7	$\overline{CS}$_TMS		Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip select / test mode start. In JTAG mode (JTAG/$\overline{HOST}$ = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test. In host interface mode (JTAG/$\overline{HOST}$ = LOW), this pin operates as the host interface chip select and is active LOW.	
F8	SCLK_TCK		Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial data clock signal. In JTAG mode (JTAG/$\overline{HOST}$ = HIGH), this pin is the JTAG clock. In host interface mode (JTAG/$\overline{HOST}$ = LOW), this pin is the host interface serial bit clock. All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.	
F9, F10, H9, H10, J8, J9, J10, K8, K9, K10	DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3		Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible.	
				20-bit mode 20bit/$\overline{10bit}$ = HIGH	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
				10-bit mode 20bit/$\overline{10bit}$ = LOW	Forced LOW
G3	$\overline{RC\_BYP}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G7	$\overline{\text{SMPTE\_BYPASS}}$		Input/Output	CONTROL SIGNAL INPUT/OUTPUT Signal levels are LVCMOS/LVTTL compatible. Indicates the presence of valid SMPTE data. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{\text{SMPTE\_BYPASS}}$ is HIGH when the device locks to a SMPTE compliant input. $\overline{\text{SMPTE\_BYPASS}}$ is LOW under all other conditions. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is LOW, this pin is an INPUT: No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ is set HIGH, the device carries out SMPTE scrambling and I/O processing. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode.
G8	DVB_ASI		Input/Output	CONTROL SIGNAL INPUT Signal Levels are LVCMOS/LVTTL compatible. Used to enable/disable DVB-ASI data extraction in manual mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is LOW, this pin is an input and when the DVB_ASI pin is set HIGH the device will carry out DVB_ASI data extraction and processing. The $\overline{\text{SMPTE\_BYPASS}}$ pin must be set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is HIGH (default), DVB-ASI is configured as a status output (set LOW), and DVB-ASI input streams are not supported or recognized.
H1	BUFF_VDD		Input Power	POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND		Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H5	TIM_861		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select CEA-861 timing mode. When TIM_861 is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.
H6	XTAL_OUT		Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.
H7	20bit/$\overline{\text{10bit}}$		Input	CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to select the output bus width. HIGH = 20-bit, LOW = 10-bit.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H8	IOPROC_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to enable or disable video processing features. When IOPROC_EN is HIGH, the video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.
J1, K1	SDO, $\overline{\text{SDO}}$		Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable the serial digital output stage. When SDO_EN/$\overline{\text{DIS}}$ is LOW, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH. When SDO_EN/$\overline{\text{DIS}}$ is HIGH, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are enabled.
J6, K6	XTAL2, XTAL1		Analog Input	Input connection for 27MHz crystal.
K2	STANDBY		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (EQ_VDD, BUFF_VDD, A_VDD)	-0.3V to +4.0V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Ambient Operating Temperature (T_A)	$-40°C \leq T_A \leq 95°C$
Storage Temperature (T_{STG})	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

NOTES:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	2
Supply Voltage, Serial Digital Input	EQ_VDD	–	3.13	3.3	3.47	V	–

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	2

NOTES

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor. See Typical Application Circuit on page 99.
2. The 3.3V supplies must track the 3.3V supply of an external CD.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10bit 3G	–	200	240	mA	–
		20bit 3G	–	190	240	mA	–
		10/20bit HD	–	160	200	mA	–
		10/20bit SD	–	130	170	mA	–
		DVB_ASI	–	130	170	mA	–
+1.8V Supply Current	I_{1V8}	10bit 3G	–	37	45	mA	–
		20bit 3G	–	16	20	mA	–
		10/20bit HD	–	15	21	mA	–
		10/20bit SD	–	4	7	mA	–
		DVB_ASI	–	4	6	mA	–
+3.3V Supply Current	I_{3V3}	10bit 3G	–	150	180	mA	–
		20bit 3G	–	115	130	mA	–
		10/20bit HD	–	110	135	mA	–
		10/20bit SD	–	90	100	mA	–
		DVB_ASI	–	90	95	mA	–
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10bit 3G	–	540	640	mW	–
		20bit 3G	–	500	600	mW	–
		10/20bit HD	–	460	560	mW	–
		10/20bit SD	–	410	490	mW	–
		DVB_ASI	–	410	490	mW	–
		Reset	–	390	–	mW	–
		Standby	–	23	45	mW	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10bit 3G	–	720	890	mW	–
		20bit 3G	–	600	720	mW	–
		10/20bit HD	–	550	700	mW	–
		10/20bit SD	–	440	540	mW	–
		DVB_ASI	–	440	530	mW	–
		Reset	–	410	–	mW	–
		Standby	–	23	45	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VSS -0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD +0.3	V	–
Output Logic LOW	V_{OL}	IOL = 5mA, 1.8V operation	–	–	0.2	V	–
		IOL = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOH = 5mA, 1.8V operation	1.4	–	–	V	–
		IOH = 8mA, 3.3V operation	2.4	–	–	V	–
Serial Input							
Serial Input Common Mode Voltage	–	75Ω load	–	2.2	–	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD -(0.6/2)	BUFF_VDD -(0.45/2)	BUFF_VDD -(0.35/2)	V	–

Notes:

The output drive strength of the digital outputs can be programmed through the host interface. please see Table 4-18: Configuration and Status Registers, register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
System								
Device Latency	–	3G		–	47	–	PCLK	–
		HD		–	47	–	PCLK	–
		SD		–	46	–	PCLK	–
		DVB-ASI		–	14	–	PCLK	–
Reset Pulse Width	t_{reset}	–		1	–	–	ms	–
Parallel Output								
Parallel Clock Frequency	f_{PCLK}	–		13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–		40	–	60	%	–
Output Data Hold Time (1.8V)	t_{oh}	3G 10-bit 6pF Cload	SPI	1.5	–	–	ns	1
			DBUS	0.4	–	–	ns	1
			STAT	0.45	–	–	ns	1
		3G 20-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		HD 10-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		HD 20-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		SD 10-bit 6pF Cload	DBUS	19.4	–	–	ns	1
			STAT	19.4	–	–	ns	1
		SD 20-bit 6pF Cload	DBUS	38.0	–	–	ns	1
			STAT	38.0	–	–	ns	1

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Hold Time (3.3V)	t_{oh}	3G 10-bit 6pF Cload	SPI	1.5	–	–	ns	2
			DBUS	0.45	–	–	ns	2
			STAT	0.45	–	–	ns	2
		3G 20-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		HD 10-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		HD 20-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		SD 10-bit 6pF Cload	DBUS	19.4	–	–	ns	2
			STAT	19.4	–	–	ns	2
		SD 20-bit 6pF Cload	DBUS	38.0	–	–	ns	2
			STAT	38.0	–	–	ns	2
Output Data Delay Time (1.8V)	t_{od}	3G 10-bit 15pF Cload	SPI	–	–	14.0	ns	3
			DBUS	–	–	1.8	ns	3
			STAT	–	–	2.5	ns	3
		3G 20-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		HD 10-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		HD 20-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		SD 10-bit 15pF Cload	DBUS	–	–	22.2	ns	3
			STAT	–	–	22.2	ns	3
		SD 20-bit 15pF Cload	DBUS	–	–	41.0	ns	3
			STAT	–	–	41.0	ns	3

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Delay Time (3.3V)	t_{od}	3G 10-bit 15pF Cload	SPI	–	–	14.0	ns	4
			DBUS	–	–	1.9	ns	4
			STAT	–	–	2.2	ns	4
		3G 20-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		HD 10-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		HD 20-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		SD 10-bit 15pF Cload	DBUS	–	–	22.2	ns	4
			STAT	–	–	22.2	ns	4
		SD 20-bit 15pF Cload	DBUS	–	–	41.0	ns	4
			STAT	–	–	41.0	ns	4
Output Data Rise/Fall Time (1.8V)	t_r/t_f	3G 10-bit 6pF Cload	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.3	ns	1
		All other modes 6pF Cload	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.4	ns	1
		3G 10-bit 15pF Cload	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.1	ns	3
		All other modes 15pF Cload	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.4	ns	3
Output Data Rise/Fall Time (3.3V)	t_r/t_f	3G 10-bit 6pF Cload	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
		All other modes 6pF Cload	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
Output Data Rise/Fall Time (3.3V)	t_r/t_f	3G 10-bit 15pF Cload	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.5	ns	4
		All other modes 15pF Cload	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.4	ns	4

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Digital Input							
Serial Input Data Rate	DR_{SDI}	–	0.27	–	2.97	Gb/s	–
Serial Input Voltage Swing	ΔV_{SDI}	T_A =25°C, differential, 270Mb/s & 1.485Gb/s	720	800	950	mV_{p-p}	6
		T_A =25°C, differential, 2.97Gb/s	720	800	880	mV_{p-p}	6
Achievable Cable Length	–	Belden 1694A cable, 3G	–	150	–	m	–
		Belden 1694A cable, HD	–	230	–	m	–
		Belden 1694A cable, SD	–	440	–	m	–
Input Return Loss	–	single ended	15	21	–	dB	7
Input Resistance	–	single ended	–	1.52	–	kΩ	–
Input Capacitance	–	single ended	–	1	–	pF	–
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	0.27	–	2.97	Gb/s	–
Serial Output Swing	ΔV_{SDO}	Differential with 100Ω load	320	–	600	mVp-p	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	–	–	–	180	ps	–
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	–	–	–	180	ps	–
Serial Output Jitter with loop-through mode	t_{OJ}	SMPTE colour bar 3G, 150m	–	–	100	ps	–
		SMPTE colour bar HD, 250m	–	–	100	ps	–
		SMPTE colour bar SD, 480m	–	–	470	ps	–
Serial Output Duty Cycle Distortion	DCD_{SDD}	3G	–	10	–	ps	–
		HD	–	10	–	ps	–
		SD	–	20	–	ps	–
Synchronous lock time	–	–	–	–	25	µs	–
Asynchronous lock time	–	–	0.1	–	20	ms	–
Lock time from power-up	–	After 20 minutes at -20°C	–	–	5	s	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	60	MHz	5
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	5
GSPI Input Data Setup Time	–		1.5	–	–	ns	5
GSPI Input Data Hold Time	–		1.5	–	–	ns	5
GSPI Output Data Hold Time	–	–	1.5	–	–	ns	5
$\overline{CS}$ low before SCLK rising edge	–	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	5
$\overline{CS}$ high after SCLK falling edge	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	5

Notes:

1. 1.89V and 0°C.
2. 3.47V and 0°C.
3. 1.71V and 85°C
4. 3.13V and 85°C
5. Timing parameters defined in Section 4.19.3
6. 0m cable length
7. Tested on a 2961 board from 5MHz to 3GHz.

3. Input/Output Circuits

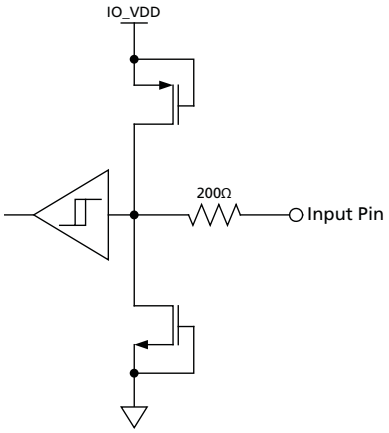

Figure 3-1: Digital Input Pin with Schmitt Trigger (20bit/$\overline{10bit}$, $\overline{CS}$_TMS, SW_EN, IOPROC_EN/$\overline{DIS}$, JTAG/$\overline{HOST}$, $\overline{RC\_BYP}$, $\overline{RESET\_TRST}$, SCLK_TCK, SDIN_TDI, SDO_EN/$\overline{DIS}$, STANDBY, TIM_861)

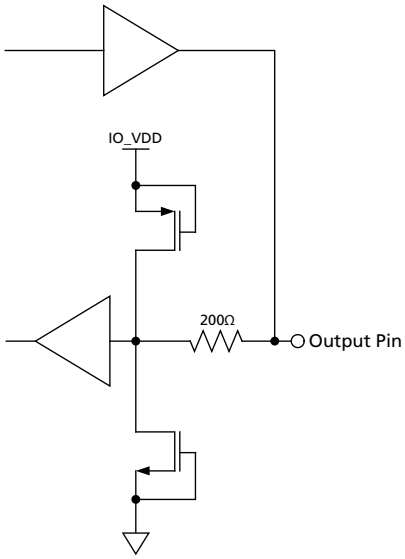

Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (DVB_ASI, $\overline{SMPTE\_BYPASS}$)

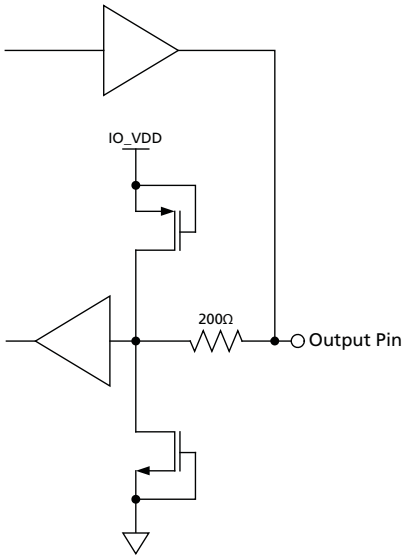

Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output unless in Reset Mode; in which case they are high-impedance. The drive strength can be set by writing to address 06Dh in the host interface register. (DOUT0, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, DOUT6, DOUT7, DOUT8, DOUT9, SDOUT_TDO, STAT0, STAT1, STAT2, STAT3, STAT4, STAT5, XTAL_OUT, DOUT10, DOUT11, DOUT12, DOUT13, DOUT14, DOUT15, DOUT16, DOUT17, DOUT18, DOUT19, PCLK)

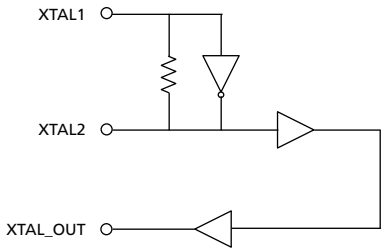

Figure 3-4: XTAL1/XTAL2/XTAL-OUT

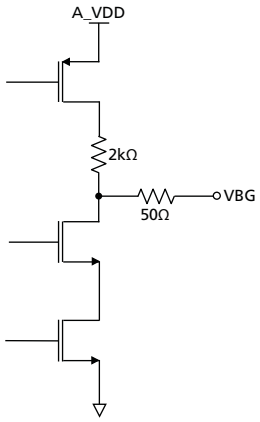

Figure 3-5: VBG

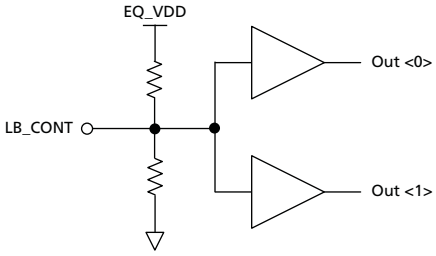

Figure 3-6: LB_CONT

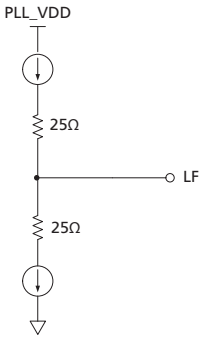

Figure 3-7: Loop Filter