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SEMTECH
GENNUM PRODUCTS

GS2971A

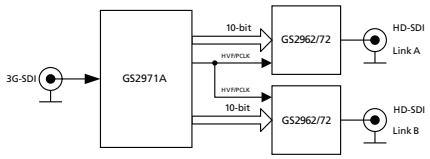
3Gb/s, HD, SD SDI Receiver, with Integrated Adaptive Cable Equalizer complete with SMPTE Audio and Video Processing

Key Features

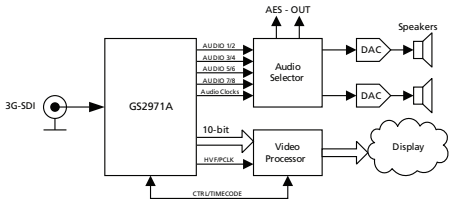
- Operation at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE ST 425 (Level A and Level B), SMPTE ST 424, SMPTE ST 292, SMPTE ST 259-C and DVB-ASI
- Integrated adaptive cable equalizer
- Typical equalized length of Belden 1694A cable:
  - 150m at 2.97Gb/s
  - 250m at 1.485Gb/s
  - 480m at 270Mb/s
- Integrated Reclocker with low phase noise, integrated VCO
- Serial digital reclocked, or non-reclocked output
- Integrated audio de-embedder for 8 channels of 48kHz audio
- Integrated audio clock generator
- Ancillary data extraction
- Optional conversion from SMPTE ST 425 Level B to Level A for 1080p 50/60 4:2:2 10-bit
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 Timing Signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI Host Interface
- -20°C to +85°C operating temperature range
- Low power operation (typically 545mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

Applications

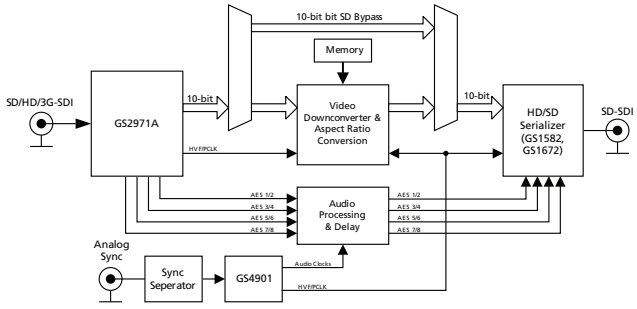
Application: Single Link (3G-SDI) to Dual Link (HD-SDI) Converter



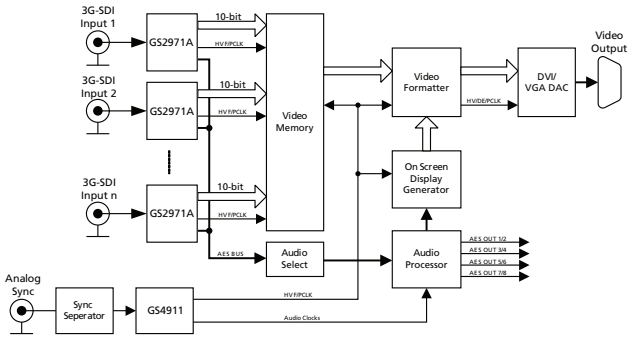
Application: 1080p50/60 Monitor



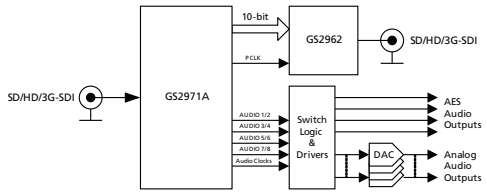
Application: Multi-format Downconverter



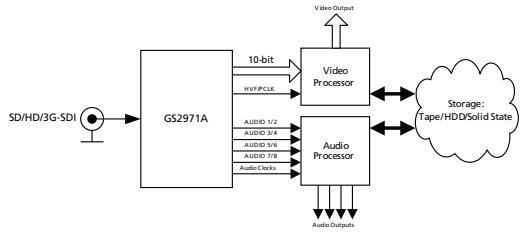
Application: Multi-input Video Monitoring System



Application: Multi-format Audio De-embedder Module



Application: Multi-format Digital VTR/Video Server



Description

The GS2971A is a multi-rate SDI integrated Receiver which includes complete SMPTE processing, as per SMPTE ST 425, SMPTE ST 292 and SMPTE ST 259-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The GS2971A integrates Semtech's adaptive cable equalizer technology, achieving unprecedented cable lengths and jitter tolerance. It features DC restoration to compensate for the DC content of SMPTE pathological signals.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop-through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The serial digital output can be connected to an external cable driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode (the default operating mode), the GS2971A performs full SMPTE processing, and features a number of data integrity checks and measurement capabilities.

The device also supports ancillary data extraction, and can provide entire ancillary data packets through host-accessible registers. It also provides a variety of other packet detection and error handling features. All of these processing features are optional, and may be individually enabled or disabled through register programming.

Both SMPTE ST 425 Level A and Level B inputs are supported with optional conversion from Level B to Level A for 1080p 50/59.94/60 4:2:2 10-bit inputs.

In DVB-ASI mode, sync word detection, alignment and 8b/10b decoding is applied to the received data stream.

In Data-Through mode all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

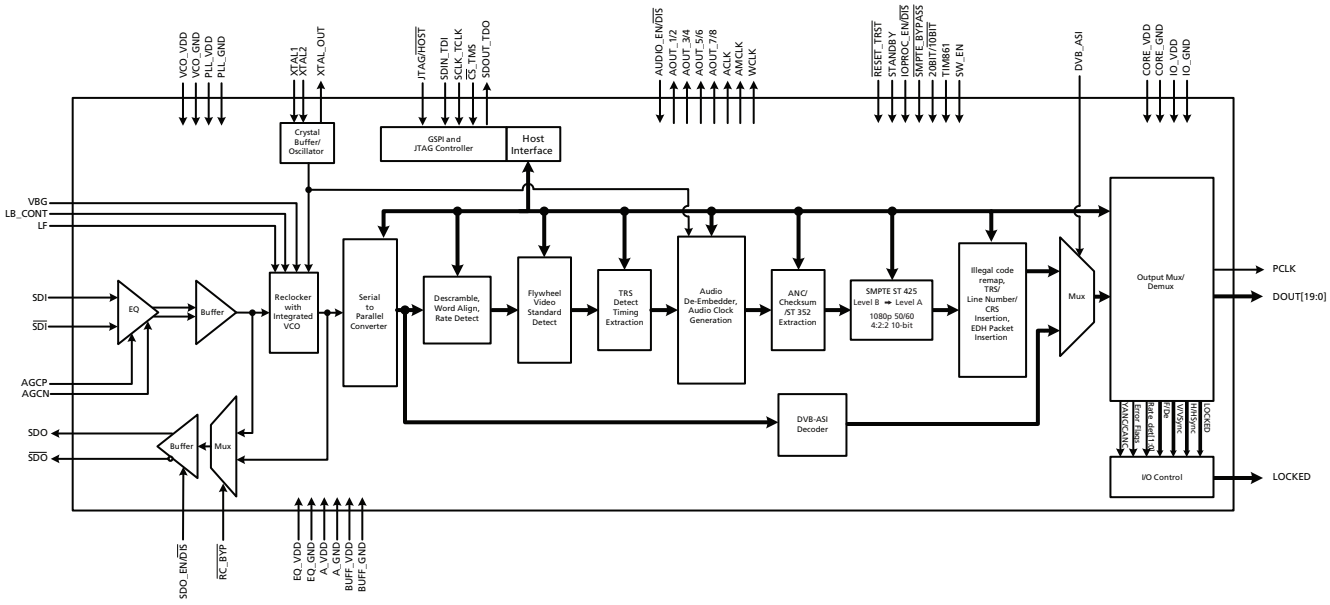
The device can also operate in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static.

Parallel data outputs are provided in 20-bit or 10-bit format for 3Gb/s, HD and SD video rates, with a variety of mapping options. As such, this parallel bus can interface directly with video processor ICs, and output data can be multiplexed onto 10 bits for a low pin count interface.

Up to eight channels (two audio groups) of serial digital audio may be extracted from the video data stream, in accordance with SMPTE ST 272-C and SMPTE ST 299.

The output audio formats supported by the device include AES/EBU and I^2S, and two other industry standard serial digital formats. A variety of audio processing features are provided to ease implementation. Audio clocks are internally generated and provided by the device.

Functional Block Diagram



GS2971A Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
3	014961	–	August 2013	Clarified IOPROC_EN/$\overline{DIS}$ register configuration throughout Section 4. Added note to Section 4.20. Updated SMPTE format throughout document.
2	158578	–	September 2012	Added back the Typ column in the Table 2-4: AC Electrical Characteristics
1	158083	–	June 2012	Updates throughout the document
0	154391	–	July 2010	New Document

Contents

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List of Tables

1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_ VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	A_VDD	PLL_ VDD	RSV	VCO_ GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	A_GND	PLL_ VDD	PLL_ VDD	STAT4	STAT5	$\overline{\text{RESET}}$ _$\overline{\text{TRST}}$	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	A_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SW_EN	JTAG/ $\overline{\text{HOST}}$	IO_GND	IO_VDD
E	EQ_VDD	EQ_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SDOUT_ TDO	SDIN_ TDI	DOUT10	DOUT11
F	AGCP	RSV	A_GND	PLL_ GND	CORE _GND	CORE _VDD	$\overline{\text{CS}}$_ TMS	SCLK_ TCK	DOUT8	DOUT9
G	AGCN	A_GND	$\overline{\text{RC\_BYP}}$	CORE _GND	CORE _GND	CORE _VDD	$\overline{\text{SMPTE}}$_ $\overline{\text{BYPASS}}$	DVB_ASI	IO_GND	IO_VDD
H	BUFF_ VDD	BUFF_ GND	AUDIO_ EN/$\overline{\text{DIS}}$	WCLK	TIM_861	XTAL_ OUT	20bit/ $\overline{\text{10bit}}$	IOPROC_ EN/$\overline{\text{DIS}}$	DOUT6	DOUT7
J	SDO	SDO_ EN/$\overline{\text{DIS}}$	AOUT _1/2	ACLK	AOUT _5/6	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STANDBY	AOUT _3/4	AMCLK	AOUT _7/8	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Description

Pin Number	Name	Type	Description
A1	VBG	Analog Input	Band Gap voltage filter connection.
A2	LF	Analog Input	Loop Filter component connection.
A3	LB_CONT	Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD	Input Power	POWER pin for the VCO. Connect to a 1.2V±5% analog supply followed by a RC filter (see 5.3 Typical Application Circuit). A 105Ω 1% resistor must be used in the RC filter circuit. VCO_VDD is nominally 0.7V.

Table 1-1: Pin Description (Continued)

<table>
<tr><th>Pin Number</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A5, A6, B5, B6, C5, C6</td><td>STAT[0:5]</td><td>Output</td><td>MULTI-FUNCTIONAL OUTPUT PORT.
Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
Each of the STAT [0:5] pins can be configured individually to output one of the following signals:
<table><tr><td>Signal</td><td>Default</td></tr><tr><td>H/HSYNC</td><td>STAT0</td></tr><tr><td>V/VSYNC</td><td>STAT1</td></tr><tr><td>F/DE</td><td>STAT2</td></tr><tr><td>LOCKED</td><td>STAT3</td></tr><tr><td>Y/1ANC</td><td>STAT4</td></tr><tr><td>C/2ANC</td><td>–</td></tr><tr><td>$\overline{\text{DATA ERROR}}$</td><td>STAT5</td></tr><tr><td>$\overline{\text{VIDEO ERROR}}$</td><td>–</td></tr><tr><td>$\overline{\text{AUDIO ERROR}}$</td><td>–</td></tr><tr><td>EDH DETECTED</td><td>–</td></tr><tr><td>CARRIER DETECT</td><td>–</td></tr><tr><td>RATE_DET0</td><td>–</td></tr><tr><td>RATE_DET1</td><td>–</td></tr></table></td></tr>
<tr><td>A7, D10, G10, K7</td><td>IO_VDD</td><td>Input Power</td><td>POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.</td></tr>
<tr><td>A8</td><td>PCLK</td><td>Output</td><td>PARALLEL DATA BUS CLOCK
Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
<table><tr><td>3G 10-bit or 20-bit mode</td><td>PCLK @ 148.5 or 148.5/1.001MHz</td></tr><tr><td>HD 10-bit mode</td><td>PCLK @ 148.5 or 148.5/1.001MHz</td></tr><tr><td>HD 20-bit mode</td><td>PCLK @ 74.25 or 74.25/1.001MHz</td></tr><tr><td>SD 10-bit mode</td><td>PCLK @ 27MHz</td></tr><tr><td>SD 20-bit mode</td><td>PCLK @ 13.5MHz</td></tr></table></td></tr>
</table>

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description	
A9, A10, B8, B9, B10,C8, C9, C10, E9, E10	DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11	Output	PARALLEL DATA BUS Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.	
			20-bit mode 20bit/$\overline{10bit}$ = HIGH	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Luma data output for SD and HD data rates; Data Stream 1 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
			10-bit mode 20bit/$\overline{10bit}$ = LOW	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1&2 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): 8b/10b decoded DVB-ASI data Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
B1	A_VDD	Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.	
B2, C3, C4	PLL_VDD	Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.	
B3, F2	RSV		These pins must be left unconnected.	
B4	VCO_GND	Input Power	GND pin for the VCO. Connect to analog GND.	
B7, D9, G9, J7	IO_GND	Input Power	GND connection for digital I/O. Connect to digital GND.	
C1, D1	SDI, $\overline{SDI}$	Analog Input	Serial Digital Differential Input.	
C2, D2, D3, E3, F3, G2	A_GND	Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.	
C7	$\overline{RESET\_TRST}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG/$\overline{HOST}$ = LOW): When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG/$\overline{HOST}$ = HIGH): When LOW, all functional blocks are set to default and the JTAG test sequence is reset. When HIGH, normal operation of the JTAG test sequence resumes after $\overline{RESET\_TRST}$ is de-asserted.	

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description
D4, E4, F4	PLL_GND	Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G4, G5	CORE_GND	Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD	Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	SW_EN	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable switch-line locking, as described in Section 4.10.1.
D8	JTAG/$\overline{\text{HOST}}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select JTAG test mode or host interface mode. When JTAG/$\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/$\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes.
E1	EQ_VDD	Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	EQ_GND	Input Power	GND pin for SDI buffer. Connect to analog GND.
E7	SDOUT_TDO	Output	COMMUNICATION SIGNAL OUTPUT Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. GSPI serial data output/test data out. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test results from the device. In host interface mode, this pin is used to read status and configuration data from the device.
E8	SDIN_TDI	Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. GSPI serial data in/test data in. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test data into the device. In host interface mode, this pin is used to write address and configuration data words into the device.
F1, G1	AGCP, AGCN		Automatic Gain Control for the equalizer. Attach the AGC capacitor between these pins.
F7	$\overline{\text{CS}}$_TMS	Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Chip select / test mode start. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test. In host interface mode (JTAG/$\overline{\text{HOST}}$ = LOW), this pin operates as the host interface chip select and is active LOW.

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description	
F8	SCLK_TCK	Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Serial data clock signal. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is the JTAG clock. In host interface mode (JTAG/$\overline{\text{HOST}}$ = LOW), this pin is the host interface serial bit clock. All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.	
F9, F10, H9, H10, J8, J9, J10, K8, K9, K10	DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3	Output	PARALLEL DATA BUS Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.	
			20-bit mode 20bit/$\overline{\text{10bit}}$ = HIGH	SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB_ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for 3G data rate DVB-ASI mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output
			10-bit mode 20bit/$\overline{\text{10bit}}$ = LOW	Forced LOW
G3	$\overline{\text{RC\_BYP}}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.	
G7	$\overline{\text{SMPTE\_BYPASS}}$	Input/Output	CONTROL SIGNAL INPUT/OUTPUT Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Indicates the presence of valid SMPTE data. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{\text{SMPTE\_BYPASS}}$ is HIGH when the device locks to a SMPTE compliant input. $\overline{\text{SMPTE\_BYPASS}}$ is LOW under all other conditions. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is LOW, this pin is an INPUT: No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ is set HIGH, the device carries out SMPTE scrambling and I/O processing. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode.	

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description
G8	DVB_ASI	Input/Output	CONTROL SIGNAL INPUT Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable/disable DVB-ASI data extraction in manual mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is LOW, this pin is an input and when the DVB_ASI pin is set HIGH the device will carry out DVB_ASI data extraction and processing. The $\overline{\text{SMPTE\_BYPASS}}$ pin must be set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is HIGH (default), DVB-ASI is configured as a status output (set LOW), and DVB-ASI input streams are not supported or recognized.
H1	BUFF_VDD	Input Power	POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND	Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H3	AUDIO_EN/$\overline{\text{DIS}}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Enables or disables audio extraction.
H4	WCLK	Output	48kHz word clock for Audio. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
H5	TIM_861	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select CEA-861 timing mode. When TIM_861 is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.
H6	XTAL_OUT	Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.
H7	20bit/$\overline{\text{10bit}}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select the output bus width. HIGH = 20-bit, LOW = 10-bit.
H8	IOPROC_EN/$\overline{\text{DIS}}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable or disable audio and video processing features. When IOPROC_EN is HIGH, the audio and video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description
J1, K1	SDO, $\overline{\text{SDO}}$	Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN/$\overline{\text{DIS}}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable/disable the serial digital output stage. When SDO_EN/$\overline{\text{DIS}}$ is LOW, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH. When SDO_EN/$\overline{\text{DIS}}$ is HIGH, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are enabled.
J3	AOUT_1/2	Output	Serial Audio Output; Channels 1 and 2. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
J4	ACLK	Output	64fs sample clock for audio. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
J5	AOUT_5/6	Output	Serial Audio Output; Channels 5 and 6. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
J6, K6	XTAL2, XTAL1	Analog Input	Input connection for 27MHz crystal.
K2	STANDBY	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH.
K3	AOUT_3/4	Output	Serial Audio Output; Channels 3 and 4. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
K4	AMCLK	Output	Oversampled master clock for audio (128fs, 256fs, 512fs selectable). Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
K5	AOUT_7/8	Output	Serial Audio Output; Channels 7 and 8. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (EQ_VDD, BUFF_VDD, A_VDD)	-0.3V to +4.0V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Operating Temperature Range	-20°C to +85°C
Functional Temperature Range	-40°C to +85°C
Storage Temperature Range	-50°C to +125°C
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

Note:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

T_A = -20°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	1
Supply Voltage, Serial Digital Input	EQ_VDD	–	3.13	3.3	3.47	V	1
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	1

Note:

1. The 3.3V supplies must track the 3.3V supply of an external CD.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10bit 3G	–	220	265	mA	–
		20bit 3G	–	210	265	mA	–
		10/20bit HD	–	170	220	mA	–
		10/20bit SD	–	140	185	mA	–
		DVB_ASI	–	130	170	mA	–
+1.8V Supply Current	I_{1V8}	10bit 3G	–	37	45	mA	–
		20bit 3G	–	16	20	mA	–
		10/20bit HD	–	15	21	mA	–
		10/20bit SD	–	4	7	mA	–
		DVB_ASI	–	4	6	mA	–
+3.3V Supply Current	I_{3V3}	10bit 3G	–	150	180	mA	–
		20bit 3G	–	115	130	mA	–
		10/20bit HD	–	110	135	mA	–
		10/20bit SD	–	90	100	mA	–
		DVB_ASI	–	90	95	mA	–
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10bit 3G	–	560	680	mW	–
		20bit 3G	–	525	640	mW	–
		10/20bit HD	–	480	590	mW	–
		10/20bit SD	–	420	520	mW	–
		DVB_ASI	–	410	500	mW	–
		Reset	–	390	–	mW	–
		Standby	–	23	45	mW	–
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10bit 3G	–	750	930	mW	–
		20bit 3G	–	620	760	mW	–
		10/20bit HD	–	570	730	mW	–
		10/20bit SD	–	460	560	mW	–
		DVB_ASI	–	440	540	mW	–
		Reset	–	410	–	mW	–
		Standby	–	23	45	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VSS -0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD +0.3	V	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output Logic LOW	V_{OL}	IOL = 5mA, 1.8V operation	–	–	0.2	V	–
		IOL = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOH = 5mA, 1.8V operation	1.4	–	–	V	–
		IOH = 8mA, 3.3V operation	2.4	–	–	V	–
Serial Input							
Serial Input Common Mode Voltage	–	75Ω load	–	2.2	–	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD -(0.6/2)	BUFF_VDD -(0.45/2)	BUFF_VDD -(0.35/2)	V	–

Note:

The output drive strength of the digital outputs can be programmed through the host interface. please see Table 4-29: Video Core Configuration and Status Registers, register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency: AUDIO_EN = 1, SMPTE mode, IOPROC_EN = 1	–	3G (Level A)	80	–	83	PCLK	–
		3G (Level B)	143	–	151	PCLK	–
		HD	80	–	83	PCLK	–
		SD	50	–	55	PCLK	–
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 1	–	3G (Level A)	44	–	48	PCLK	–
		3G (Level B)	108	–	116	PCLK	–
		HD	44	–	48	PCLK	–
		SD	44	–	48	PCLK	–
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 0	–	3G (Level A)	33	–	36	PCLK	–
		HD	33	–	36	PCLK	–
		SD	32	–	35	PCLK	–
Device Latency: AUDIO_EN = 0, SMPTE bypass, IOPROC_EN = 0	–	3G (Level A)	6	–	9	PCLK	–
		HD	6	–	9	PCLK	–
		SD	5	–	9	PCLK	–
Device Latency: DVB-ASI	–	SD	12	–	16	PCLK	–
Reset Pulse Width	t_{reset}	–	1	–	–	ms	–
Parallel Output							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Hold Time (1.8V)	t_{oh}	3G 10-bit 6pF C_{LOAD}	SPI	1.5	–	–	ns	1
			AUDIO	1.5	–	–	ns	1
			DBUS	0.3	–	–	ns	1
			STAT	0.3	–	–	ns	1
		3G 20-bit 6pF C_{LOAD}	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		HD 10-bit 6pF C_{LOAD}	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		HD 20-bit 6pF C_{LOAD}	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		SD 10-bit 6pF C_{LOAD}	DBUS	19.4	–	–	ns	1
			STAT	19.4	–	–	ns	1
		SD 20-bit 6pF C_{LOAD}	DBUS	38.0	–	–	ns	1
			STAT	38.0	–	–	ns	1
Output Data Hold Time (3.3V)	t_{oh}	3G 10-bit 6pF C_{LOAD}	SPI	1.5	–	–	ns	2
			AUDIO	1.5	–	–	ns	2
			DBUS	0.3	–	–	ns	2
			STAT	0.3	–	–	ns	2
		3G 20-bit 6pF C_{LOAD}	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		HD 10-bit 6pF C_{LOAD}	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		HD 20-bit 6pF C_{LOAD}	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		SD 10-bit 6pF C_{LOAD}	DBUS	19.4	–	–	ns	2
			STAT	19.4	–	–	ns	2
		SD 20-bit 6pF C_{LOAD}	DBUS	38.0	–	–	ns	2
			STAT	38.0	–	–	ns	2

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Delay Time (1.8V)	t_{od}	3G 10-bit 15pF C_{LOAD}	SPI	–	–	14.0	ns	3
			AUDIO	–	–	7.0	ns	3
			DBUS	–	–	1.8	ns	3
			STAT	–	–	2.5	ns	3
		3G 20-bit 15pF C_{LOAD}	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		HD 10-bit 15pF C_{LOAD}	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		HD 20-bit 15pF C_{LOAD}	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		SD 10-bit 15pF C_{LOAD}	DBUS	–	–	22.2	ns	3
			STAT	–	–	22.2	ns	3
		SD 20-bit 15pF C_{LOAD}	DBUS	–	–	41.0	ns	3
			STAT	–	–	41.0	ns	3
Output Data Delay Time (3.3V)	t_{od}	3G 10-bit 15pF C_{LOAD}	SPI	–	–	14.0	ns	4
			AUDIO	–	–	7.0	ns	4
			DBUS	–	–	1.9	ns	4
			STAT	–	–	2.2	ns	4
		3G 20-bit 15pF C_{LOAD}	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		HD 10-bit 15pF C_{LOAD}	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		HD 20-bit 15pF C_{LOAD}	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		SD 10-bit 15pF C_{LOAD}	DBUS	–	–	22.2	ns	4
			STAT	–	–	22.2	ns	4
		SD 20-bit 15pF C_{LOAD}	DBUS	–	–	41.0	ns	4
			STAT	–	–	41.0	ns	4

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Rise/Fall Time (1.8V)	t_r/t_f	3G 10-bit 6pF C_{LOAD}	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.3	ns	1
			AUDIO	–	–	0.6	ns	1
		All other modes 6pF C_{LOAD}	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.4	ns	1
			AUDIO	–	–	0.6	ns	1
		3G 10-bit 15pF C_{LOAD}	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.1	ns	3
			AUDIO	–	–	2.3	ns	3
		All other modes 15pF C_{LOAD}	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.4	ns	3
			AUDIO	–	–	2.3	ns	3
Output Data Rise/Fall Time (3.3V)	t_r/t_f	3G 10-bit 6pF C_{LOAD}	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
			AUDIO	–	–	0.6	ns	2
		All other modes 6pF C_{LOAD}	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
			AUDIO	–	–	0.6	ns	2
Output Data Rise/Fall Time (3.3V)	t_r/t_f	3G 10-bit 15pF C_{LOAD}	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.5	ns	4
			AUDIO	–	–	2.2	ns	4
		All other modes 15pF C_{LOAD}	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.4	ns	4
			AUDIO	–	–	2.2	ns	4
Serial Digital Input								
Serial Input Data Rate	DR_{SDI}	–		0.27	–	2.97	Gb/s	–
Serial Input Voltage Swing	ΔV_{SDI}	T_A =25°C, differential, 270Mb/s & 1.485Gb/s		720	800	950	mV_{p-p}	6
		T_A =25°C, differential, 2.97Gb/s		720	800	880	mV_{p-p}	6
Achievable Cable Length	–	Belden 1694A cable, 3G		–	150	–	m	–
		Belden 1694A cable, HD		–	230	–	m	–
		Belden 1694A cable, SD		–	460	–	m	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Return Loss	–	single ended	15	21	–	dB	7
Input Resistance	–	single ended	–	1.52	–	kΩ	–
Input Capacitance	–	single ended	–	1	–	pF	–
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	0.27	–	2.97	Gb/s	–
Serial Output Swing	ΔV_{SDO}	Differential with 100Ω load	320	–	600	mV_{p-p}	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	–	–	–	180	ps	–
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	–	–	–	180	ps	–
Serial Output Jitter with loop-through mode	t_{OJ}	3G, PRBS23, Belden 1694A cable, 140m	–	–	100	ps	–
		HD, PRBS23, Belden 1694A cable, 210m	–	–	100	ps	–
		SD, PRBS23, Belden 1694A cable, 440m	–	–	470	ps	–
Serial Output Duty Cycle Distortion	DCD_{SDD}	3G	–	10	–	ps	–
		HD	–	10	–	ps	–
		SD	–	20	–	ps	–
Synchronous lock time	–	–	–	–	25	µs	–
Asynchronous lock time	–	–	0.1	–	20	ms	–
Lock time from power-up	–	After 20 minutes at -20°C	–	–	5	s	–
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	60	MHz	5
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	5
GSPI Input Data Setup Time	–		1.5	–	–	ns	5
GSPI Input Data Hold Time	–		1.5	–	–	ns	5
GSPI Output Data Hold Time	–		1.5	–	–	ns	5
$\overline{CS}$ low before SCLK rising edge	–		1.5	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–		37.1	–	–	ns	5

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	5
$\overline{CS}$ high after SCLK falling edge	–		37.1	–	–	ns	5

Notes:

1. 1.89V and 0ºC.
2. 3.47V and 0ºC.
3. 1.71V and 85ºC
4. 3.13V and 85ºC
5. Timing parameters defined in Section 4.20.3
6. 0m cable length
7. Tested on a 2971 board from 5MHz to 3GHz.

3. Input/Output Circuits

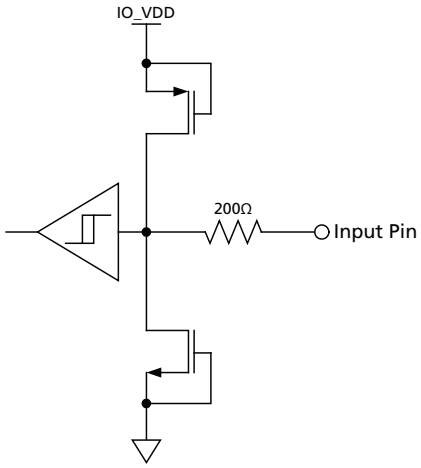

Figure 3-1: Digital Input Pin with Schmitt Trigger (20BIT/$\overline{10BIT}$, AUDIO_EN/$\overline{DIS}$, $\overline{CS}$_TMS, SW_EN, IOPROC_EN/$\overline{DIS}$, JTAG/$\overline{HOST}$, $\overline{RC\_BYP}$, $\overline{RESET\_TRST}$, SCLK_TCK, SDIN_TDI, SDO_EN/$\overline{DIS}$, STANDBY, TIM_861)

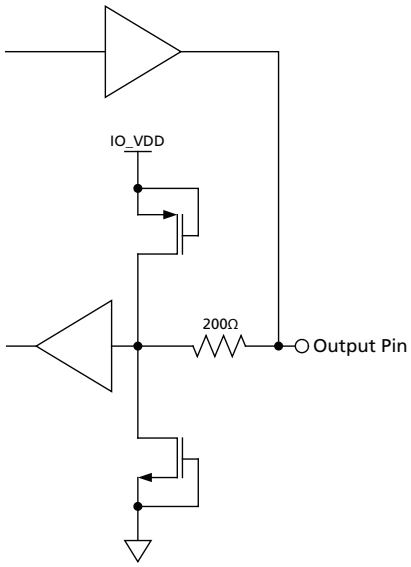

Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (ACLK, AMCLK, AOUT_1/2, AOUT_3/4, AOUT_5/6, AOUT_7/8, DVB_ASI, $\overline{SMPTE\_BYPASS}$, WCLK)