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SEMTECH
GENNUM PRODUCTS

GS2985

GS2985 Multi-Rate SDI Reclocker with Equalization & De-emphasis

Features

- SMPTE 424M, SMPTE 292M and SMPTE 259M-C compliant
- Supports DVB-ASI at 270Mb/s
- Single supply operation at 3.3V or 2.5V
- 180mW typical power consumption (210mW with RCO enabled) at 2.5V
- Input signal equalization and output-signal de-emphasis settings to compensate for board-trace dielectric losses
- 4:1 input multiplexer patented technology
- Choice of dual reclocked data outputs or one reclocked data output and one clock output
- Uses standard 27MHz crystal
- Cascadable crystal buffer supports multiple reclockers using a single crystal
- Differential inputs and outputs
  - support DC coupling to industry-standard differential logic
  - on-chip 100Ω differential data input/output termination
  - selectable 400mVppd or 800mVppd output swing on each output
  - seamless interface to other Gennum products
- 4 wire SPI host interface for device configuration and monitoring
- Standard logic control and status signal levels
- Auto and Manual modes for rate selection
- Standards indication in Auto mode
- Lock Detect Output
- Mute, Bypass and Autobypass functions
- SD/$\overline{\text{HD}}$ indication output to control GS2978 or GS2988 dual slew-rate cable drivers
- Operating temperature range: -40°C to +85°C
- Small footprint QFN package (9mm x 9mm)
  - Package-compatible with GS2975A
- Pb-free and RoHS compliant

Applications

- SMPTE 424M, SMPTE 292M and SMPTE 259M-C coaxial cable serial digital interfaces

Description

The GS2985 is a multi-rate serial digital reclocker designed to automatically recover the embedded clock from a digital video signal and retime the incoming video data. It will recover the embedded clock signal and retime the data from a SMPTE 424M, SMPTE 292M, or SMPTE 259M-C compliant digital video signal.

A serial host interface provides the ability to configure and monitor multiple GS2985 devices in a daisy-chain configuration.

Adjustable input trace equalization (EQ) for up to 40" of FR4 trace losses, and adjustable output de-emphasis (DE) for up to 20" of FR4 trace losses, can be configured via the host interface.

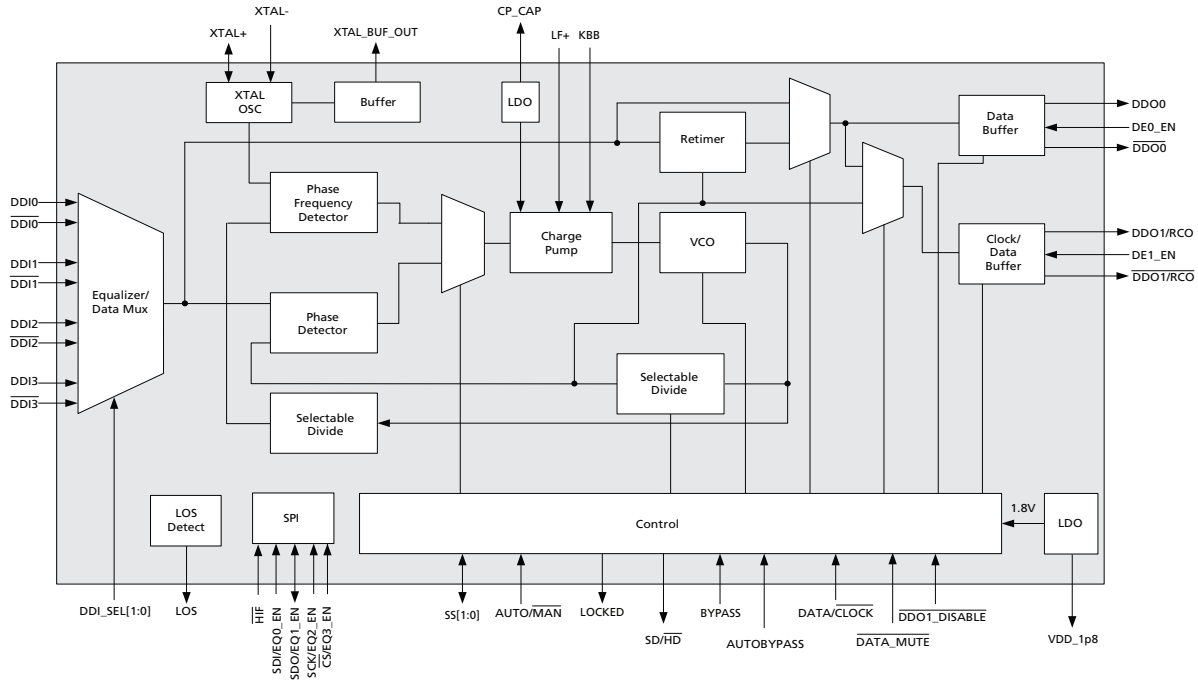
The GS2985 can operate in either auto or manual rate selection mode. In Auto mode, the device will automatically detect and lock onto incoming SMPTE SDI data signals at any supported rate. For single rate data systems, the GS2985 can be configured to operate in Manual mode. In both modes, the device requires only one external crystal to set the VCO frequency when not locked and provides adjustment free operation.

The GS2985 accepts industry-standard differential input levels including LVPECL and CML. The differential data and clock outputs feature selectable output swing via the host interface, ensuring compatibility with most industry-standard, terminated differential receivers.

The GS2985 features dual differential outputs. The second output can be configured to emit either the recovered clock signal or the re-timed video data. This output can also be disabled to save power.

In systems which require passing of non-SMPTE data rates, the GS2985 can be configured to either automatically or manually enter a bypass mode in order to pass the signal without reclocking.

The GS2985 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant. This component and all homogeneous sub-components are RoHS compliant.



GS2985 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
5	158296	–	July 2012	Removed jumper from Figure 5-1: GS2985 Typical Application Circuit.
4	158127	–	May 2012	Corrected 4.15.3 section to make it easier to follow and changed to Semtech Template.
3	158063	–	May 2012	Corrected DRIVER_1 [7:5] Function Description in Table 4-12: Host Register Map
2	153705	–	March 2010	Converted to Data Sheet. Updated Power numbers in Table 2-1: DC Electrical Characteristics. Added Table 4-5: Suggested LOS Threshold Settings.
1	152592	–	September 2009	Updates to Section 4.15 Host Interface.
0	152329	–	July 2009	Converted document to Preliminary Data Sheet.
D	152240	–	July 2009	Added Figure 4-2: De-emphasis Waveform.
C	152042	–	June 2009	Removed 'Proprietary & Confidential" from document.

Version	ECR	PCN	Date	Changes and/or Modifications
B	151967	–	May 2009	Added Section 4.15 Host Interface.
A	151318	–	April 2009	New document.

Contents

1. Pin Out

1.1 Pin Assignment

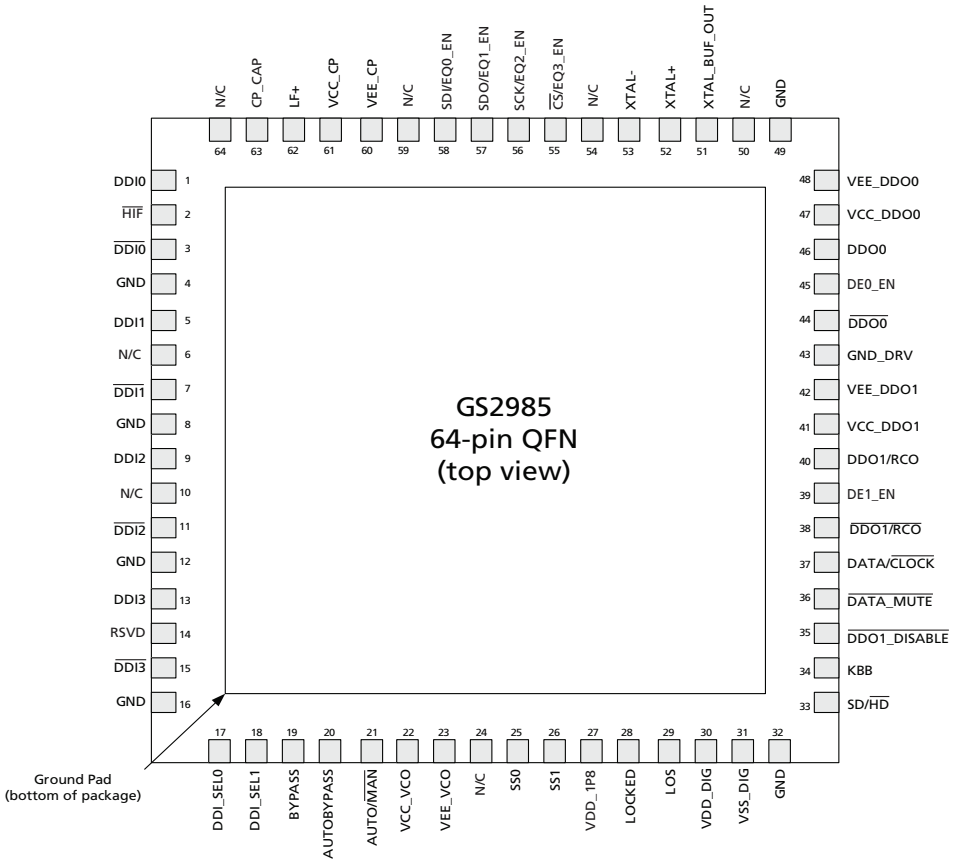


Figure 1-1: GS2985 Pin Out

1.2 Pin Descriptions

Table 1-1: GS2985 Pin Descriptions

Pin Number	Name	Type	Description
1, 3	DDI0, $\overline{\text{DDI0}}$	Input	Serial Digital Differential Input 0.
2	$\overline{\text{HIF}}$	Logic Input	Host interface selection pin. Active-low input. See Section 4.15.14.
4, 8, 12, 16, 32, 49	GND	Power	Connect to GND.
5, 7	DDI1, $\overline{\text{DDI1}}$	Input	Serial Digital Differential Input 1.
6, 10, 24, 50, 54, 59, 64	N/C	No Connect	Do not connect.
9, 11	DDI2, $\overline{\text{DDI2}}$	Input	Serial Digital Differential Input 2.
13, 15	DDI3, $\overline{\text{DDI3}}$	Input	Serial Digital Differential Input 3.
14	RSVD	Reserved	Reserved pin. Do not connect to this pin.
17, 18	DDI_SEL[0:1]	Logic Input	Selects one of four serial digital input signals for processing. See Section 4.4.
19	BYPASS	Logic Input	Bypasses the reclocker stage. See Section 4.12.
20	AUTOBYPASS	Logic Input	When HIGH, this pin automatically bypasses the reclocker stage when the PLL is not locked to a supported rate. See Section 4.12.
21	AUTO/$\overline{\text{MAN}}$	Logic Input	When set HIGH, the standard is automatically detected from the input data rate.
22	VCC_VCO	Power	Most positive power supply connection for the internal VCO section. Connect to a 3.3V supply with a 422Ω resistor, or to a 2.5V supply with a 267Ω resistor.
23	VEE_VCO	Power	Most negative power supply connection for the internal VCO section. Connect to GND.
25, 26	SS0, SS1	Bi-directional	When AUTO/$\overline{\text{MAN}}$ is HIGH, SS[1:0] are outputs displaying the data rate to which the PLL has locked to. When AUTO/$\overline{\text{MAN}}$ is LOW, SS[1:0] are inputs forcing the PLL to lock only to the selected data rate. See Table 4-8 from Section 4.10.
27	VDD_1P8	Power	External capacitor for internal 1.8V digital supply.
28	LOCKED	Output	Lock Detect status signal. HIGH when the PLL is locked.
29	LOS	Output	Loss Of Signal status. HIGH when the input signal is invalid.
30	VDD_DIG	Power	Most positive power supply connection for the digital core. Connect to 3.3V or 2.5V.
31	VSS_DIG	Power	Most negative power supply for the digital core. Connect to GND.

Table 1-1: GS2985 Pin Descriptions

Pin Number	Name	Type	Description
33	SD/$\overline{HD}$	Output	This signal will be LOW for all rates other than 270Mb/s. This signal is HIGH for 270Mb/s.
34	KBB	Analog Input	Controls the loop bandwidth of the PLL. Leave this pin floating for serial reclocking applications.
35	$\overline{DDO1\_DISABLE}$	Logic Input	Disables the DDO1/RCO and $\overline{DDO1}$/$\overline{RCO}$ outputs when LOW. See Section 4.14.
36	$\overline{DATA\_MUTE}$	Logic Input	Mutes the DDO0/$\overline{DDO0}$ and DDO1/$\overline{DDO1}$ (if data is selected) outputs when LOW. Set HIGH for normal operation.
37	DATA/$\overline{CLOCK}$	Logic Input	DATA/$\overline{CLOCK}$ select. See Section 4.14.
38, 40	$\overline{DDO1/RCO}$, DDO1/RCO	Output	Differential serial clock or data outputs.
39	DE1_EN	Logic Input	De-emphasis on/off pin for serial digital output 1. HIGH = de-emphasis on LOW = de-emphasis off
41	VCC_DDO1	Power	Most positive power supply connection for the DDO1/$\overline{DDO1}$ output driver. Connect to 3.3V or 2.5V.
42	VEE_DDO1	Power	Most negative power supply connection for the DDO1/$\overline{DDO1}$ output driver. Connect to GND.
43	GND_DRV	Power	Connect to GND.
44, 46	$\overline{DDO0}$, DDO0	Output	Differential Serial Digital Outputs.
45	DE0_EN	Logic Input	De-emphasis on/off pin for serial digital output 0. HIGH = de-emphasis on LOW = de-emphasis off
47	VCC_DDO0	Power	Most positive power supply connection for the DDO0/$\overline{DDO0}$ output driver. Connect to 3.3V or 2.5V.
48	VEE_DDO0	Power	Most negative power supply connection for the DDO0/$\overline{DDO0}$ output driver. Connect to GND.
51	XTAL_BUF_OUT	Output	Buffered output of the reference oscillator.
52	XTAL+	Output	Reference crystal output.
53	XTAL-	Input	Reference crystal input.
55	$\overline{CS}$/EQ3_EN	Input/Logic Input	In host mode ($\overline{HIF}$ set LOW): Chip select input for SPI serial host interface. Active-low input. In non-host mode ($\overline{HIF}$ set HIGH): Trace equalization on/off pin for Serial Digital Differential Input 3. Active-high input.

Table 1-1: GS2985 Pin Descriptions

Pin Number	Name	Type	Description
56	SCK/EQ2_EN	Input/Logic Input	In host mode ($\overline{HIF}$ set LOW): Burst-mode clock input for SPI serial host interface. In non-host mode ($\overline{HIF}$ set HIGH): Trace equalization on/off pin for Serial Digital Differential Input 2. Active-high input.
57	SDO/EQ1_EN	Input/Logic Input	In host mode ($\overline{HIF}$ set LOW): Serial digital data output for SPI serial host interface. Active-high output. In non-host mode ($\overline{HIF}$ set HIGH): Trace equalization on/off pin for Serial Digital Differential Input 1. Active-high input.
58	SDI/EQ0_EN	Input/Logic Input	In host mode ($\overline{HIF}$ set LOW): Serial digital data input for SPI serial host interface. Active-high input. In non-host mode ($\overline{HIF}$ set HIGH): Trace equalization on/off pin for Serial Digital Differential Input 0. Active-high input.
60	VEE_CP	Power	Most negative power supply connection for the internal charge pump. Connect to GND.
61	VCC_CP	Power	Most positive power supply connection for the internal charge pump. Connect to 3.3V or 2.5V
62	LF+	Passive	Loop Filter capacitor connection. (CLF = 47nF). Connect as shown in Typical Application Circuit on page 41.
63	CP_CAP	Power	External capacitor for internal LDO regulator supplying the charge pump circuit.
–	Center Pad	–	Ground pad on bottom of package. Connect to GND.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5 to +3.6V_{DC}
Input ESD Voltage	4kV
Storage Temperature Range	-50°C < T_A < 125°C
Operating Temperature Range	-40°C to 85°C
Input Voltage Range	-0.3 to (VCC + 0.3) V_{DC}
Solder Reflow Temperature	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	VDD	3.3V	3.135	3.3	3.465	V
		2.5V	2.375	2.5	2.625	V
Power (DDO1/RCO disabled, minimum output swing)	P	VDD = 3.3V	–	250	325	mW
		VDD = 2.5V	–	180	235	mW
Power (DDO1/RCO enabled, minimum output swing)		VDD = 3.3V	–	290	390	mW
		VDD = 2.5V	–	210	275	mW
Power in Power-down mode		VDD = 3.3V	–	48	60	mW
		VDD = 2.5V	–	30	40	mW
Serial Input Termination	–	Differential	80	100	120	Ω
Serial Output Termination	–	Differential	80	100	120	Ω
Serial Input Common Mode Voltage	–	–	1.6	–	VDD	V
Serial Output Common Mode Voltage	–	–	–	VCC-(∆VOD/2)	–	V
VIL (2.5V operation)	–	VOUT≤VOL, max	-0.3	–	0.7	V
VIL (3.3V operation)		VOUT≤VOL, max	-0.3	–	0.8	V

Table 2-1: DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VIH (2.5V operation)	–	VOUT≥VOH, min	1.7	–	VDD +0.3	V
VIH (3.3V operation)		VOUT≥VOH, min	2	–	VDD +0.3	V
IIN	–	VIN = 0V or VIN = VDD	–	+/-10	+/-20	µA
VOL (2.5V operation)	–	VDD = min, IOL = 100µA	–	–	0.4	V
VOL (3.3V operation)		VDD = min, IOL = 100µA	–	–	0.4	V
VOH (2.5V operation)	–	VDD = min, IOH = -100µA	2.1	–	–	V
VOH (3.3V operation)		VDD = min, IOH = -100µA	VDD -0.4	–	–	V
Hysteresis Voltage (SPI inputs)	–	2.5V operation	–	350	–	mV
		3.3V operation	–	420	–	mV

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate (for reclocking)	DR_{SDO}	–	0.27	–	2.97	Gb/s	–
Serial Input Data Rate (bypass)		–	DC	–	2.97	Gb/s	–
SPI Operating Speed	–	–	–	–	10	MHz	–
Input Voltage Swing	ΔVSDI	set ATTEN_EN = 1 for ΔVSDI>1V_{pp}	100		2000	mV_{p-pd}	–
Output Voltage Swing	ΔVOD	default	300	400	500	mV_{p-pd}	–
		see DRIVER_1 register (0x01) addresses 8 & 9 in 4.15.14 Host Register Map.	600	800	1000	mV_{p-pd}	–
Input Trace Equalization	–	LOW	Recommended setting for 0 to 10 inches of FR4				–
		MED	Recommended setting for 10 to 20 inches of FR4				–
		HIGH	Recommended setting for >20 inches of FR4				–

Table 2-2: AC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output De-Emphasis	–	OFF - 0	–	0	–	dB	–
		ON - 0	–	0	–	dB	–
		ON - 1	–	0.7	–	dB	–
		ON - 2	–	1.3	–	dB	–
		ON - 3	–	2	–	dB	–
		ON - 4	–	2.6	–	dB	–
		ON - 5	–	3.3	–	dB	–
		ON - 6	–	4	–	dB	–
		ON - 7	–	4.7	–	dB	–
Input Jitter Tolerance		square-wave modulated jitter	0.8	–	–	UI	–
Loop Bandwidth	BW_{LOOP} (270Mb/s)	KBB = VCC	–	170	–	kHz	–
		KBB = FLOAT	–	340	–	kHz	–
		KBB = GND	–	680	–	kHz	–
	BW_{LOOP} (1485Mb/s)	KBB = VCC	–	0.875	–	MHz	–
		KBB = FLOAT	–	1.75	–	MHz	–
		KBB = GND	–	3.5	–	MHz	–
	BW_{LOOP} (2970Mb/s)	KBB = VCC	–	1.75	–	MHz	–
		KBB = FLOAT	–	3.5	–	MHz	–
		KBB = GND	–	7.0	–	MHz	–
PLL Lock Time (asynchronous)	t_{alock}	–	–	0.5	1	ms	–
PLL Lock Time (synchronous)	t_{slock}	CLF = 47nF, SD/$\overline{HD}$ = 0	–	0.5	4	µs	–
		CLF = 47nF, SD/$\overline{HD}$ = 1	–	5	10	µs	–
Serial Data Output Jitter Intrinsic (DDO0)	$t_{OJ(270Mb/s)}$	KBB = FLOAT PRN 2^23-1 test pattern	–	0.01	0.02	UI	1
	$t_{OJ(1485Mb/s)}$	KBB = FLOAT PRN 2^23-1 test pattern	–	0.03	0.04	UI	1
	$t_{OJ(2970Mb/s)}$	KBB = FLOAT PRN 2^23-1 test pattern	–	0.05	0.08	UI	1
Output Rise/Fall Time	tr/f	20% to 80% (400mV swing)	–	65	90	ps	–
		20% to 80% (800mV swing)	–	80	110	ps	–
Output Rise/Fall Time Mismatch	–	–	–	–	15	ps	–

Table 2-2: AC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Eye Cross Shift	–	percentage of signal amplitude	–	–	5	%	–
Power Supply Noise Rejection	–	50 - 100Hz	–	100	–	mV_{p-p}	–
		100Hz - 10MHz	–	40	–	mV_{p-p}	–
		10MHz - 1.485GHz	–	10	–	mV_{p-p}	–

Notes:

1. Accumulated jitter measured peak to peak differential over 1000 hits.

3. Input/Output Circuits

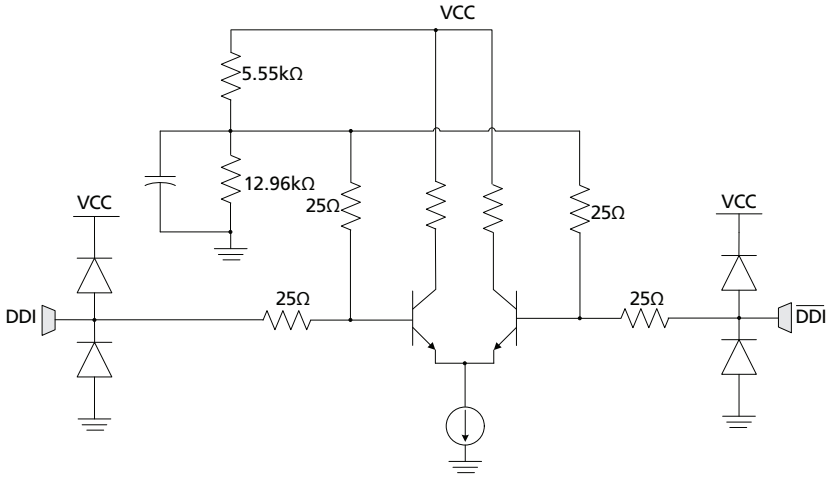


Figure 3-1: High-speed Inputs (DDI0, $\overline{\text{DDI0}}$, DDI1, $\overline{\text{DDI1}}$, DDI2, $\overline{\text{DDI2}}$, DDI3, $\overline{\text{DDI3}}$)

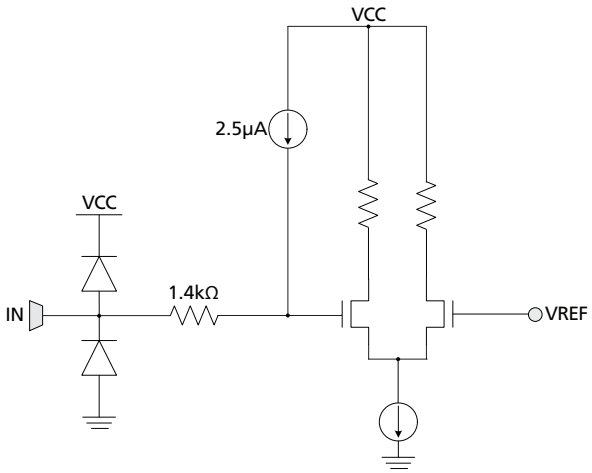


Figure 3-2: Low-speed Input with weak internal pull-up ($\overline{\text{HIF}}$, RSVD, AUTO/$\overline{\text{MAN}}$, $\overline{\text{DDO1\_DISABLE}}$, $\overline{\text{DATA\_MUTE}}$)

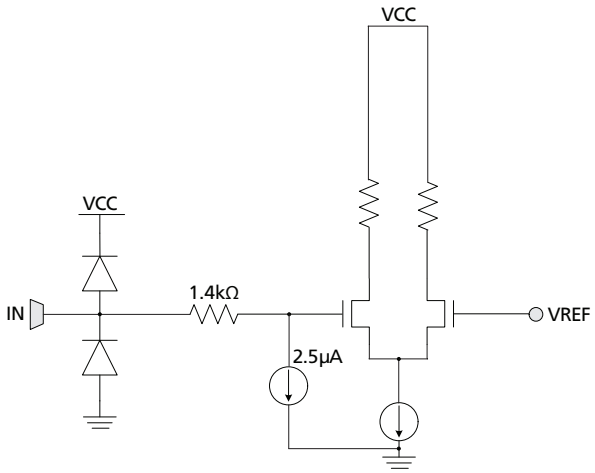


Figure 3-3: Low-speed Input with weak internal pull-down (DDI_SEL0, DDI_SEL1, BYPASS, AUTOBYPASS, DE1_EN, DE0_EN)

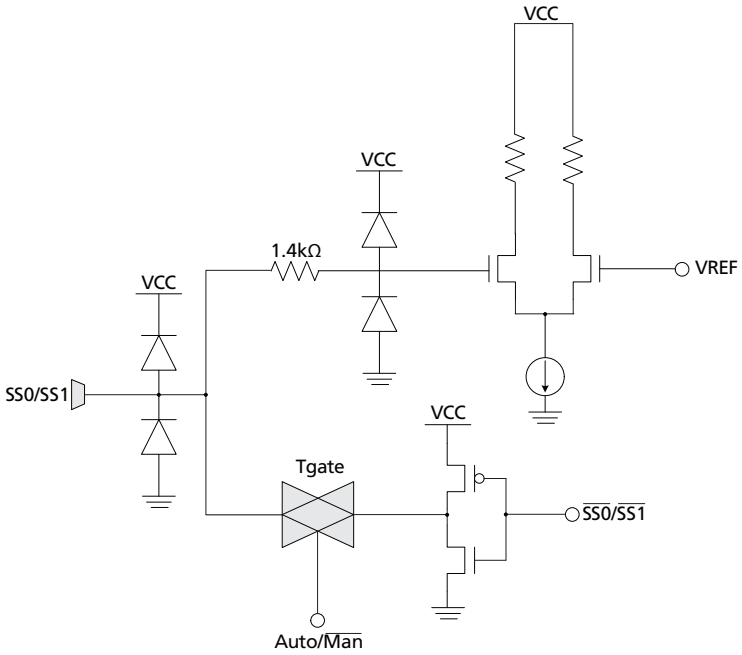


Figure 3-4: Data Rate Control/Indicators (SS0, SS1)

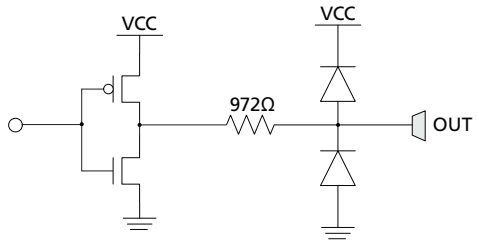


Figure 3-5: Low-speed Outputs (LOCKED, LOS, HD/$\overline{SD}$)

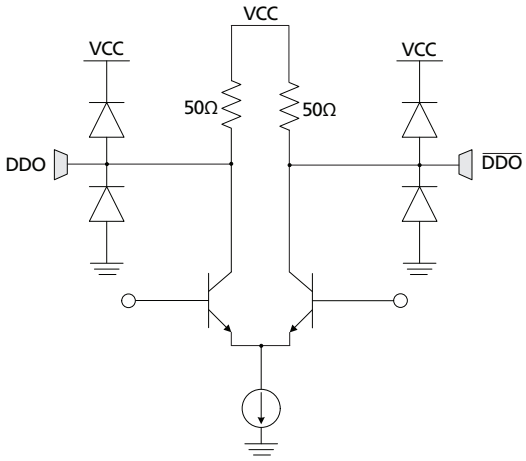


Figure 3-6: High-speed Outputs ($\overline{DDO1}$/$\overline{RCO}$, DDO1/RCO, $\overline{DDO0}$, DDO0)

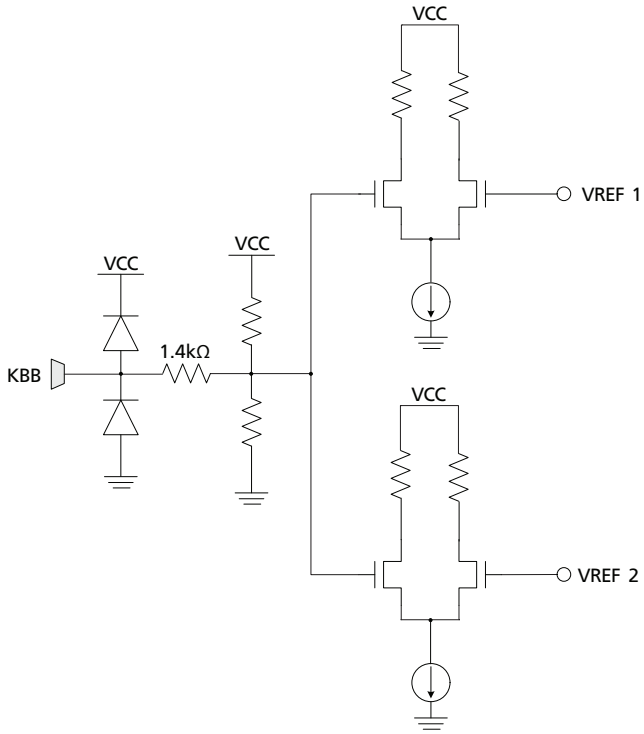


Figure 3-7: Loop Bandwidth Control (KBB)

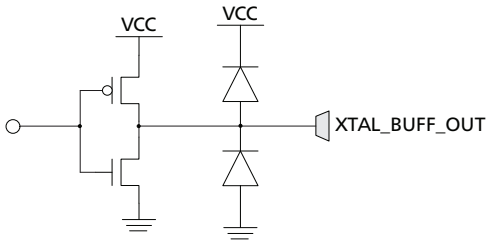


Figure 3-8: Crystal Buffered Output (XTAL_BUF_OUT)

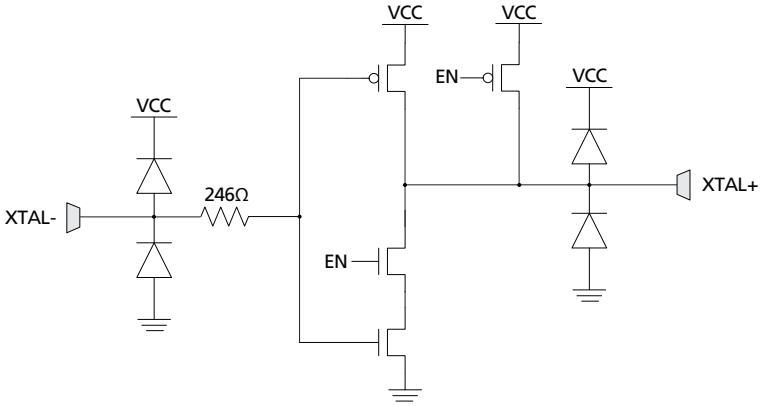


Figure 3-9: High-speed Crystal Oscillator I/O (XTAL-, XTAL+)

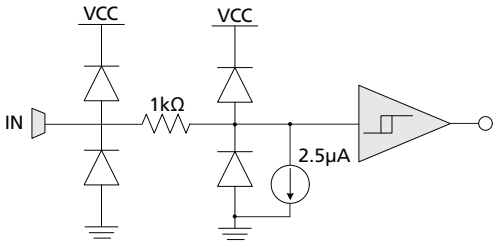


Figure 3-10: SPI Inputs/EQ Ctrl ($\overline{CS}$/EQ3_EN, SCK/EQ2_EN, SDI/EQ0_EN)

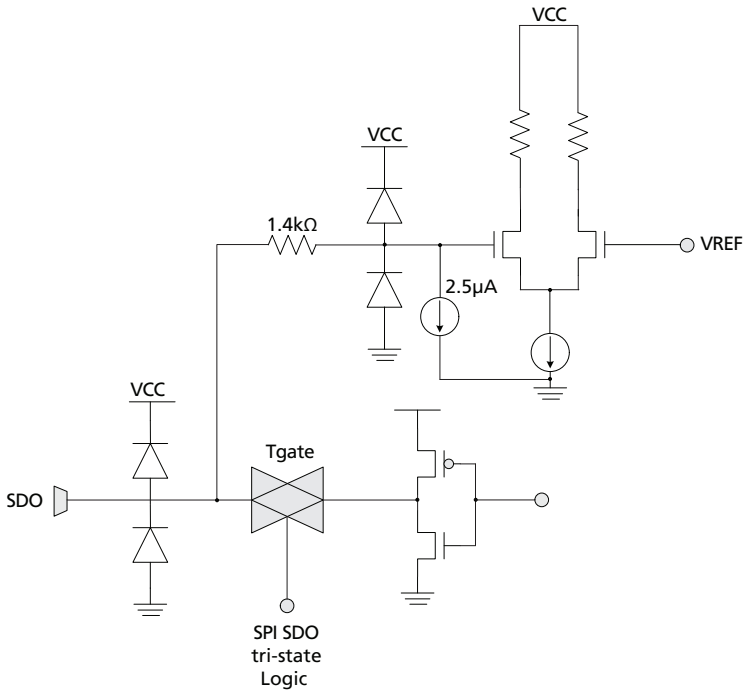


Figure 3-11: SPI Output/EQ Control (SDO/EQ1_EN)

4. Detailed Description

The GS2985 is a multi-standard reclocker for serial digital SDTV signals operating at 270Mb/s, and HDTV signals operating at 1.485Gb/s, 1.485/1.001Gb/s, 2.97Gb/s and 2.97/1.001Gb/s.

4.1 Serial Data Input

The GS2985 features four differential input buffers.

The serial data input signal is connected to the DDI0/$\overline{\text{DDI0}}$, DDI1/$\overline{\text{DDI1}}$, DDI2/$\overline{\text{DDI2}}$ and DDI3/$\overline{\text{DDI3}}$ input pins of the device.

Input signals can be single-ended or differential, DC or AC-coupled.

The input circuit is self-biasing, to allow for simple AC or DC-coupling of input signals to the device.

The serial digital data inputs are also compatible when DC-coupled with LVPECL or CML differential outputs from crosspoint switches which operate from 3.3V or 2.5V supplies. This includes but is not limited to: GS2974A, GS2974B, and GS2984 equalizers.

4.2 Modes of Operation

The GS2985 has two modes of operation: Legacy Mode ($\overline{\text{HIF}}$ = HIGH) and SPI Mode ($\overline{\text{HIF}}$ = LOW).

In Legacy Mode, chip functions are controlled via pins only, and offers limited control of input equalization and output de-emphasis.

In SPI mode, access is gained to additional EQ and DE settings as well as access to additional features such as LOS adjustment, polarity invert, auto-mute, etc.

4.3 Input Trace Equalization

The GS2985 features adjustable trace equalization to compensate for PCB trace dielectric losses at 1.5GHz.

The trace equalization has three peak-gain settings. The maximum peak gain value is optimized for compensating the high-frequency losses associated with 25 inches of 5-mil stripline in FR4 material. For boards with different striplines or materials, users can experiment to find the EQ setting which optimizes their system performance.

These settings are accessible via the serial host interface.

Each serial digital input; DDI, $\overline{\text{DDI}}$ includes a pin EQn_EN to turn its trace equalizer on or off. When a pin EQn_EN is tied LOW or left unconnected, the trace equalization for input n is set to the Low Range.

When an EQn_EN pin is tied HIGH, and input n is selected, the trace equalization for input n is set to the Medium Range.

Table 4-1: Input Trace Equalization Operation

EQn_EN Setting	Trace Equalization Range
LOW	Low
HIGH	Medium

The default peak-gain setting upon power-up is optimized for compensating the high-frequency losses associated with approximately 10 inches of 5-mil stripline in FR4 material.

The EQn_EN pins are multiplexed with the serial host interface pins. The EQn_EN functionality is enabled when pin $\overline{\text{HIF}}$ is tied HIGH, as shown in Table 4-2:

Table 4-2: EQn_EN Pins Multiplexed

Pin	Function
SDI/EQ0_EN	Active-high logic input to enable trace-equalization for high-speed input channel 0.
SDO/EQ1_EN	Active-high logic input to enable trace-equalization for high-speed input channel 1.
SCK/EQ2_EN	Active-high logic input to enable trace-equalization for high-speed input channel 2.
$\overline{\text{CS}}$/EQ3_EN	Active-high logic input to enable trace-equalization for high-speed input channel 3.

4.4 4:1 Input Mux

The GS2985 incorporates a 4:1 input mux, which allows the connection of four independent streams of video/data. There are four differential inputs (DDI[3:0] / $\overline{\text{DDI[3:0]}}$). The active channel can be selected via the DDI_SEL[1:0] pins as shown in Table 4-3.

Table 4-3: Input Selection Table

DDI_SEL[1:0]	Selected Input
00	DDI0
01	DDI1
10	DDI2
11	DDI3

The DDI_SEL pins include internal pull-downs, which pull the input voltage LOW if either pin is unconnected. Active circuitry associated with the input buffers and trace EQ can only be turned on for the selected input. Inputs which are not selected have their input buffers and trace EQs turned OFF to save power. Unused inputs can be either left floating, or tied to VCC.

4.5 Crystal Buffer

The GS2985 features a crystal buffer supporting a Gennum recommended external 27MHz crystal. The GS2985 requires an external 27MHz reference clock for correct operation. This reference clock is generated by connecting a crystal to the XTAL- and XTAL+ pins of the device.

Alternately, a 27MHz external clock source can be connected to the XTAL- pin of the device, while the XTAL+ pin should be left floating.

4.6 LOS (Loss Of Signal) Detection

The LOS (Loss Of Signal) status pin is an active-high output that indicates when the serial digital input signal selected at the 4:1 input mux is invalid. In order for this output to be asserted, transitions must not be present for a period of t_{LA} = 5 - 10µs. After this output has been asserted, LOS will de-assert within t_{LD} = 0 - 5µs after the appearance of a transition at the DDIx input. See Figure 4-1.

This signal is HIGH (signal lost), when the number of data edges within a window is below a defined threshold. The output is automatically muted when LOS is detected.

This signal is LOW (signal valid), when the number of data edges within a window is above a defined threshold. See Table 4-4.

Table 4-4: LOS Operation

LOS	Signal
HIGH	Invalid
LOW	Valid

The LOS function is operational for all operating modes of the device.

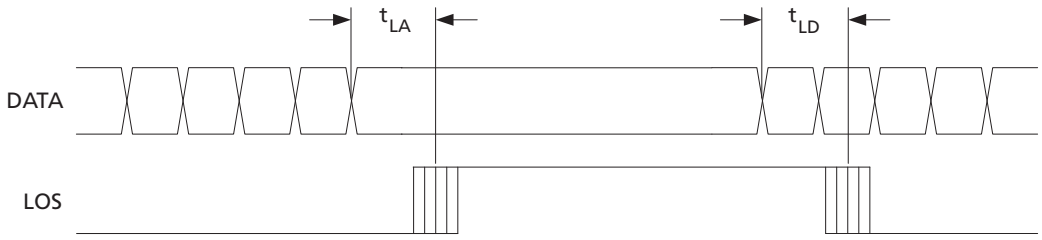


Figure 4-1: LOS Signal Timing

The LOS detector has two major modes. In legacy mode, a simple edge-based detector is used to monitor the received signal at the output of the data slicer. Since the incoming signal has undergone considerable gain by this point, the legacy detector can be more susceptible to false de-assertion of LOS for unused channels which experience significant cross-talk from adjacent active channels.

The new LOS detector uses a measure of both signal amplitude and duration to minimize false detection of the impulse like signals that are characteristic of cross-talk. In this mode, the signal is tapped off at the output of the equalizer stage, prior to the high gain buffers.

The threshold setting within the detector can be adjusted to increase or decrease its sensitivity. Gennum recommends using the least sensitive threshold level. This provides the most margin against false de-assertion of LOS.

Table 4-5: Suggested LOS Threshold Settings

		LOS Detection Method Select	LOS Threshold Adjust
Input Signal Amplitude	>250mV	0x1	0x0
	200mV to 250mV	0x1	0x1
	150mV to 200mV	0x1	0x2
	<150mV	0x1 or 0x0	0x3

The LOS mode can be selected by using the host interface, in register TOP_1 (address 0x02).

4.7 Serial Digital Reclocker

The output of the Equalizer is fed to the reclocker. The function of the reclocker is to re-time the input signal and to generate system clocks.

The reclocker operates at three frequencies; 2.97Gb/s, 1.485Gb/s and 270Mb/s, and provides a minimum input jitter tolerance of 0.8UI to square-wave-modulated jitter at these rates.

When there is no serial input signal, the internal clock maintains a frequency close to the expected incoming data rate, by locking to the external reference crystal.

4.8 Lock Detection

The lock detect block indicates, via the active-high LOCKED signal, when the device has achieved lock to the incoming data stream.

The lock logic within the GS2985 includes a system that monitors the frequency and the phase of the incoming data, as well as a monitor to detect harmonic lock.

Table 4-6: Lock Operation

Lock Signal	Status
HIGH	Locked
LOW	Not locked

The LOCKED output signal is also available via the host interface.

4.8.1 Lock Detect and Asynchronous Lock

The reference crystal is used to assist the PLL in achieving a short lock time. The lock detection algorithm is a continuous process, which begins at device power up or after a system reset, and continues until the device is powered down.

The asynchronous lock time is defined as the time it takes the device to lock when a video signal is first applied to the serial digital inputs, or when the digital video signal rate changes.

The synchronous lock time is defined as the time it takes the device to lock to a signal which has been momentarily interrupted.

4.9 Serial Data Output

The GS2985 features two current-mode differential output drivers, each capable of driving a maximum of 800mV$_{pp}$, differential, into an external 100Ω differential load.

Each of the GS2985's output buffers include two on-chip, 50Ω termination resistors.

4.9.1 Output Signal Interface Levels

The serial digital outputs of the GS2985 are compatible when DC-coupled with all Gennum serial digital interface products that feature a differential LVPECL or CML receiver designed for SDI applications and operate from 3.3V or 2.5V supplies. This includes but is not limited to: GS2978, GS2988, and GS2989 cable drivers.

4.9.2 Adjustable Output Swing

It is possible, via the host interface, to force the output swing to 400mV$_{pp}$ or 800mV$_{pp}$ differential, when the outputs are terminated with 50Ω loads.

The default output swing upon power-up is 400mV$_{pp}$ differential.

4.9.3 Output De-emphasis

The GS2985 features adjustable output de-emphasis to compensate for PCB trace dielectric losses.

The output de-emphasis has eight settings, evenly distributed from a minimum of 0dB (output de-emphasis OFF) to a peak de-emphasis setting that is optimized for compensating the high-frequency losses associated with approximately 20 inches of 5-mil stripline in FR4 material. These settings are accessible via the serial host interface.

The action of the de-emphasis settings is to attenuate the trailing edge of the output data waveform relative to the output swings set through the host interface.

Each serial digital output DDOn, $\overline{\text{DDOn}}$ includes a DEn_EN pin to turn its output de-emphasis on or off. De-emphasis is also turned OFF when in Bypass mode.

Table 4-7: Output De-emphasis

DEn_EN pin	Status of Output n
HIGH	Output De-emphasis ON
LOW	Output De-emphasis OFF

When DEn_EN is set LOW or left unconnected, the de-emphasis for output n is OFF. When $\overline{HIF}$ is HIGH, these DE_EN controls select between OFF and a setting that compensates for roughly five inches of trace.

All other settings are available only via the host interface.

When a DEn_EN pin is tied HIGH, the output de-emphasis for output n is ON.

The default de-emphasis setting upon power-up is 0dB (OFF).

NOTE: Changing the de-emphasis setting will vary both V1 & V2 (see Figure 4-2).

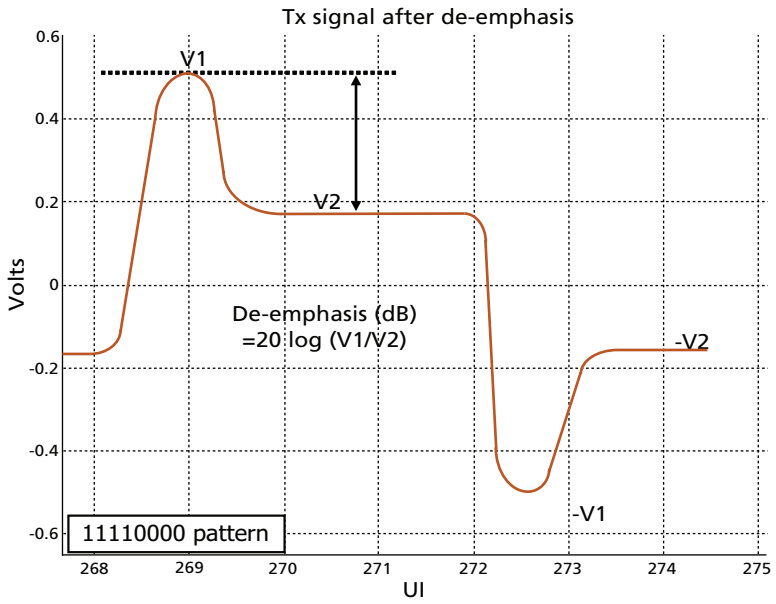


Figure 4-2: De-emphasis Waveform

4.10 Automatic and Manual Data Rate Selection

The GS2985 can be configured to manually lock to a specific data rate or automatically search for and lock to the incoming data rate. The AUTO/$\overline{MAN}$ pin selects Automatic data rate detection mode (AUTO mode) when HIGH and manual data rate selection mode (MANUAL mode) when LOW.

In AUTO mode, the SS[1:0] bi-directional pins become outputs and the bit pattern indicates the data rate at which the PLL is currently locked to (or previously locked to). The search algorithm

cycles through the data rates and starts over if that data rate is not found (see Figure 4-3).

A “search algorithm” cycles through the supported data rates until lock is achieved, as shown in Figure 4-3 below.

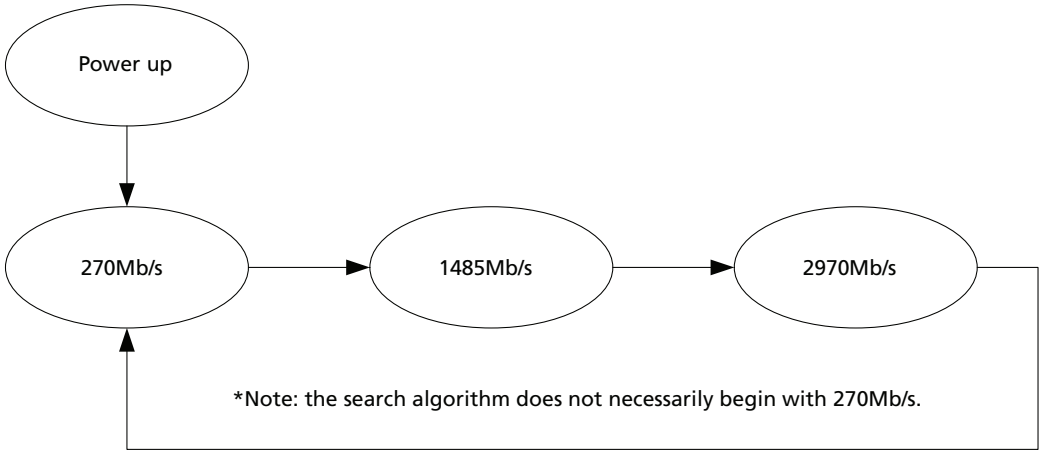


Figure 4-3: GS2985 Automatic Mode Search Algorithm

In MANUAL mode, the SS[1:0] pins become inputs and the data rate can be programmed. In this mode, the search algorithm is disabled and the GS2985's PLL will only lock to the data rate selected in accordance with Table 4-8.

Table 4-8: Data Rate Indication/Selection Bit Pattern

SS[1:0]	Data Rate (Mb/s)
0	Reserved
1	270
2	1485 or 1485/1.001
3	2970 or 2970/1.001

4.11 SD/$\overline{\text{HD}}$ Indication

The SD/$\overline{\text{HD}}$ signal indicates the output data rate of the device and can be connected to the SD/$\overline{\text{HD}}$ input pin of dual slew rate cable drivers such as the GS2988.

When this signal is HIGH, the data rate is 270Mb/s. This signal is LOW for all other data rates.

This signal is also LOW when the device is operating in bypass mode (Auto-bypass and User-bypass).

The SD/$\overline{\text{HD}}$ signal is LOW when the device is not locked.