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GS3241

3G-SDI Re-timing Adaptive Cable Equalizer

Key Features

- 75Ω cable input interface with on-chip termination
- SMPTE ST 424, ST 292-1 and ST 259 compliant input/output
- Multi-standard operation from 1Mb/s to 2.97Gb/s
- In addition to standard SMPTE rates, the device also supports re-timing of DVB-ASI at 270Mb/s, and MADI at 125Mb/s
- 3D Input Signal Eye Monitor
- PRBS generator and checker
- Automatic cable equalization—typical equalized cable lengths of Belden 1694A cable:
  - 190m at 2.97Gb/s
  - 260m at 1.485Gb/s
  - 450m at 270Mb/s and 125Mb/s
- Cable equalizer features:
  - Automatic power down on loss of signal
  - Programmable carrier detect with squelch threshold adjustment
  - Programmable launch swing compensation for non-compliant source
  - Manual and automatic cable equalizer bypass
- Trace driver features:
  - Integrated 100Ω, differential output termination
  - Extends output DC-coupling support with 1.2V to 2.5V output supply range
  - Trace driver data output pre-emphasis to compensate for up to 60″ FR4 at 2.97Gb/s
  - Manual or automatic re-timer bypass
  - Manual or automatic mute or disable on LOS
- CDR features:
  - Manual or automatic rate modes
  - Wide Loop bandwidth control
  - Re-timing at the following data rates: 125Mb/s, 270Mb/s, 1.485Gb/s, and 2.97Gb/s—this includes the f/1.001 rates

Additional Features

- Single 1.8V power supply for analog and digital core
- GSPI serial control and monitoring interface
- Four configurable GPIO pins for control or status monitoring
- Wide operating temperature range: -40°C to +85°C
- Small 6mm x 4mm 40-pin QFN
- Pb-free/Halogen-free/RoHS and WEEE compliant package
- Pin compatible with the GS12141, GS12142, and GS12241

Applications

SMPTE ST 424, SMPTE ST 292, SMPTE ST 259 interfaces requiring cable equalizing functionality. Typical applications: Cameras, Switchers, Distribution Amplifiers and Routers.

Description

The GS3241 is a low-power, multi-rate re-timing Cable Equalizer supporting rates up to 3G -SDI. It is designed to equalize and restore signals received over 190m coaxial cable at 3G, compensate for DC content of SMPTE pathological signals, and re-time the incoming data.

The integrated eye monitor provides non-disruptive mission mode analysis of the post equalized input signal. The 256x128 resolution scan matrix allows accurate signal analysis to speed up prototyping and enable field analysis.

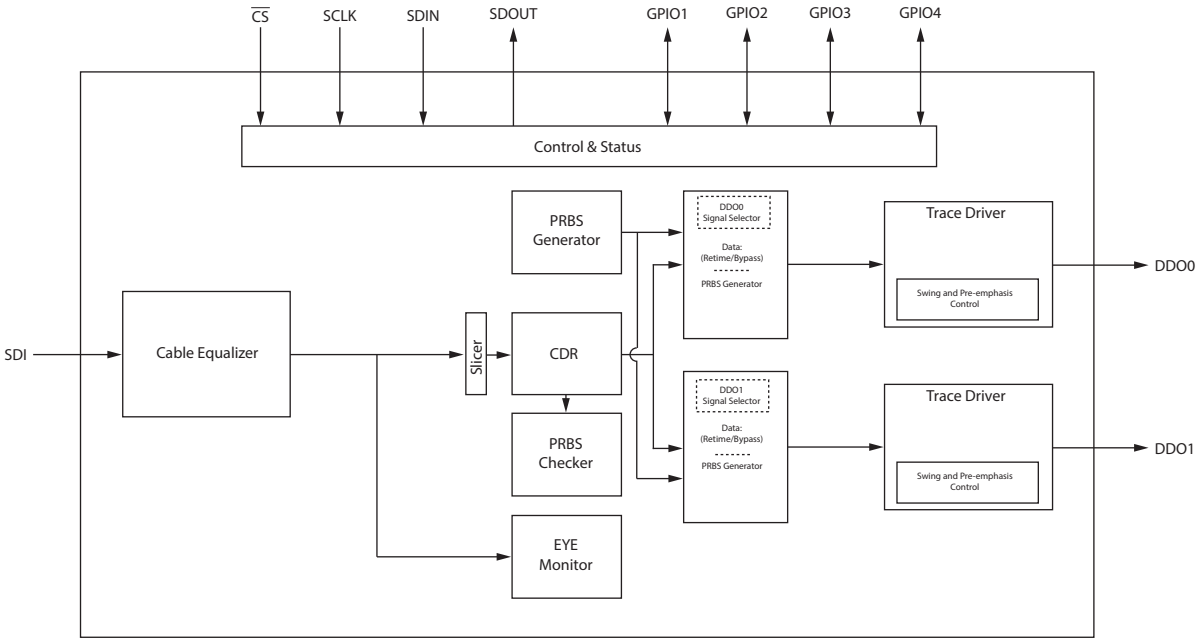
Built in macros enable customizable cross section analysis and quick horizontal and vertical eye opening measurements.

With high phase consistency between scans and configurable space and time thresholds, algorithms can be deployed in the field to analyse long term signal quality variation (Bathtub Plot) to reduce costly system installation debug time for intermittent errors.

The two independently controlled trace drivers feature highly configurable pre-emphasis and swing controls to compensate for long trace and connector losses. The pre-emphasis pulse width can be optimized to compensate for perturbations to frequency response of transmission lines due to vias connectors and stubs.

The GS3241 is pin compatible with the GS12141 and GS12241 single input, as well as the GS12142 dual input 12G UHD-SDI Multi-rate Re-timing Cable Equalizers.

Note: For the GS3241 to be pin compatible with the GS12142, careful design considerations are required. Contact for your local Semtech FAE for details.



GS3241 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
2	038575	—	September 2017	Updated Table 2-3.
1	037745	—	August 2017	Updated Host Initiated Device Reset. Added Device Power-up Sequence and Output Driver Data Rate Selection sections.
0	034153	—	November 2016	New Document.

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1. Pin Out

1.1 GS3241 Pin Assignment

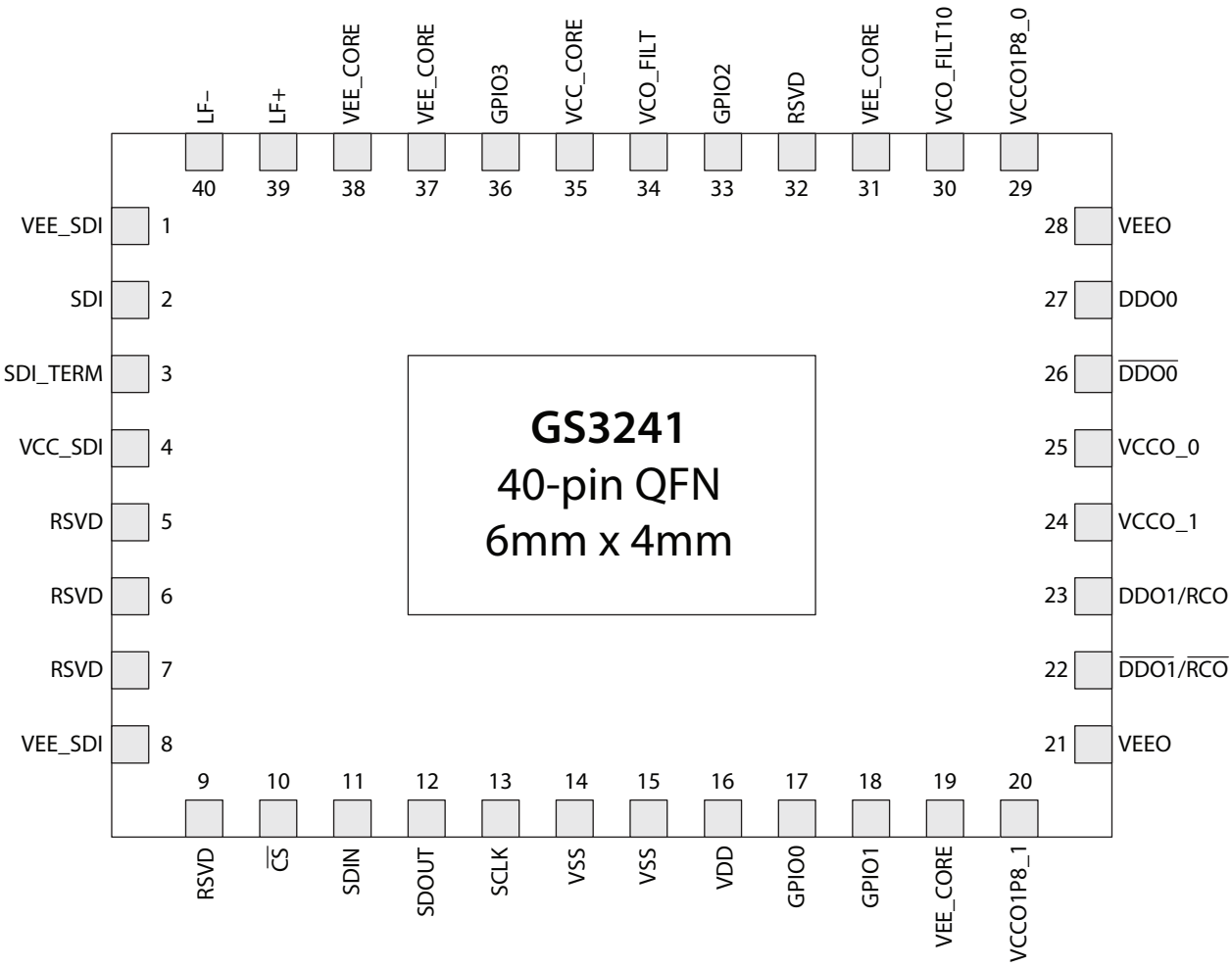

Figure 1-1: GS3241 Pin Assignment

1.2 GS3241 Pin Descriptions

Table 1-1: GS3241 Pin Descriptions

Pin Number	Name	Type	Description
1, 8	VEE_SDI	Power	Most negative power supply connection for the Cable Equalizer. Connect to ground.
2	SDI	Input	Single-ended CML input with internal 75Ω termination.
3	SDI_TERM	—	Input Common Mode termination. Decouple to ground through resistor and capacitor. See Section 6.1 for recommended values.
4	VCC_SDI	Power	Most positive power supply connection for the Cable Equalizer. Connect to 1.8V and decouple to ground. See Section 6.1 for recommended values.
5, 6, 7, 9, 32	RSVD	—	These pins may be left floating. Please contact your Semtech FAE for additional information on circuit compatibility with the GS3281.
10	$\overline{CS}$	Digital Input	Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-up. Active-LOW input. Refer to Section 4.9.1 for more details.
11	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.9.2 for more details.
12	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS output. Refer to Section 4.9.3 for more details.
13	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.9.4 for more details.
14, 15	VSS	Power	Most negative power supply for digital core logic. Connect to ground.
16	VDD	Power	Most positive power supply connection for digital core logic. Connect to 1.8V and decouple to ground. See Section 6.1 for recommended values.
17	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Default function: Direction = Output Signal = HIGH indicates LOS (Loss of Signal, inverse of Carrier Detect) Pin is 1.8V CMOS I/O, please refer to GPIO0_CFG for more information on how to configure GPIO0.

Table 1-1: GS3241 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
18	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Default function: Direction = Output Signal = HIGH indicates PLL is locked Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1.
19, 31, 37, 38	VEE_CORE	Power	Most negative power supply connection for the analog core. Connect to ground.
20	VCCO1P8_1	Power	Most positive power supply connection for trace driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 for recommended values.
21, 28	VEEO	Power	Most negative power supply connection for the output drivers. Connect to ground.
22, 23	$\overline{\text{DDO1}}$/$\overline{\text{RCO}}$, DDO1/RCO	Output	Differential CML output with two internal 50Ω pull-ups. The data signal or PRBS generator can be selected for this output. The PRBS generator can be configured to generate a PRBS7 or a clock pattern.
24	VCCO_1	Power	Most positive power supply connection for the DDO1/ $\overline{\text{DDO1}}$ output driver. Connect to 1.2V – 2.5V and decouple to ground. See Section 6.1 for recommended values.
25	VCCO_0	Power	Most positive power supply connection for the DDO0/$\overline{\text{DDO0}}$ output driver. Connect to 1.2V – 2.5V and decouple to ground. See Section 6.1 for recommended values.
26, 27	$\overline{\text{DDO0}}$/DDO0	Output	Differential CML output with two internal 50Ω pull-ups. The data signal or PRBS generator can be selected for this output. The PRBS generator can be configured to generate a PRBS7 or a clock pattern.
29	VCCO1P8_0	Power	Most positive power supply connection for trace driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 for recommended values.
30	VCO_FILT10	Passive	VCO filter capacitor connection. Decouple to ground. See Section 6.1 for recommended values.
33	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. Default function: Direction = Input Signal = Set HIGH to put device in sleep Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2.
34	VCO_FILT	Passive	VCO filter capacitor connection. Decouple to ground. See Section 6.1 for recommended values.
35	VCC_CORE	Power	Most positive power supply connection for the analog core. Connect to 1.8V and decouple to ground. See Section 6.1 for recommended values.

Table 1-1: GS3241 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
36	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Default function: Direction = Input Signal = Set HIGH to disable DDO1 Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3.
39	LF+	Passive	Loop filter capacitor connection. Connect to pin 40 through capacitor. See Section 6.1 for recommended values.
40	LF-	Passive	Loop filter capacitor connection. Connect to pin 39 through capacitor. See Section 6.1 for recommended values.
Tab	—	—	Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation. It is not recommended to connect device ground pins to the central paddle.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage—Core (VCC_SDI, VCC_CORE, VDD)	-0.5V to +2.2V
Supply Voltage—Output Driver (VCCO_0, VCCO_1)	-0.5V to +2.8V
Input ESD Voltage (any pin)	2kV HBM
Storage Temperature Range (T_S)	-50°C to +125°C
Input Voltage Range (SDI, $\overline{SDI}$)	-0.3 to (VCC_SDI +0.3)V
Input Voltage Range (GPIO2, GPIO3)	-0.3 to (VCC_CORE +0.3)V
Input Voltage Range ($\overline{CS}$, SDIN, SCLK, VSS, VDD, GPIO0, GPIO1)	-0.3 to (VDD +0.3)V
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	VCC_SDI, VCC_CORE, VDD		1.71	1.8	1.89	V	—
Supply Voltage - Output Driver	VCCO_0, VCCO_1		1.14	1.2	1.26	V	—
			1.71	1.8	1.89	V	—
			2.38	2.5	2.63	V	—
Power—Mission Mode (DDO0/$\overline{\text{DDO0}}$ enabled, DDO1/$\overline{\text{DDO1}}$ disabled)	P_D	VCCO_0 = 1.2V, Output Swing = 400mV$_{ppd}$	—	405	—	mW	1
		VCCO_0 = 1.8V, Output Swing = 400mV$_{ppd}$	—	410	—	mW	1
		VCCO_0 = 1.8V, Output Swing = 800mV$_{ppd}$	—	430	—	mW	1
		VCCO_0 = 2.5V, Output Swing = 400mV$_{ppd}$	—	420	—	mW	1
		VCCO_0 = 2.5V, Output Swing = 800mV$_{ppd}$	—	440	—	mW	1
Power—Sleep Mode	P_D	Sleep	—	35	50	mW	—
Supply Current—Trace Driver	I_{CCO_0}, I_{CCO_1}	VCCO = 1.2V, Output Swing = 400mV$_{ppd}$	—	9	16	mA	1, 3
		VCCO = 1.8V, Output Swing = 400mV$_{ppd}$	—	9	16	mA	1, 3
		VCCO = 1.8V, Output Swing = 800mV$_{ppd}$	—	18	27	mA	1, 3
		VCCO = 2.5V, Output Swing = 400mV$_{ppd}$	—	9	16	mA	1, 3
		VCCO = 2.5V, Output Swing = 800mV$_{ppd}$	—	18	27	mA	1, 3
Supply Current—Trace Driver Pre-driver	I_{CCO1P8_0}, I_{CCO1P8_1}	VCCO1P8_0 Output Swing = 800mV$_{ppd}$	—	25	32	mA	1, 3
		VCCO1P8_1 Output Swing = 800mV$_{ppd}$	—	25	32	mA	1, 3

Table 2-2: DC Electrical Characteristics (Continued)

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Current—Analog Core	I_{CC_CORE}	CDR Locked to Rate	—	124	142	mA	—
		CDR Unlocked During Rate Search	—	182	—	mA	—
		PRBS Generator Enabled	—	119	—	mA	4,5
		PRBS Checker Enabled	—	60	—	mA	4
		Eye Monitor Enabled	—	54	—	mA	4
Supply Current—Cable Equalizer	I_{CC_SDI}	—	—	55	75	mA	—
Supply Current—Digital Logic	I_{DD}	—	—	15	18	mA	—
DDO Output Common Mode Voltage	V_{CMOUT}	—	—	$V_{CMOUT} = V_{CCO} - \Delta V_{DDO}/2$	—		2
DDO Output Termination		Differential	—	100	—	Ω	2
SDI Input Termination		Between SDI and GND	—	75	—	Ω	—
Input Voltage—Digital Pins ($\overline{CS}$, SDIN, SCLK, GPIO[0:3])	V_{IH}		0.65* VDD	—	VDD	V	—
	V_{IL}		0	—	0.35* VDD	V	—
Output Voltage—Digital Pins (SDOUT, GPIO[0:3])	V_{OH}	I_{OH} = -5mA	VDD - 0.45	—	—	V	—
	V_{OL}	I_{OL} = +5mA	—	—	0.45	V	—

Notes:

1. Pre-emphasis is disabled.
2. This applies for DDO0 and DDO1.
3. The specifications provided are per symbol, not a combined value.
4. Current listed is an increase to ICC_CORE when stated condition is true.
5. Selected clock source = VCO free running.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VCC_SDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +1.2/1.8/2.5V ±5%, T_A = -40°C to +85°C, unless otherwise shown.
The rise/fall time of signals at source should not be more than 62ns.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR_{SDI}	—	0.001	—	2.97	Gb/s	—
Upstream Launch Swing	V_{SDI}	—	720	800	880	mV_{pp}	3
Differential Output Voltage Swing	ΔV_{DDO}	200mV	150	200	250	mV_{ppd}	9
		800mV	600	800	1000	mV_{ppd}	10
Intrinsic Input Jitter Tolerance	IIJT	MADI/SD/HD/3G	0.8	0.95	—	UI	—
PLL Lock Time—Asynchronous	t_{ALOCK}	—	—	75	—	ms	6
PLL Lock Time—Synchronous	t_{SLOCK}	SD	—	—	10	µs	6
		HD/3G	—	—	2	µs	6
DDO, $\overline{DDO}$, Rise/Fall Time	$t_{riseDDO1}$, $t_{fallDDO1}$	All rates	—	—	40	ps	5,7
DDO Mismatch in Rise/Fall Time	—	—	—	—	8	ps	5,7
DDO Duty Cycle Distortion	—	—	—	—	10	ps	7
Input Return Loss	—	5MHz to 1.485GHz	—	—	-17	dB	1
		1.485GHz to 2.97GHz	—	—	-12	dB	1
Serial Data Output Jitter DDO0, $\overline{DDO0}$ DDO1, $\overline{DDO1}$	$t_{OJ(125Mb/s)}$	450m	—	0.01	0.05	UI_{pp}	2,11
	$t_{OJ(270Mb/s)}$	450m	—	0.05	0.20	UI_{pp}	2,11
	$t_{OJ(270Mb/s)}$	400m	—	0.05	0.10	UI_{pp}	2,11
	$t_{OJ(1.485Gb/s)}$	260m	—	0.03	0.10	UI_{pp}	2,11
	$t_{OJ(2.97Gb/s)}$	190m	—	0.05	0.10	UI_{pp}	2,11

Table 2-3: AC Electrical Characteristics (Continued)

VCC_SDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +1.2/1.8/2.5V ±5%, T_A = -40°C to +85°C, unless otherwise shown.
The rise/fall time of signals at source should not be more than 62ns.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Loop Bandwidth	$BW_{LOOP(125Mb/s)}$	Setting 0.0625x	—	10	—	kHz	8
		Setting 0.125x	—	20	—	kHz	8
		Setting 0.25x	—	38	—	kHz	8
		Setting 0.5x (Default)	—	76	—	kHz	8
		Setting 1.0x	—	150	—	kHz	8
	$BW_{LOOP(270Mb/s)}$	Setting 0.0625x	—	20	—	kHz	8
		Setting 0.125x	—	40	—	kHz	8
		Setting 0.25x	—	80	—	kHz	8
		Setting 0.5x	—	160	—	kHz	8
		Setting 1.0x (Default)	—	316	—	kHz	8
	$BW_{LOOP(1.485Gb/s)}$	Setting 0.0625x	—	110	—	kHz	8
		Setting 0.125x	—	220	—	kHz	8
		Setting 0.25x	—	440	—	kHz	8
		Setting 0.5x (Default)	—	876	—	kHz	8
		Setting 1.0x	—	1750	—	kHz	8
	$BW_{LOOP(2.97Gb/s)}$	Setting 0.0625x	—	220	—	kHz	8
		Setting 0.125x	—	440	—	kHz	8
		Setting 0.25x	—	880	—	kHz	8
		Setting 0.5x (Default)	—	1.76	—	MHz	8
		Setting 1.0x	—	3.5	—	MHz	8

Table Notes:

1. Values achieved with Semtech evaluation board and connector.
2. Measured using a clean input source.
3. Default value for CFG_EQ_INPUT_LAUNCH_SWING_COMP parameter in control register 0x18. The default parameter value is 80_d (50_h).
4. Default trace driver swing Setting.
5. Rise/Fall time was measured between 80% and 20%.
6. Please see 4.3.3.1 for the further definition on Synchronous and Asynchronous Lock Time.
7. This specification applies to and DDO1/$\overline{\text{DDO1}}$ and DDO0/$\overline{\text{DDO0}}$.
8. Please see PLL_LOOP_ BANDWIDTH_ 1 for the full range of loop bandwidth settings.
9. Output Driver Setting of 8.
10. Output Driver Setting of 36.
11. Max jitter occurs at the maximum cable length.

Note: For GSPI Timing see Table 4-11: GSPI Timing Parameters.

3. Input/Output Circuits

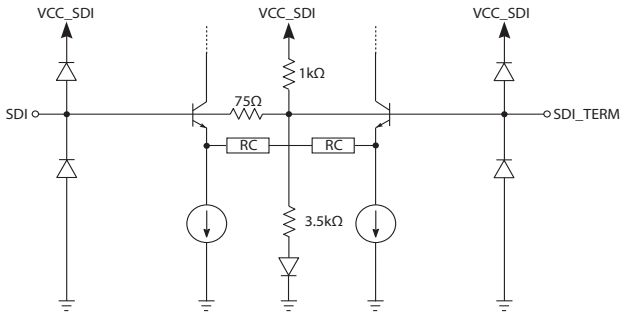

Figure 3-1: SDI, SDI_TERM

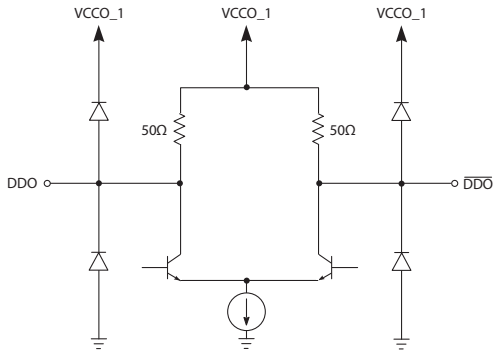

Figure 3-2: DDO1/$\overline{DDO1}$, DDO0/$\overline{DDO0}$

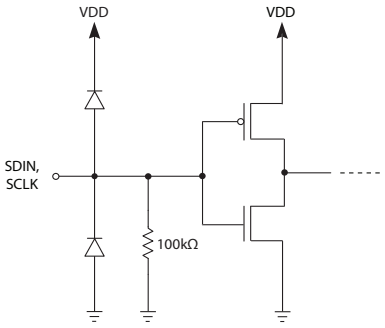

Figure 3-3: SDIN, SCLK

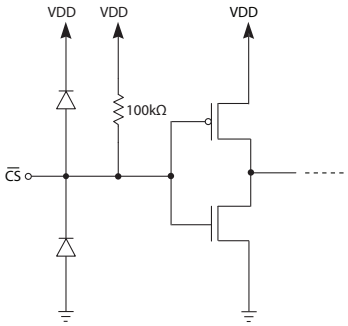

Figure 3-4: $\overline{CS}$

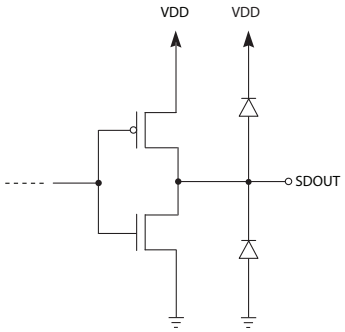

Figure 3-5: SDOUT

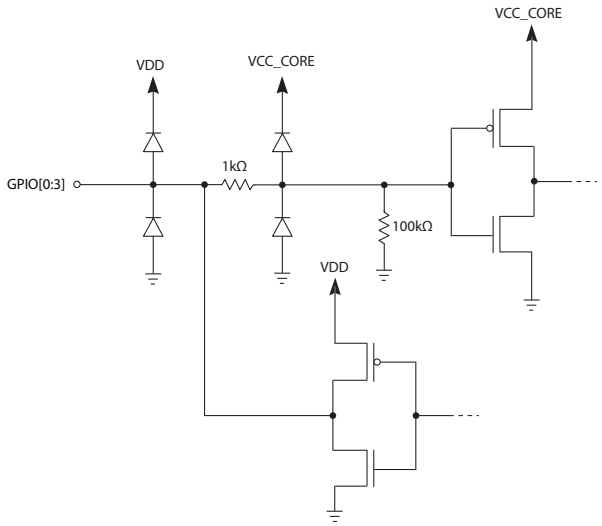

Figure 3-6: GPIO[0:3]

4. Detailed Description

4.1 Device Description

The GS3241 features a 75Ω internally terminated Cable Equalizer, which can equalize up to 190m of Belden1694A cable at 3G. The device includes a CDR which will lock to and retime valid SMPTE, MADI, and DVB-ASI signals to produce extremely low output jitter, even at extended cable lengths. The CDR has extensive LBW control to enable jitter transfer optimization. To facilitate system testing, the device also includes 3D eye monitor, PRBS7 checker and generator. The two trace drivers have independent amplitude and pre-emphasis control which can compensate for 14dB of insertion loss at 1.485GHz. The pre-emphasis control is two dimensional in both drivers, where both pre-emphasis pulse amplitude and width adjustments can be made to help optimize for interconnect mismatches such as vias and connectors.

4.1.1 Sleep Mode

To enable low power operation, the GS3241 has manual and automatic sleep mode control.

The default mode is automatic sleep mode on LOS (Loss Of Signal). The device can also be manually put into sleep mode. When the device is in sleep mode, all the core blocks are powered down, except the host interface and carrier detect circuits. The trace driver can be configured to be disabled or muted during sleep.

The **CTRL_AUTO_SLEEP** and **CTRL_MANUAL_SLEEP** parameters in register 0x3, control the sleep mode of the device. The default value of the **CTRL_AUTO_SLEEP** parameter is 1_b (auto sleep). While in auto sleep mode, the **CTRL_MANUAL_SLEEP** parameter has no effect. To enable host control of the sleep mode, set the **CTRL_AUTO_SLEEP** parameter to 0_b manual sleep control. To prevent the device from entering sleep, set the **CTRL_MANUAL_SLEEP** parameter to 0_b (not sleep). To manually configure the device to sleep, set the **CTRL_MANUAL_SLEEP** parameter to 1_b (sleep).

The device can also be manually made to sleep through the *GPIO* pins. The default GPIO pin to control sleep is *GPIO2* (pin 33). Drive this pin HIGH to make the device sleep.

Section 4.6 describes the PRBS generator function. If the device's PRBS generator is intended to be used without a valid input signal, the device should be manually set to not sleep as described above. Without a valid input signal, an LOS status will be generated and the device will enter sleep mode and the PRBS block will be disabled. For a description of LOS thresholds and settings, see Section 4.2.3.

4.2 Cable Equalizer

The GS3241 can automatically adjust its gain to equalize and restore SMPTE compliant signals received over different lengths of coaxial cable having loss characteristics similar to Belden 8281 or 1694A. With the default settings, the device will automatically equalize MADI at 125Mb/s and most common SMPTE compliant signal between SD at 270Mb/s and 3G-SDI at 2.97Gb/s and bypass signals below 125Mb/s.

The GS3241 features programmable Launch Swing Compensation, squelch threshold adjust, and bypass, all of which can be set through the device's host interface. The equalized or bypassed signal is then routed to the eye monitor and serial digital re-timer (CDR) block.

4.2.1 Cable Equalizer Bypass

With the default settings, the device will automatically bypass signals below 125Mb/s. During cable equalizer-bypass mode, the device supports LOW data rate and slow edge signals such as SMPTE310 and AES3id. The rise/fall times must not exceed 62ns. These signals will not be re-timed by the CDR block. The following two methods allow the user to force the signal to bypass the equalization and DC restoration stages:

1. Via the host interface, by setting **CTRL_CEQ_AUTO_BYPASS** to 0_b, and **CTRL_CEQ_MANUAL_BYPASS** to 1_b in register 0x17.

2. Via the *GPIO[0:3]* pin (see Section 4.8).

4.2.2 Upstream Launch Swing Compensation

The GS3241 cable equalizer has an automatic gain control circuit, that is optimized on the assumption that the trace driver in the upstream device is SMPTE compliant and has a launch swing of $800mV_{pp}$ ±10%. When the source amplitude is known to be non-SMPTE compliant, a compensation adjustment can be made in the GS3241. The GS3241 can adjust for launch swings in the range of 250mV to 1V in approximately $50mV_{ppd}$ increments. Upstream launch swing compensation can be adjusted through the **CFG_EQ_INPUT_LAUNCH_SWING_COMP** parameter in control register 0x18. The default parameter value is 80_d (50_h), which corresponds to a nominal launch swing of $800mV_{ppd}$.

4.2.3 Carrier Detect, Squelch Control, and Loss of Signal

The GS3241 cable equalizer has highly configurable carrier detection and squelching capability. The carrier detection can be made more robust against spurious signals and noise at the inputs and the squelch control can be configured and enabled to reduce false outputs to low level signals such as crosstalk.

The GS3241 reports two separate carrier detect parameters—**STAT_PRI_CD** and **STAT_SEC_CD**. They are described in Section 4.2.3.1 and Section 4.2.3.2 respectively.

Note: The parameters referred to within Section 4.2.3 to Section 4.2.3.2 are linked to their respective registers in Table 4-1.

4.2.3.1 Primary Carrier Detection (STAT_PRI_CD) Configuration

Primary carrier detection (**STAT_PRI_CD**) can be configured for higher stability by filtering out longer transients or glitches. This can be achieved by increasing the sampling window over which the signal is sampled and the number of samples required to assert or de-assert it.

There are three configuration parameters that control assertion or de-assertion of **STAT_PRI_CD**:

- **CFG_CD_FILTER_SAMPLE_WIN**
- **CFG_FILTER_DEASSERT_CNT**
- **CFG_CD_FILTER_ASSERT_CNT**

See Figure 4-1 for a visual representation of the **STAT_PRI_CD** configuration parameters.

With the default values in place:

- An assertion (setting HIGH) of **STAT_PRI_CD** will take place after a valid signal is present for ~6.5ms
- A de-assertion (setting LOW) of **STAT_PRI_CD** will take place after loss of a valid signal for ~96ms

If the application requires any adjustment of the sampling window, assertion count, or de-assertion count, please consult the following equations to calculate the associated time to assert or de-assert STAT_PRI_CD.

STAT_PRI_CD de-assert time:

- *(1.6µs) * (CFG_CD_FILTER_SAMPLE_WIN + 1) * CFG_CD_FILTER_ DEASSERT_CNT*

STAT_PRI_CD assert time:

- (1.6µs) * (CFG_CD_FILTER_SAMPLE_WIN + 1) * CFG_CD_FILTER_ASSERT_CNT

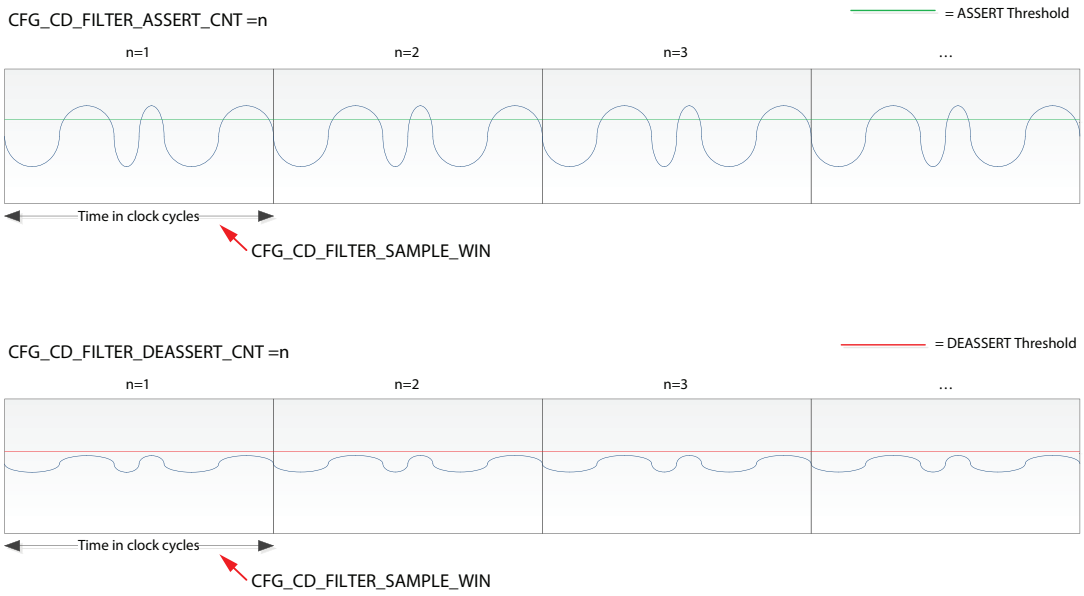

Figure 4-1: STAT_PRI_CD Configuration Parameters

4.2.3.2 Secondary Carrier Detection (STAT_SEC_CD) Configuration

The secondary carrier detection signal acts as an additional carrier detection which can be further filtered through squelch controls. It also serves as the control signal for Mute on LOS (Loss Of Signal) and Disable on LOS. Please refer to Section 4.7.6 to Section 4.7.6.2 for further information on this.

If the application requires the use of squelch settings, start by setting the following:

- **CFG_SEC_CD_INCL_CLI_SQUELCH** = 1

Once this parameter is set, the device will apply squelch based off of the settings found within the following parameters:

- **CFG_CLI_SQUELCH_THRESHOLD**
- **CFG_CLI_SQUELCH_HYSTERESIS**

The device will use these parameters to determine squelch status and set that within **STAT_CLI_SQUELCH**. Based off of this, secondary carrier detection can be described as:

- **STAT_SEC_CD** = inverse of (**STAT_CLI_SQUELCH** & **STAT_PRI_CD**).

To help detail how the device determines the state of Squelch, we define the following variables:

- CLI = STAT_CABLE_LEN_INDICATION
- THR = CFG_CLI_SQUELCH_THRESHOLD
- HYS = CFG_CLI_SQUELCH_HYSTERESIS
- SQL = STAT_CLI_SQUELCH

The following rules define the state of SQL. **Note:** If the cable equalizer is in bypass (**STAT_CEQ_BYPASS** = 1), the device will set SQL to 0.

- If CLI > (THR + HYS), the device will set SQL to 1, otherwise:
- If CLI < (THR - HYS), the device will set SQL to 0, otherwise:
- If CLI ≥ (THR - HYS) and CLI ≤ (THR + HYS), SQL remains unchanged
- If SQL = 1, the device will not indicate lock and the trace driver state will be defined by output state control parameters settings, see Section 4.7.6 for more details

Table 4-1: Cable Equalizer Status and Configuration Parameters

Register Address$_h$ and Name	Parameter Name	Parameter Description
15, CARR_ DET_CFG	CFG_SEC_CD_INCL_CLI_SQUELCH	Enables or disables squelch control.
16, SQUELCH_ PARAMETERS	CFG_CLI_SQUELCH_THRESHOLD	Used to tune the squelch threshold based on the tolerance requirements of the application.
	CFG_CLI_SQUELCH_HYSTERESIS	Used to tune the squelch hysteresis based on the tolerance requirements of the application.
20, CD_FILTER_ DELAYS_0	CFG_CD_FILTER_SAMPLE_WIN	Primary carrier detect sampling window size.
21, CD_FILTER_ DELAYS_1	CFG_CD_FILTER_DEASSERT_CNT	Primary carrier detect de-assertion count.
22, CD_FILTER_ DELAYS_2	CFG_CD_FILTER_ASSERT_CNT	Primary carrier detect assertion count.
84, STICKY_ COUNTS_0	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.
	STAT_CNT_SEC_CD_CHANGES	A counter showing the number of times the secondary Carrier Detect signal changed.
86, CURRENT_ STATUS_0	STAT_CLI_SQUELCH	Cable equalizer Squelch status.
87, CURRENT_ STATUS_1	STAT_PRI_CD	Primary filtered carrier detect of the analog carrier detect signal.
	STAT_SEC_CD	Secondary filtered carrier detect of the analog carrier detect signal.
88, EQ_GAIN_IND	STAT_CABLE_LEN_INDICATION	SDI cable length indicator.

4.3 Serial Digital Re-timer (CDR)

The GS3241 includes an integrated CDR, whose purpose is to lock to a valid incoming signal from the cable equalizer stage and produce a lower jitter signal at the cable or trace driver outputs. The CDR has the ability to lock to any of the following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), and 3G-SDI (2.97Gb/s). This includes the f/1.001 rates.The default settings of the re-timer block are optimal for most applications. However, the following controls allow the user to customize the behaviour of the re-timer: LBW control, Automatic and Manual Rate Detection. Please see Section 4.3.1 to Section 4.3.2 for a description of these functionalities.

Note: The parameters referred to within Section 4.3.1 to Section 4.3.2 are linked to their respective registers in Table 4-3. For a complete list of registers and functions, please see Section 5.

4.3.1 PLL Loop Bandwidth Control

The ratio of output peak-to-peak jitter to input peak-to-peak jitter of the CDR can be represented by a low-pass jitter transfer function, with a bandwidth equal to the PLL LBW. Although the default LBW settings for the GS3241 CDR are ideal for most SDI signals, the GS3241 allows the user to adjust the LBW for each supported rate.

Registers 0x0B through 0x0C contain the following parameters which allow the user to configure rate dependent LBW: **CFG_PLL_LBW_3G**, **CFG_PLL_LBW_HD**, **CFG_PLL_LBW_SD**, and **CFG_PLL_LBW_MADI**. The LBW settings are defined in terms of ratios of the nominal LBW. For each rate, where '1.0x' is the nominal LBW, the following ratios are available: 0.0625x, 0.125x, 0.25x, 0.5x, and 1.0x. Table 2-3 provides the specific loop bandwidths for each data rate and LBW setting. Lowering the LBW will lower the jitter amplitude above the LBW frequency. Although lower output jitter is desirable, the lower LBW may reduce the device's IJT to very high jitter that may be present outside the LBW.

4.3.2 Automatic and Manual Rate Detection

With the default rate detect setting, the CDR will automatically attempt to lock to any of following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), and 3G-SDI (2.97Gb/s). This includes the f/1.001 rates. However, the CDR can be configured to only lock to a single rate, by setting the **CFG_AUTO_RATE_DETECT_ENA** and **CFG_MANUAL_RATE** parameters in register 0x06.

The **STAT_LOCK** parameter in register 0x86 will indicate that the CDR is locked when its value is 1_b and unlocked when its value is 0_b. The lock status can also be monitored externally on any *GPIO* pin, however it is the default mode for *GPIO1*, pin 18. The **STAT_DETECTED_RATE** parameter in register 0x87 will indicate the data rate at which the CDR is locked to. A value of 0_d in the **STAT_DETECTED_RATE** parameter indicates that the device is not locked, while values between 1_d and 4_d will indicate that the device is locked to one of the four available rates between MADI at 125Mb/s and 3G-SDI at 2.97Gb/s.

Table 4-2: Detected Data Rates

STAT_DETECTED_RATE [2:0]	Detected Data Rate
0	Unlocked
1	MADI (125Mb/s)
2	SD (270Mb/s)
3	HD (1.485Gb/s)
4	3G (2.97Gb/s)
5	Reserved
6	Reserved
7	Reserved

If the CDR cannot lock to any of the valid rates in automatic mode or the selected rate in manual mode, the signal can automatically be bypassed to the output. If the CDR does lock to the incoming signal, the re-timed and bypassed (if manual bypass control enabled) signals are available at the appropriate output. See the Section 4.7 for more details.

4.3.3 Lock Time

4.3.3.1 Synchronous and Asynchronous Lock Time

Synchronous lock time is defined as the time it takes the device to re-lock to an existing signal that has been momentarily interrupted or to a new signal of the same data rate as the previous signal which has been quickly switched in.

Asynchronous lock time is defined as the time it takes the device to lock when a signal is first applied to the serial digital inputs, or when the signal rate changes. The asynchronous and synchronous lock times are defined in Table 2-3.

Note: To ensure synchronous lock times are met, the maximum interruption time of the signal is 10µs for an SD-SDI signal. HD, and 3G signals must have a maximum interruption time of 6µs. The new signal, after interruption, must have the same frequency as the original signal but may have an arbitrary phase.

Table 4-3: CDR Control and Status Parameters

Register Address$_h$ and Name	Parameter Name	Description
06, RATE_ DETECT_ MODE	CFG_AUTO_RATE_DETECT_ENA	Enables or disables the automatic rate detection mode of the CDR.
	CFG_MANUAL_RATE	Select a single rate for CDR rate detection when CFG_AUTO_RATE_DETECT_ENA is 0_b.
0B, PLL_LOOP_ BANDWIDTH_ 1	CFG_PLL_LBW_3G	Configures the Loop Bandwidth for 3G signals.
	CFG_PLL_LBW_HD	Configures the Loop Bandwidth for HD signals.
0C, PLL_LOOP_ BANDWIDTH_ 2	CFG_PLL_LBW_SD	Configures the Loop Bandwidth for SD signals.
	CFG_PLL_LBW_MADI	Configures the LBW for MADI signals.
11, GPIO1_CFG	CFG_GPIO1_FUNCTION	Sets the function of GPIO1.
	CFG_GPIO1_OUTPUT_ ENA	Sets the GPIO pin as either an output or an input.
85, STICKY_ COUNTS_1	STAT_CNT_PLL_LOCK_CHANGES	Counter showing the number of times the PLL lock status changed.
	STAT_CNT_RATE_CHANGES	Counter showing the number of times the PLL lock rate changed.
86, CURRENT_ STATUS_0	STAT_LOCK	The status of the PLL. Locked, or unlocked.
87, CURRENT_ STATUS_1	STAT_DETECTED_RATE	The rate at which the PLL is locked to.

4.4 PRBS Checker

The GS3241 includes an integrated PRBS checker, which can error check a PRBS7 signal out of the cable equalizer input block.

There are two modes of operation for the PRBS checker:

- **Timed Mode:** Used for precise measurements of up to ~3.334s.
  - In timed mode, the host sets the measurement time and executes the checker operation. The device ends the PRBS error check measurement when the timer expires, and the host reads back the measurement status and error count.
- **Continuous Mode:** Can be used for longer measurements but with less precision in the time interval.
  - In continuous mode, the host controls the starts and stops of the PRBS error checking operation then reads back the measurement status and error count.

Note: When working with the PRBS Checker, please note the following:

- The parameters referred to in this Section 4.4.1 to Section 4.4.2 are briefly described and linked to their respective registers in Table 4-4. For a complete list of registers and functions, please see Section 5.
- The PRBS generator and checker can be active at the same time, however, the generator can not be looped back on itself for error checking.

4.4.1 Timed PRBS Check Measurement Procedure

For applications where measurement times are ~3.34s or less, the timed PRBS check mode is the most suitable. Alternatively, to achieve precise timing for lower BER signals, the timed PRBS check measurement can be repeated by the host and the total measurement time and error count is determined by summing the individual measurements.

In timed mode, the host sets the total measurement time by setting the **CFG_PRBS_CHECK_PREDIVIDER** and the **CFG_PRBS_CHECK_MEAS_TIME** parameters to the required values to achieve the total measurement time required by the application.

To perform a timed PRBS measurement, please complete the following steps:

1. Set the appropriate settings within **CFG_PRBS_CHECK_PREDIVIDER** and **CFG_PRBS_CHECK_MEAS_TIME** to achieve the total measurement time required by the application. The TMT (Total Measurement Time) is determined by the following equation:
   TMT = CFG_PRBS_CHECK_PREDIVIDER * (CFG_PRBS_CHECK_MEAS_TIME *256+1) * (1/40MHz)

   Note: Using the default **CFG_PRBS_CHECK_PREDIVIDER** setting of 0 (pre-divider = 4) and **CFG_PRBS_CHECK_MEAS_TIME** setting of 3 (MEAS_TIME = 3), the TMT (total measurement time) is ~77µs per measurement.
2. Follow the steps outlined in Figure 4-2: Timed PRBS Check Flow.

4.4.2 Continuous PRBS Check Measurement Procedure

As previously mentioned, the maximum measurement time for a timed PRBS error measurement is ~3.35 seconds. For links with very low error rates, this time is insufficient to capture an adequate number of errors. For these situations, the continuous PRBS check measurement is more appropriate.

In continuous PRBS measurement mode, the measurement can run as long as required (assuming the device remains locked) to ensure the BER test level is met.

To perform a continuous PRBS measurement, please follow the steps outlined in the flowchart found within Figure 4-3: Continuous PRBS Check Flow.

Table 4-4: PRBS Checker Parameter Description

Address$_h$	Parameter Name	Description
50, PRBS_CHK_CFG	CFG_PRBS_CHECK_PREDIVIDER	Selects pre-divider for PRBS check measurement timer.
	CFG_PRBS_CHECK_MEAS_TIME	Selects PRBS check measurement interval for timed measurements.
51, PRBS_CHK_CTRL	CTRL_PRBS_CHECK_TIMED_CONT_B	Selects between timed and continuous type PRBS measurement.
	TRL_PRBS_CHECK_START	Used to start and stop PRBS measurements.
89, PRBS_CHK_ERR_CNT	STAT_PRBS_CHK_ERR_CNT	PRBS error count storage location.
8A, PRBS_CHK_STATUS	STAT_PRBS_CHECK_STATUS	Status indication of PRBS checker.
	STAT_PRBS_CHECK_LAST_ABORT	Indication bit for PRBS successful completion or abort.

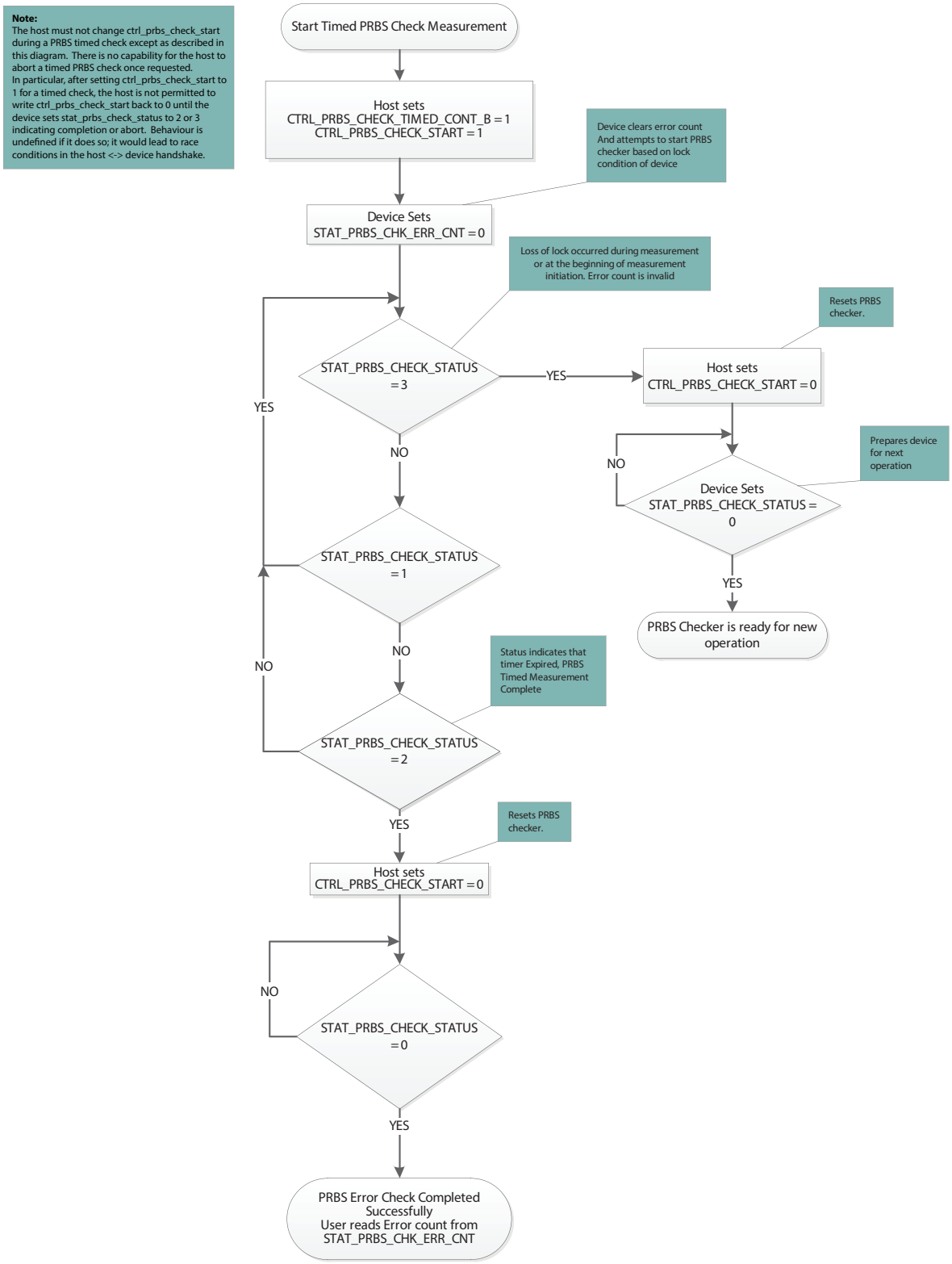

Figure 4-2: Timed PRBS Check Flow