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GS3281

3G-SDI Re-timing Cable Driver

Key Features

- Dual non-inverted 75Ω cable interface with on-chip termination
- SMPTE ST 424, ST 292-1 and ST 259 compliant input/output
- Multi-standard operation from 1Mb/s to 2.97Gb/s
- In addition to standard SMPTE rates, the device also supports re-timing of DVB-ASI at 270Mb/s, and MADI at 125Mb/s.
- Cable driver features:
  - Wide swing control
  - Pre-emphasis to compensate for significant insertion loss between device output and BNC
  - Automatic/manual output slew rate control
  - Manual or automatic re-timer bypass
  - Manual or automatic Mute or disable on LOS
- Trace equalizer features:
  - Integrated 100Ω, differential input termination
  - Automatic power down on loss of signal
  - Adjustable carrier detect threshold
  - DC-coupling from 1.2V to 2.5V CML logic
  - Trace equalization to compensate for up to 60" FR4 at 2.97Gb/s
  - Automatic input offset compensation
- CDR features:
  - Manual or automatic rate modes
  - Wide Loop bandwidth control
  - Re-timing at the following data rates: 125Mb/s, 270Mb/s, 1.485Gb/s, and 2.97Gb/s. This includes the f/1.001 rates.

Additional Features

- Single 1.8V power supply for analog and digital core
- 2.5V or 3.3V for cable driver output supply
- GSPI serial control and monitoring interface
- Four configurable GPIO pins for control or status monitoring
- Wide operating temperature range: -40°C to +85°C
- Small 6mm x 4mm 40-pin QFN
- Pb-free/Halogen-free/RoHS and WEEE compliant package
- Pin compatible with the GS12181, GS12182, GS12081, and GS12281

Applications

SMPTE ST 424, SMPTE ST 292, SMPTE ST 259 interfaces requiring cable driving functionality. Typical applications: Cameras, Switchers, Distribution Amplifiers and Routers.

Description

The GS3281 is a low-power, multi-rate, re-timing cable driver supporting rates up to 3G-SDI. It is designed to receive 100Ω differential input signals, automatically recover the embedded clock from the digital video signal and re-time the incoming data, and transmit the re-timed signal over 75Ω coaxial cables. The 100Ω trace input supports up to 17dB of insertion loss.

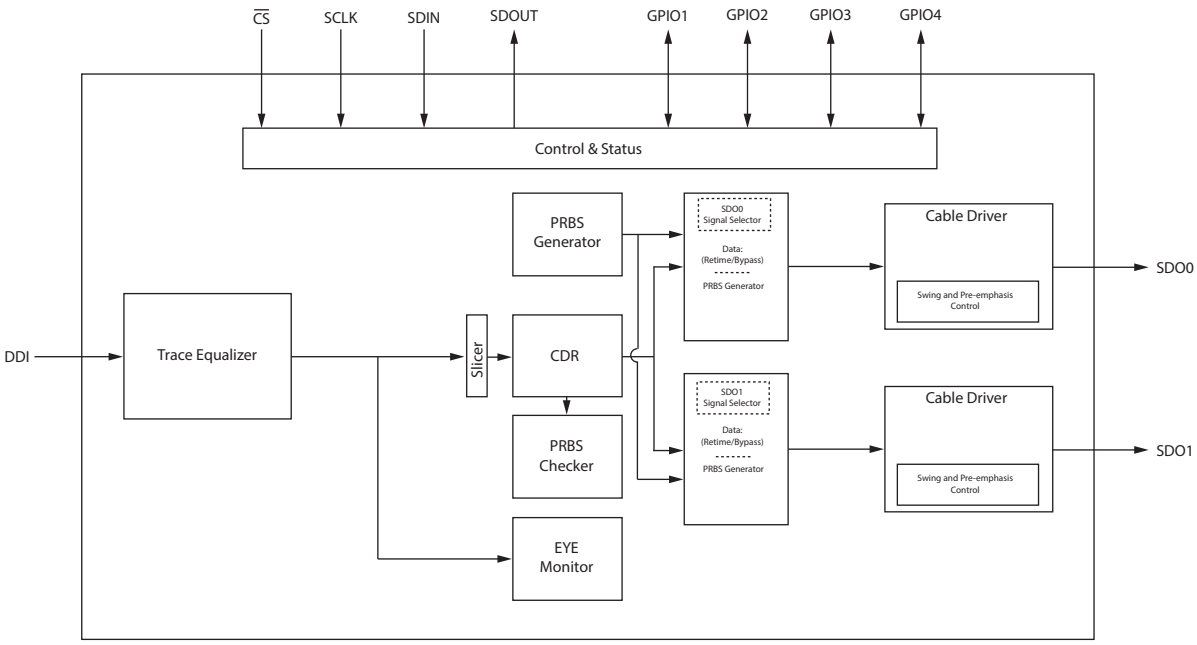
The integrated eye monitor provides non-disruptive mission mode analysis of the post equalized input signal. The 256x128 resolution scan matrix allows accurate signal analysis to speed up prototyping and enable field analysis.

Built in macros enable customizable cross section analysis and quick horizontal and vertical eye opening measurements.

With high phase consistency between scans and configurable space and time thresholds, algorithms can be deployed in the field to analyze long term signal quality variation (Bathtub Plot) to reduce costly system installation debug time for intermittent errors. The two cable drivers have highly configurable pre-emphasis and swing controls to compensate for long trace and connector losses. Additionally, automatic and user selectable output slew rate control is provided for each cable driver output.

The GS3281 is pin compatible with the GS12181 and GS12281 single input, and the GS12182 dual input 12G UHD-SDI Multi-rate Re-timing Cable Drivers, as well as the GS12081 12G UHD-SDI Multi-rate Cable Driver.

Note: For the GS3281 to be pin compatible with the GS12182, careful design considerations are required. Contact for your local Semtech FAE for details.



GS3281 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
2	038573	—	September 2017	Updated Section 4.3.2 and Section 5.
1	037774	—	August 2017	Added Device Power Up Sequence and Output Driver Data Rate Selection sections. Updated Host Initiated Device Reset section, and Section 6.1 Typical Application Circuit.
0	034284	—	November 2016	New Document.

Contents

1. Pin Out

1.1 GS3281 Pin Assignment

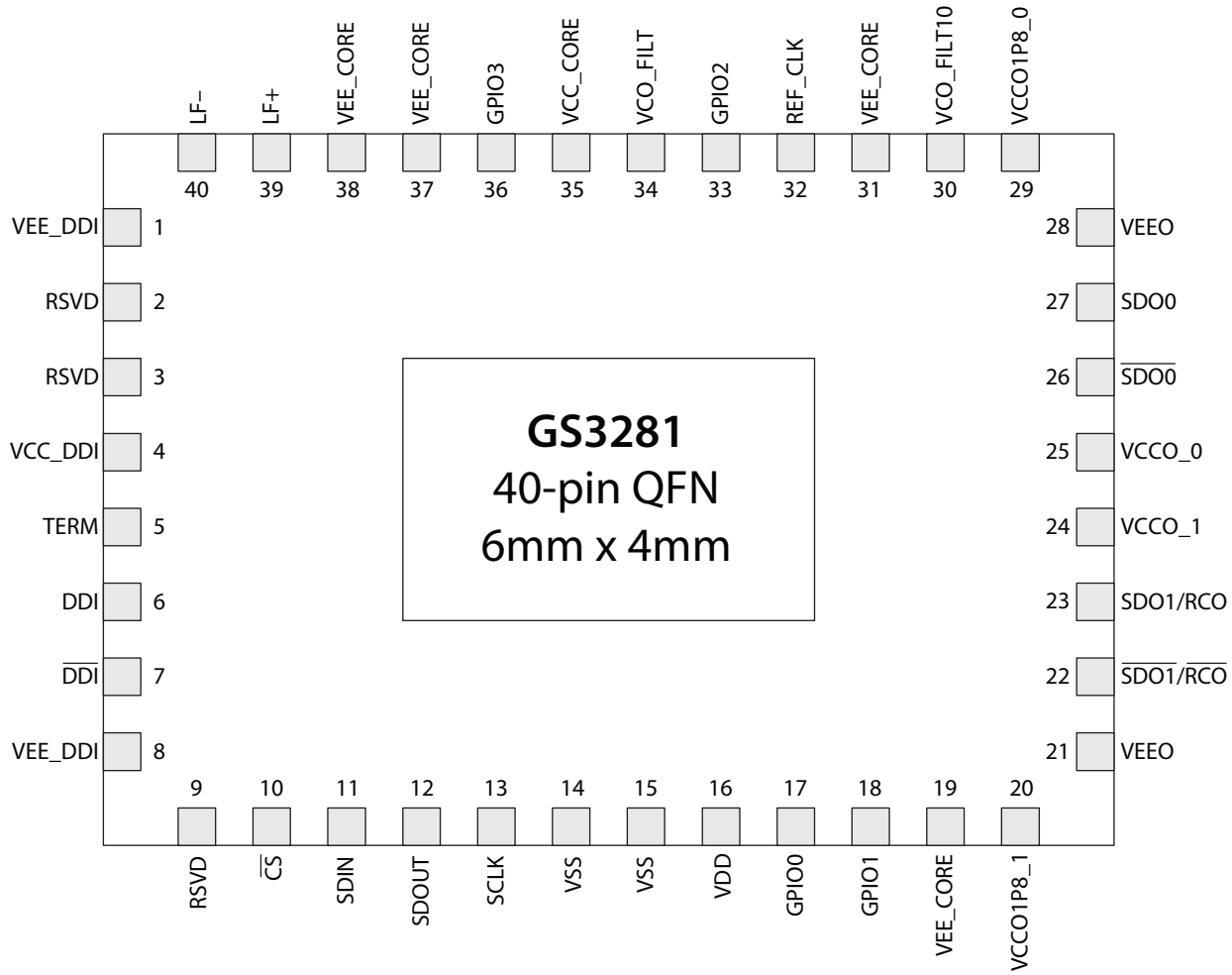


Figure 1-1: GS3281 Pin Assignment

1.2 GS3281 Pin Descriptions

Table 1-1: GS3281 Pin Descriptions

Pin Number	Name	Type	Description
1, 8	VEE_DDI	Power	Most negative power supply connection for the Trace Equalizer. Connect to ground.
2, 3, 9	RSVD	—	These pins may be left floating. Please contact your Semtech FAE for additional information on circuit compatibility with the GS3241.
4	VCC_DDI	Power	Most positive power supply connection for the Trace Equalizer. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
5	TERM	—	Input Common Mode termination. Decouple to ground. See Section 6.1 Typical Application Circuit for values.
6, 7	DDI, $\overline{\text{DDI}}$	Input	Serial digital differential input. Differential CML input with internal 100Ω termination.
10	$\overline{\text{CS}}$	Digital Input	Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-up. Active-LOW input. Refer to Section 4.9.1 for more details.
11	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.9.2 for more details.
12	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS output. Refer to Section 4.9.3 for more details.
13	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.9.4 for more details.
14, 15	VSS	Power	Most negative power supply for digital core logic. Connect to ground.
16	VDD	Power	Most positive power supply connection for digital core logic. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
17	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Default function: Direction = Output Signal = HIGH indicates LOS (Loss of Signal, inverse of Carrier Detect) Pin is 1.8V CMOS I/O, please refer to GPIO0_CFG for more information on how to configure GPIO0.

Table 1-1: GS3281 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
18	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Default function: Direction = Output Signal = HIGH indicates PLL is locked Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1.
19, 31, 37, 38	VEE_CORE	Power	Most negative power supply connection for the analog core. Connect to ground.
20	VCCO1P8_1	Power	Most positive power supply connection for cable driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
21, 28	VEEO	Power	Most negative power supply connection for the output drivers. Connect to ground.
22, 23	$\overline{\text{SDO1}}$/$\overline{\text{RCO}}$, SDO1/RCO	Output	Differential CML output with two internal 75Ω pull-ups. The data signal or PRBS generator can be selected for this output. The PRBS generator can be configured to generate a PRBS7 or a clock pattern. **Note:** If one of the two outputs is not used by the application, ensure that it is connected to ground through a capacitor and resistor. See Section 6.1 Typical Application Circuit for values.
24	VCCO_1	Power	Most positive power supply connection for the SDO1/ $\overline{\text{SDO1}}$ output driver. Connect to 2.5V or 3.3V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
25	VCCO_0	Power	Most positive power supply connection for the SDO/$\overline{\text{SDO0}}$ output driver. Connect to 2.5V or 3.3V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
26, 27	$\overline{\text{SDO0}}$, SDO0	Output	Differential CML output with two internal 75Ω pull-ups. The data signal or PRBS generator can be selected for this output. The PRBS generator can be configured to generate a PRBS7 or a clock pattern. **Note:** If one of the two outputs is not used by the application, ensure that it is connected to ground through a capacitor and resistor. See Section 6.1 Typical Application Circuit for values.
29	VCCO1P8_0	Power	Most positive power supply connection for cable driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
30	VCO_FILT10	Passive	VCO filter capacitor connection. Decouple to ground. See Section 6.1 Typical Application Circuit for values.
32	REF_CLK	Digital Input	Optional 27MHz reference input. 1.8V CMOS input with 100kΩ pull-down. Connect to ground if not used.

Table 1-1: GS3281 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
33	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. Default function: Direction = Input Signal = Set HIGH to put device in sleep Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2.
34	VCO_FILT	Passive	VCO filter capacitor connection. Decouple to ground. See Section 6.1 Typical Application Circuit for values.
35	VCC_CORE	Power	Most positive power supply connection for the analog core. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
36	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Default function: Direction = Input Signal = Set HIGH to disable SDO1/$\overline{\text{SDO1}}$ Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3.
39	LF+	Passive	Loop filter capacitor connection. Connect to pin 40 through capacitor. See Section 6.1 Typical Application Circuit for values.
40	LF-	Passive	Loop filter capacitor connection. Connect to pin 39 through capacitor. See Section 6.1 Typical Application Circuit for values.
Tab	—	—	Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation. It is not commended to connect device ground pins to the central paddle.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage—Core (VCC_DDI, VCC_CORE, VDD)	-0.5V to +2.2V
Supply Voltage—Output Driver (VCCO_0, VCCO_1)	-0.5V to +3.65V
Input ESD Voltage (any pin)	2kV HBM
Storage Temperature Range (T_S)	-50°C to +125°C
Input Voltage Range (DDI, $\overline{DDI}$)	-0.3 to (VCC_DDI +0.3)V
Input Voltage Range (GPIO2, GPIO3 REF_CLK)	-0.3 to (VCC_CORE +0.3)V
Input Voltage Range ($\overline{CS}$, SDIN, SCLK, VSS, VDD, GPIO0, GPIO1)	-0.3 to (VDD +0.3)V
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	VCC_DDI, VCC_CORE, VDD		1.71	1.8	1.89	V	—
Supply Voltage - Output Driver	VCCO_0, VCCO_1		2.38	2.5	2.63	V	—
			3.14	3.3	3.47	V	—
Power - Mission Mode (SDO0/$\overline{SDO0}$ enabled SDO1/$\overline{SDO1}$ disabled)	P_D	VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$,	—	375	—	mW	1
		VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$ with max pre-emphasis	—	390	—	mW	—
Power - Mission Mode (SDO0/$\overline{SDO0}$ disabled SDO1/$\overline{SDO1}$ disabled)	P_D		—	280	—	mW	1
Power - Sleep Mode	P_D	Sleep	—	40	54	mW	—
Supply Current - Cable Driver	I_{CCO_0}, I_{CCO_1}	VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$	—	23	34	mA	1,4
		VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$, with max pre-emphasis	—	29	38	mA	4
		VCCO_0 = 3.3V, Output Swing = 800mV$_{pp}$	—	24	33	mA	1,4
		VCCO_0 = 3.3V, Output Swing = 800mV$_{pp}$, with max pre-emphasis	—	30	37	mA	4
	I_{CCO1P8_0}, I_{CCO1P8_1}	Output Swing = 800mV$_{pp}$	—	20	28	mA	4
Supply Current – Analog Core	I_{CC_CORE}	CDR Locked to Rate	—	120	146	mA	—
		CDR Unlocked During Rate Search	—	143	—	mA	—
		PRBS Generator Enabled	—	71	—	mA	5,6
		PRBS Checker Enabled	—	58	—	mA	5
		Eye Monitor Enabled	—	70	—	mA	5
Supply Current - Trace Equalizer	I_{CC_DDI}		—	21	32	mA	—
Supply Current - Digital Logic	I_{DD}		—	15	18	mA	—

Table 2-2: DC Electrical Characteristics (Continued)

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
DDI Input Common Mode Voltage	V_{CMIN}		0.94	—	2.525	V	2
SDO Output Common Mode Voltage	V_{CMOUT}		—	$V_{CMOUT} = V_{CCO} - \Delta V_{SDO}/2$	—		—
DDI Input Termination		Differential	—	100	—	Ω	—
SDO Output Termination		Between SDO and GND	—	75	—	Ω	3
Input Voltage - Digital Pins ($\overline{CS}$, SDIN, SCLK, GPIO[0:3])	V_{IH}		0.65* VDD	—	VDD	V	—
	V_{IL}		0	—	0.35* VDD	V	—
Output Voltage - Digital Pins (SDOUT, GPIO[0:3])	V_{OH}	I_{OH} = -5mA	VDD - 0.45	—	—	V	—
	V_{OL}	I_{OL} = +5mA	—	—	0.45	V	—

Notes:

1. Pre-emphasis is disabled.
2. 0.94V is when trace EQ is DC coupled to upstream driver running from 1.2V supply, and 2.525V is when trace EQ is DC coupled to upstream driver running from 2.5V supply.
3. Applies to both SDO0 and SDO1.
4. The specifications provided are per symbol, not a combined value.
5. Current listed is an increase to ICC_CORE when stated condition is true.
6. Selected clock source = VCO free running.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VCC_DDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +2.5/3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR_{DDI}	—	0.001	—	2.97	Gb/s	—
Serial Output Voltage Swing	V_{SDO}	—	720	800	880	mV_{pp}	3
Differential Input Voltage Swing	ΔV_{DDI}	—	200	—	800	mV_{ppd}	—
Input Trace Equalization	—	3G	—	60	—	Inches	13dB, 7
		HD	—	60	—	Inches	6dB, 7
		SD	—	60	—	Inches	3dB, 7
		MADI	—	60	—	Inches	3dB, 7
Intrinsic Input Jitter Tolerance Square Wave Modulation	IIJT	MADI/SD/HD/3G	0.8	0.95	—	UI	—
PLL Lock Time – Asynchronous	t_{ALOCK}	Referenceless with MADI rate detection disabled	—	—	16.7	ms	5
		Referenceless with MADI rate detection enabled	—	—	32	ms	5
PLL Lock Time – Synchronous	t_{SLOCK}	SD	—	—	10	µs	5
		HD/3G	—	—	5	µs	5
SDO/$\overline{SDO}$ Rise/Fall Time	$t_{riseSDO}$, $t_{fallSDO}$	SD	400	—	1000	ps	6
		HD/3G	—	—	70	ps	6
		Bypass	—	—	40	ps	6
SDO/$\overline{SDO}$ Mismatch in Rise/Fall Time	—	SD	—	—	100	ps	6
		HD/3G	—	—	20	ps	6
SDO/$\overline{SDO}$ Eye Cross Shift	—	SD	—	—	5	%	6
		HD/3G	—	—	8	%	6
SDO/$\overline{SDO}$ Overshoot	—	—	—	—	10	%	6
Output Return Loss	—	5MHz to 1.485GHz	—	—	-17	dB	1
		1.485GHz to 2.97GHz	—	—	-12	dB	1
Serial Data Output Jitter (SDO/$\overline{SDO}$)	$t_{OJ(125Mb/s)}$	BW = default, Pattern = PRBS	—	0.015	0.08	UI_{pp}	2, 6, 8
	$t_{OJ(270Mb/s)}$		—	0.03	0.08	UI_{pp}	2, 6, 8
	$t_{OJ(1.485Gb/s)}$		—	0.03	0.08	UI_{pp}	2, 6, 8
	$t_{OJ(2.97Gb/s)}$		—	0.04	0.08	UI_{pp}	2, 6, 8
	$t_{OJ(Bypass)}$		—	0.13	0.20	UI_{pp}	2, 6, 8

Table 2-3: AC Electrical Characteristics (Continued)

VCC_DDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +2.5/3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Loop Bandwidth	$BW_{LOOP(125Mb/s)}$	Setting 0.0625x	—	10	—	kHz	4
		Setting 0.125x	—	20	—	kHz	4
		Setting 0.25x	—	38	—	kHz	4
		Setting 0.5x (Default)	—	76	—	kHz	4
		Setting 1.0x	—	150	—	kHz	4
	$BW_{LOOP(270Mb/s)}$	Setting 0.0625x	—	20	—	kHz	4
		Setting 0.125x	—	40	—	kHz	4
		Setting 0.25x	—	80	—	kHz	4
		Setting 0.5x	—	160	—	kHz	4
		Setting 1.0x (Default)	—	316	—	kHz	4
	$BW_{LOOP(1.485Gb/s)}$	Setting 0.0625x	—	110	—	kHz	4
		Setting 0.125x	—	220	—	kHz	4
		Setting 0.25x	—	440	—	kHz	4
		Setting 0.5x (Default)	—	876	—	kHz	4
		Setting 1.0x	—	1750	—	kHz	4
	$BW_{LOOP(2.97Gb/s)}$	Setting 0.0625x	—	220	—	kHz	4
		Setting 0.125x	—	440	—	kHz	4
		Setting 0.25x	—	880	—	kHz	4
		Setting 0.5x (Default)	—	1.76	—	MHz	4
		Setting 1.0x	—	3.5	—	MHz	4

Notes:

1. Values achieved with Semtech evaluation board and connector.
2. Measured using a clean input source.
3. Default driver swing Setting.
4. Please see PLL_LOOP_ BANDWIDTH_ 1 for the full range of loop bandwidth settings.
5. Please see Section 4.3.3.1for the further definition on Synchronous and Asynchronous Lock Time.
6. This specification applies to SDO0/$\overline{\text{SDO0}}$ and SDO1/$\overline{\text{SDO1}}$.
7. Trace insertion loss was measured with FR4 material using 7 mil stripline traces using a PRBS23 signal.
8. Measured under minimal trace loss conditions.

Note: For GSPI Timing see Table 4-10: GSPI Timing Parameters.

3. Input/Output Circuits

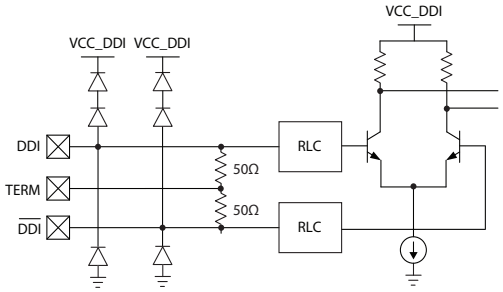


Figure 3-1: DDI, $\overline{\text{DDI}}$

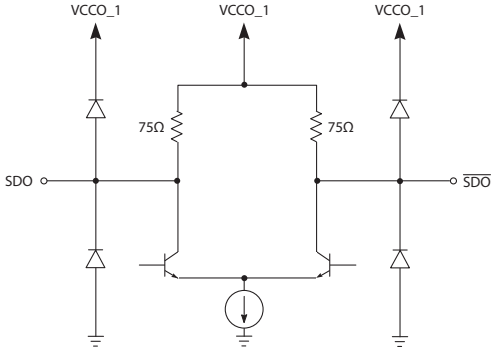


Figure 3-2: SDO0/$\overline{\text{SDO0}}$ and SDO1/$\overline{\text{SDO1}}$

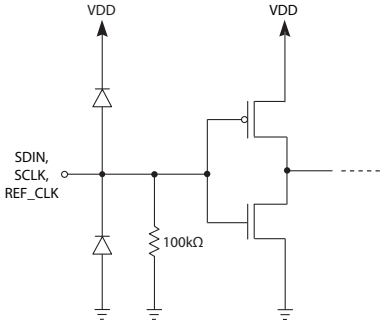


Figure 3-3: SDIN, SCLK, REF_CLK

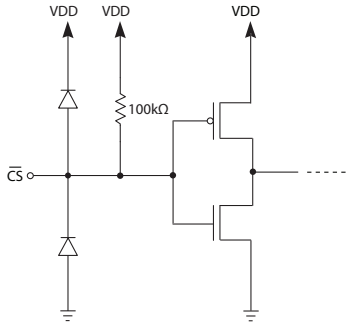


Figure 3-4: $\overline{\text{CS}}$

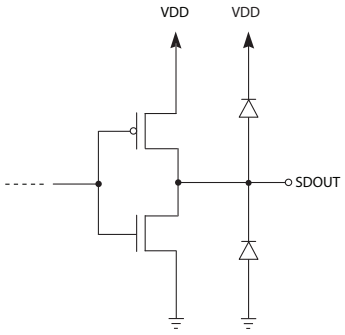


Figure 3-5: SDOUT

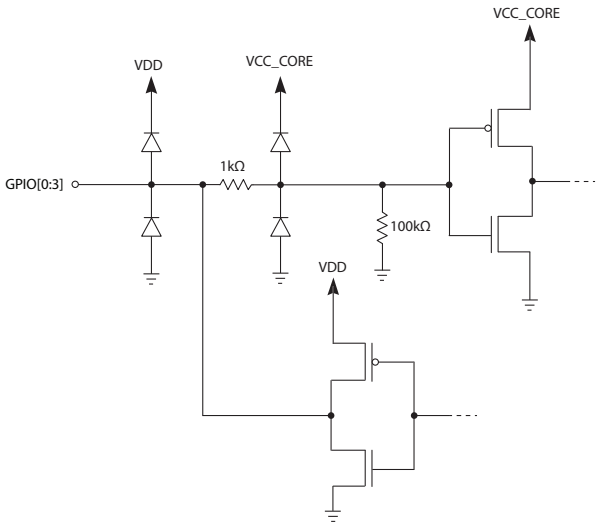


Figure 3-6: GPIO[0:3]

4. Detailed Description

4.1 Device Description

The GS3281 is a dual output SMPTE compliant re-timing cable driver with integrated 75Ω internal terminations. It includes a 100Ω differential trace equalizer to receive the outgoing signal from the system. The Trace Equalizer has offset correction and boost control, which can compensate for 17dB of insertion loss at 1.485GHz. The device includes a CDR which will lock to and retime valid SMPTE signals to produce extremely low output jitter, even at extended trace lengths. The CDR has extensive LBW control to enable jitter transfer optimization. To facilitate system testing, the device also includes 3D eye monitor, PRBS7 checker and generator. The Cable Driver has amplitude and pre-emphasis control to compensate for significant insertion loss between device output and BNC. The pre-emphasis control is two dimensional, where both pre-emphasis pulse amplitude and width adjustments can be made to help optimize for interconnect mismatches such as vias and connectors.

Note: The parameters referred to within Section 4.2.1 to Section 4.2.2 are linked to their respective registers in Table 4-1. For a complete list of registers and functions, please see Section 5.

4.1.1 Sleep Mode

To enable low power operation, the GS3281 has manual and automatic sleep mode control.

The default mode is automatic sleep mode on LOS (Loss of signal). The device can also be manually put into sleep mode. When the device is in sleep mode, all the core blocks are powered-down, except the host interface and carrier detect circuits. The cable driver can be configured to be disabled or muted during sleep.

The **CTRL_AUTO_SLEEP** and **CTRL_MANUAL_SLEEP** parameters in register 0x3, control the sleep mode of the device. The default value of the **CTRL_AUTO_SLEEP** parameter is 1_b (auto sleep). While in auto sleep mode, the **CTRL_MANUAL_SLEEP** parameter has no effect. To enable host control of the sleep mode, set the **CTRL_AUTO_SLEEP** parameter to 0_b manual sleep control. To prevent the device from entering sleep, set the **CTRL_MANUAL_SLEEP** parameter to 0_b (not sleep). To manually configure the device to sleep, set the **CTRL_MANUAL_SLEEP** parameter to 1_b (sleep).

The device can also be manually made to sleep through the *GPIO* pins. The default GPIO pin to control sleep is *GPIO2* (pin 33). Drive this pin HIGH to make the device sleep.

Section 4.6 describes the PRBS generator function. If the device's PRBS generator is intended to be used without a valid input signal, the device should be manually set to not sleep as described above. Without a valid input signal, an LOS status will be generated and the device will enter sleep mode and the PRBS block will be disabled. For a description of LOS thresholds and settings, see Section 4.2.2.

4.2 Trace Equalizer

The GS3281 features a differential input buffer with 100Ω differential input termination, which includes a trace equalizer that can be configured to compensate for up to 60" of 7-mil stripline of FR4 at 2.97Gb/s.

The differential input signal can be either DC-coupled or AC-coupled and is capable of operation with any binary coded signal that between 1Mb/s and 2.97Gb/s.

The input circuit is compatible with industry standard CML differential transmitters when DC coupled using industry standard 100Ω differential termination circuitry.

The trace equalizer includes an automatic input offset compensation circuit. This reduces offset-induced data jitter in the link due to asymmetric performance of DC-coupled upstream differential drivers. The input offset compensation circuit also improves the input sensitivity of the trace equalizer.

Note: The parameters referred to within Section 4.2.1 to Section 4.2.2 are linked to their respective registers in Table 4-1. For a complete list of registers and functions, please see Section 5.

4.2.1 Input Trace Equalization

The trace equalizer can compensate for up to 17dB of insertion loss at 1.485GHz in 8 increments, which can be adjusted through the **CFG_TREQ0_BOOST** parameter in control register 0x1E. The default value of **CFG_TREQ0_BOOST** is (2_h). Please refer to Figure 4-1 for recommended boost setting.

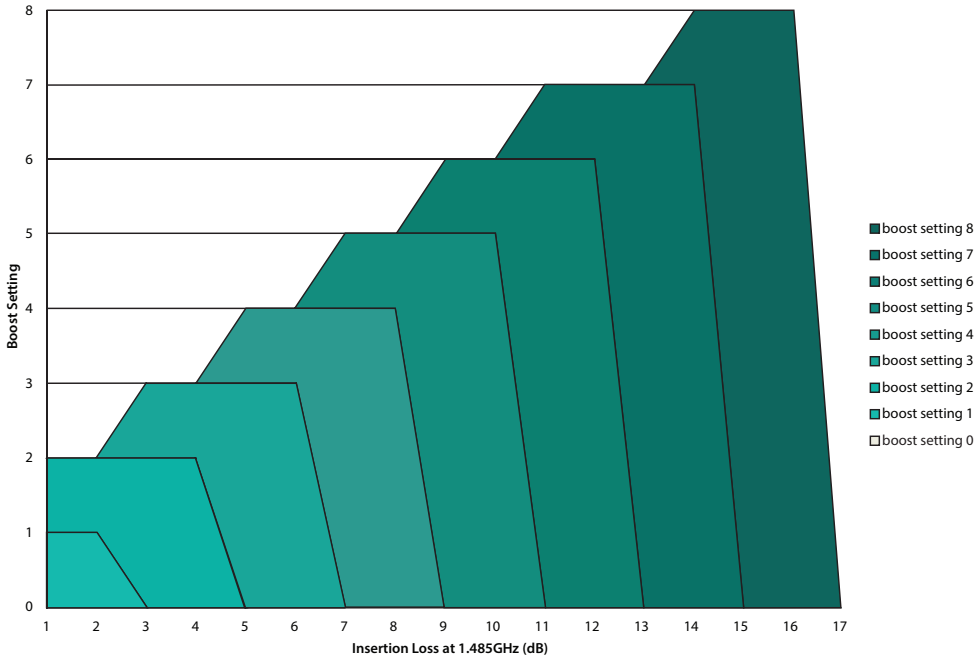


Figure 4-1: GS3281 Trace EQ Boost Setting Recommendation

By default at power up or after system reset, the trace equalizer is configured to compensate for up to 3" of 7-mil stripline in FR4 material at high frequencies.

Note: Although not a requirement, launch swing of $800mV_{ppd}$ is recommended for trace lengths longer than 5".

4.2.2 CD (Carrier Detect) and LOS (Loss of Signal)

LOS is the complement of CD and is used by various automatic control modes including mute on LOS, which will be covered in the output section of this document.

The default settings of the trace equalizer Carrier Detection sub-block should satisfy most applications; however the Carrier Detection mechanism in the trace equalizer is highly configurable and allows the system designer to optimize the sensitivity and hysteresis of the Carrier Detection mechanism to meet specific system requirements.

The trace equalizer Carrier Detect is reported by status parameter **STAT_PRI_CD** in register 0x87.

The first CD control parameter is **CFG_TREQ0_CD_BOOST** in register 0x1E. This parameter determines the method and therefore the level of equalization to be used on the input signal routed to the Carrier Detection sub-block. The default value is 0_b, which maximizes the level of equalization. Alternatively, the designer can choose to have this signal equalized at the same level as the main signal routed to the CDR by setting **CFG_TREQ0_CD_BOOST** to 1_b. The setting of this parameter has no impact on the main signal routed to the CDR.

The last two CD control parameters can be found in register 0x1F. Parameters **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TRE0Q_CD_DEASSERT_THRESH** set the Carrier Detect assert and de-assert thresholds to the input signal, which also defines the hysteresis of CD signal.

The default values of **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TREQ0_CD_DEASSERT_THRESH** are is 4_d and 3_d respectively. With the default settings, the minimum launch swing needed to assert the carrier detect is 200mV and it will be de-asserted when the signal level falls below 150mV.

The **STAT_PRI_CD** (Carrier Detect) parameter will be set to 0_b and the LOS will be set to 1_b whenever a new signal at the input does not exceed the assert threshold, or an existing signal falls below the de-assert threshold. The result is that the device will not indicate lock, and the outputs will mute (assuming Mute on LOS is left to its default value in the **CONTROL_OUTPUT_MUTE** register (0x49). See Section 4.7.5 for more details.

Given a differential input trace with 17dB of insertion loss at 1.485GHz and **CFG_TREQ0_CD_BOOST** = 0_b, Figure 4-2 illustrates the relationship between launch swing voltage, and minimum threshold setting to assert or de-asset Carrier Detect at all rates up to threshold setting at 2.97Gb/s.

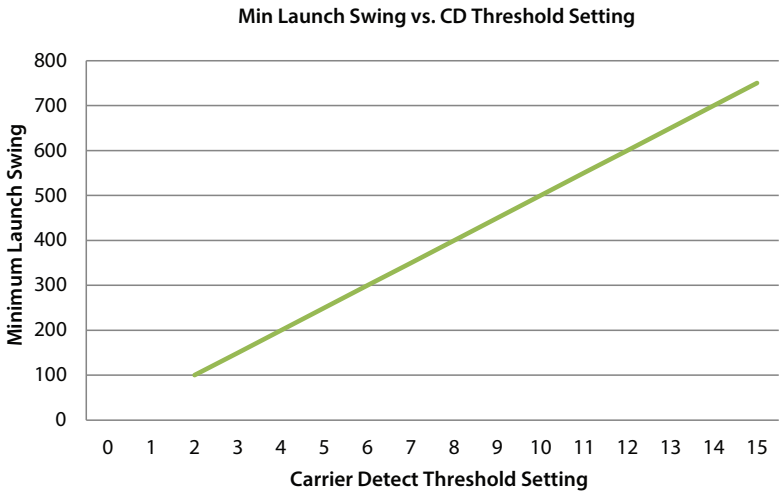


Figure 4-2: Input Voltage Vs. Carrier Detect Threshold Setting

Table 4-1: Trace Equalizer Configuration and Status Parameters

Register Address$_h$ and Name	Parameter Name	Description
1F, TREQ0_CD_ HYSTERESIS	CFG_TREQ0_CD_DEASSERT_THRESH	Sets the Carrier Detect de-assert threshold.
	CFG_TREQ0_CD_ASSERT_THRESH	Sets the Carrier Detect assert threshold.
1E, TREQ0_ INPUT_BOOST	CFG_TREQ0_CD_BOOST	Selects the boost method of the CD signal.
	CFG_TREQ0_BOOST	Sets the Trace Equalizer boost level.
84, STICKY_ COUNTS_0	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.
87, CURRENT_ STATUS_1	STAT_PRI_CD	Primary carrier detection status.

4.3 Serial Digital Re-timer (CDR)

The GS3281 includes an integrated CDR, whose purpose is to lock to a valid incoming signal from the trace equalizer stage and produce a lower jitter signal at the cable driver outputs. The CDR has the ability to lock to any of the following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), and 3G-SDI (2.97Gb/s). This includes the f/1.001 rates. The default settings of the re-timer block are optimal for most applications. However, the following controls allow the user to customize the behaviour of the re-timer: LBW control, Automatic and Manual Rate Detection.

Note: The parameters referred to within Section 4.3.1 to Section 4.3.3.1 are linked to their respective registers in Table 4-3. For a complete list of registers and functions, please see Section 5.

4.3.1 PLL Loop Bandwidth Control

The ratio of output peak-to-peak jitter to input peak-to-peak jitter of the CDR can be represented by a low-pass jitter transfer function, with a bandwidth equal to the PLL LBW. Although the default LBW settings for the GS3281 CDR are ideal for most SDI signals, the GS3281 allows the user to adjust the LBW for each MADI and SMPTE compliant rate.

Registers 0x0B through 0x0C contain the following parameters which allow the user to configure rate dependent LBW: **CFG_PLL_LBW_3G**, **CFG_PLL_LBW_HD**, **CFG_PLL_LBW_SD**, and **CFG_PLL_LBW_MADI**. The LBW settings are defined in terms of ratios of the nominal LBW. For each rate, where '1.0x' is the nominal LBW, the following ratios are available: 0.0625x, 0.125x, 0.25x, 0.5x, and 1.0x. Table 2-3 provides the specific loop bandwidths for each data rate and LBW setting. Lowering the LBW will lower the jitter amplitude above the LBW frequency. Although lower output jitter is desirable, the lower LBW may reduce the device's IJT to very high jitter that may be present outside the LBW.

4.3.2 Automatic and Manual Rate Detection

With the default rate detect setting, the CDR will automatically attempt to lock to any of following data rates: SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), and 3G-SDI (2.97Gb/s). This includes the f/1.001 rates. However, the CDR can be configured to only lock to a single rate, by setting the **CFG_AUTO_RATE_DETECT_ENA** and **CFG_MANUAL_RATE** parameters in register 0x06. In addition to **CFG_MANUAL_RATE**, with automatic rate detection enabled (**CFG_AUTO_RATE_DETECT_ENA** = 1), specific rates can be excluded from the rate detect list through the **CFG_RATE_ENA_<r>** rate disable mask parameter in 0x06, where r is the rate to be disabled. For details on specific settings, please see the RATE_ DETECT_ MODE register.

The **STAT_LOCK** parameter in register 0x86 will indicate that the CDR is locked when its value is 1_b and unlocked when its value is 0_b. The lock status can also be monitored externally on any *GPIO* pin, however it is the default mode for *GPIO1*, pin 18. The **STAT_DETECTED_RATE** parameter in register 0x87 will indicate the data rate at which the CDR is locked to. A value of 0_d in the **STAT_DETECTED_RATE** parameter indicates that the device is not locked, while values between 1_d and 4_d will indicate that the device is locked to one of the four available rates between MADI at 125Mb/s and 3G-SDI at 2.97Gb/s.

Table 4-2: Detected Data Rates

STAT_DETECTED_RATE [2:0]	Detected Data Rate
0	Unlocked
1	MADI (125Mb/s)
2	SD (270Mb/s)
3	HD (1.485Gb/s)
4	3G (2.97Gb/s)
5	Reserved
6	Reserved

If the CDR cannot lock to any of the valid rates in automatic mode or the selected rate in manual mode, the signal can automatically be bypassed to the output. If the CDR does lock to the incoming signal, the re-timed and bypassed (if manual bypass control enabled) signals are available at the appropriate output. See the Section 4.7 for more details.

4.3.3 Lock Time

4.3.3.1 Synchronous and Asynchronous Lock Time

Synchronous lock time is defined as the time it takes the device to re-lock to an existing signal that has been momentarily interrupted or to a new signal of the same data rate as the previous signal which has been quickly switched in.

Asynchronous lock time is defined as the time it takes the device to lock when a signal is first applied to the serial digital inputs, or when the signal rate changes. The asynchronous and synchronous lock times are defined in Table 2-3.

Note: To ensure synchronous lock times are met, the maximum interruption time of the signal is 10µs for an SD-SDI signal. HD, and 3G signals must have a maximum interruption time of 6µs. The new signal, after interruption, must have the same frequency as the original signal but may have an arbitrary phase.

Table 4-3: CDR Control and Status Parameters

Register Address$_h$ and Name	Parameter Name	Description
06, RATE_ DETECT_ MODE	CFG_AUTO_RATE_DETECT_ENA	Enables or disables the automatic rate detection mode of the CDR.
	CFG_MANUAL_RATE	Select a single rate for CDR rate detection when CFG_AUTO_RATE_DETECT_ENA is 0_b.
	CFG_RATE_ENA_3G	3G auto rate detection enable
	CFG_RATE_ENA_HD	HD auto rate detection enable
	CFG_RATE_ENA_SD	SD auto rate detection enable
	CFG_RATE_ENA_MADI	MADI auto rate detection enable
08, REF_CLK_ MODE	CFG_REF_CLK_MODE_MANUAL	Enables or disables external reference clock mode.
0B, PLL_LOOP_ BANDWIDTH_ 1	CFG_PLL_LBW_3G	Configures the Loop Bandwidth for 3G signals.
	CFG_PLL_LBW_HD	Configures the Loop Bandwidth for HD signals.
0C, PLL_LOOP_ BANDWIDTH_ 2	CFG_PLL_LBW_SD	Configures the Loop Bandwidth for SD signals.
	CFG_PLL_LBW_MADI	Configures the LBW for MADI signals.
11, GPIO1_CFG	CFG_GPIO1_FUNCTION	Sets the function of GPIO1.
	CFG_GPIO1_OUTPUT_ ENA	Sets the GPIO pin as either an output or an input.
85, STICKY_ COUNTS_1	STAT_CNT_PLL_LOCK_CHANGES	Counter showing the number of times the PLL lock status changed.
	STAT_CNT_RATE_CHANGES	Counter showing the number of times the PLL lock rate changed.
86, CURRENT_ STATUS_0	STAT_LOCK	The status of the PLL. Locked, or unlocked.
87, CURRENT_ STATUS_1	STAT_DETECTED_RATE	The rate at which the PLL is locked to.

4.4 PRBS Checker

The GS3281 includes an integrated PRBS checker, which can error check a PRBS7 signal out of the trace equalizer input blocks.

There are two modes of operation for the PRBS checker:

- Timed Mode: Used for precise measurements of up to ~3.334s.
  - In timed mode, the host sets the measurement time and executes the checker operation. The device ends the PRBS error check measurement when the timer expires, and the host reads back the measurement status and error count.
- Continuous Mode: Can be used for longer measurements but with less precision in the time interval.
  - In continuous mode, the host controls the starts and stops of the PRBS error checking operation then reads back the measurement status and error count.

Note: When working with the PRBS Checker, please note the following.

- The parameters referred to in Section 4.4.1 to Section 4.4.2 are briefly described and linked to their respective registers in Table 4-4. For a complete list of registers and functions, please see Section 5.
- The PRBS generator and checker can be active at the same time, however, the generator can not be looped back on itself for error checking.

4.4.1 Timed PRBS Check Measurement Procedure

For applications where measurement times are ~3.34s or less, the timed PRBS check mode is the most suitable. Alternatively, to achieve precise timing for lower BER signals, the timed PRBS check measurement can be repeated by the host and the total measurement time and error count is determined by summing the individual measurements.

In timed mode, the host sets the total measurement time by setting the **CFG_PRBS_CHECK_PREDIVIDER** and the **CFG_PRBS_CHECK_MEAS_TIME** parameters to the required values to achieve the total measurement time required by the application.

To perform a timed PRBS measurement, please complete the following steps:

1. Set the appropriate settings within **CFG_PRBS_CHECK_PREDIVIDER** and **CFG_PRBS_CHECK_MEAS_TIME** to achieve the total measurement time required by the application. The TMT (total measurement time) is determined by the following equation:

   TMT = CFG_PRBS_CHECK_PREDIVIDER * (CFG_PRBS_CHECK_MEAS_TIME *256+1) * (1/40MHz)

   Note: Using the default **CFG_PRBS_CHECK_PREDIVIDER** setting of 0 (pre-divider = 4) and **CFG_PRBS_CHECK_MEAS_TIME** setting of 3 (MEAS_TIME = 3), the TMT (total measurement time) is ~77µs per measurement.
2. Follow the steps outlined in Figure 4-3: Timed PRBS Check Flow.

4.4.2 Continuous PRBS Check Measurement Procedure

As previously mentioned, the maximum measurement time for a timed PRBS error measurement is ~3.35 seconds. For links with very low error rates, this time is insufficient to capture an adequate number of errors. For these situations, the continuous PRBS check measurement is more appropriate.

In continuous PRBS measurement mode, the measurement can run as long as required (assuming the device remains locked) to ensure the BER test level is met.

To perform a continuous PRBS measurement, please follow the steps outlined in the flowchart found within Figure 4-4: Continuous PRBS Check Flow.

Table 4-4: PRBS Checker Parameter Description

Register Address$_h$ and Name	Parameter Name	Description
50, PRBS_ CHK_CFG	CFG_PRBS_CHECK_PREDIVIDER	Selects pre-divider for PRBS check measurement timer.
	CFG_PRBS_CHECK_MEAS_TIME	Selects PRBS check measurement interval for timed measurements.
51, PRBS_CHK_ CTRL	CTRL_PRBS_CHECK_TIMED_CONT_B	Selects between timed and continuous type PRBS measurement.
	TRL_PRBS_CHECK_START	Used to start and stop PRBS measurements.
89, PRBS_ CHK_ ERR_CNT	STAT_PRBS_CHK_ERR_CNT	PRBS error count storage location.
8A, PRBS_ CHK_STATUS	STAT_PRBS_CHECK_STATUS	Status indication of PRBS checker.
	STAT_PRBS_CHECK_LAST_ABORT	Indication bit for PRBS successful completion or abort.

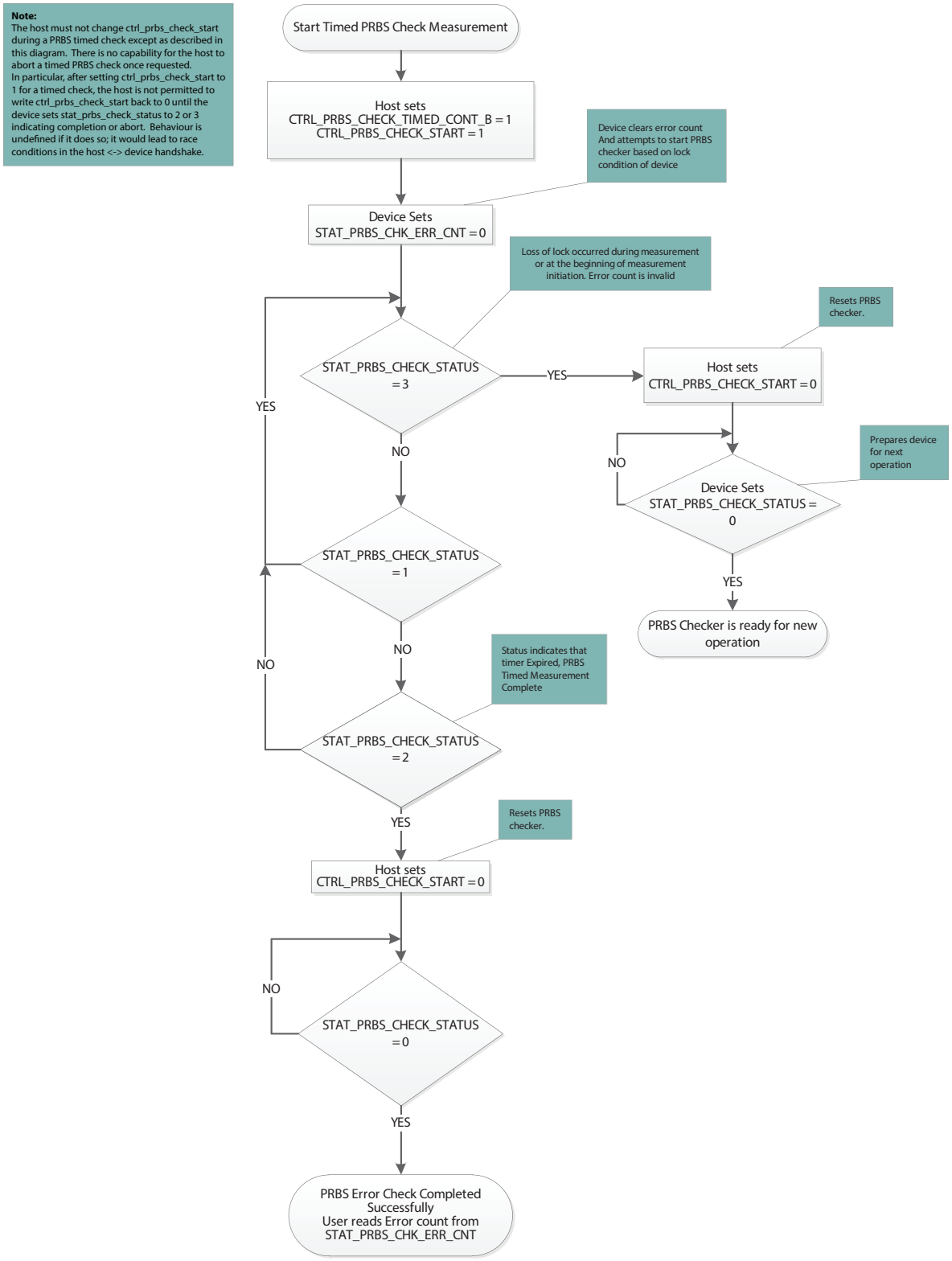


Figure 4-3: Timed PRBS Check Flow

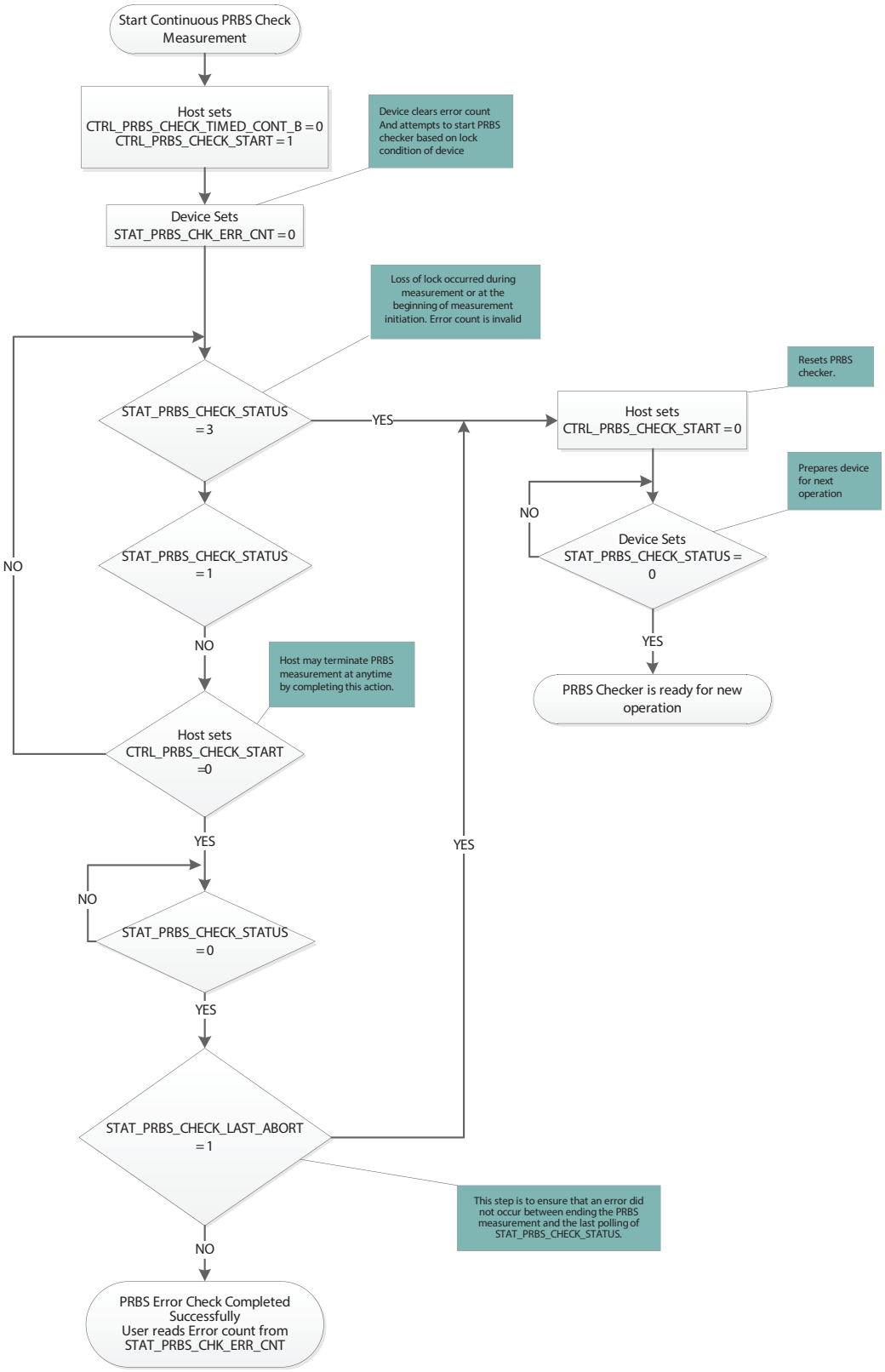


Figure 4-4: Continuous PRBS Check Flow