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GS3470

3G, HD, SD SDI Receiver

Key Features

- Operation at 2.970Gb/s, 2.970/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s, and 270Mb/s
- Supports SMPTE ST 425 (Level A and Level B), SMPTE ST 424, SMPTE 292, SMPTE ST 259-C, and DVB-ASI
- 2K and Multi-link UHD support
- Configurable Power-down modes
- Integrated Retimer
- Serial digital reclocked or non-reclocked loop-through output
- Integrated audio de-embedder for 8 channels of 48kHz audio and audio clock generation
- Ancillary data extraction
- Parallel data bus selectable as either 20-bit or 10-bit, SDR or DDR rate
- Comprehensive error detection and correction features
- Dual serial digital input buffer with 2x2 MUX
- Serial Loopback independently configurable to select either input
  - Performance optimized for 270Mb/s, 1.485Gb/s, and 2.97Gb/s.
- Dual/Quad Link 3G-SDI support with multiple GS3470 devices
- Output H, V, F, or CEA 861 timing signals
- GSPI host interface
- +1.2V digital core power supply, +1.2V and +1.8V analog power supplies, and selectable +1.8V or +2.5V I/O power supply
- -20ºC to +85ºC operating temperature range
- Low power operation — typically 220mW
- Small 9mm x 9mm 100-ball BGA package (0.80mm Ball Pitch)
- Pb-free, Halogen-free, and RoHS/ WEEE-compliant package

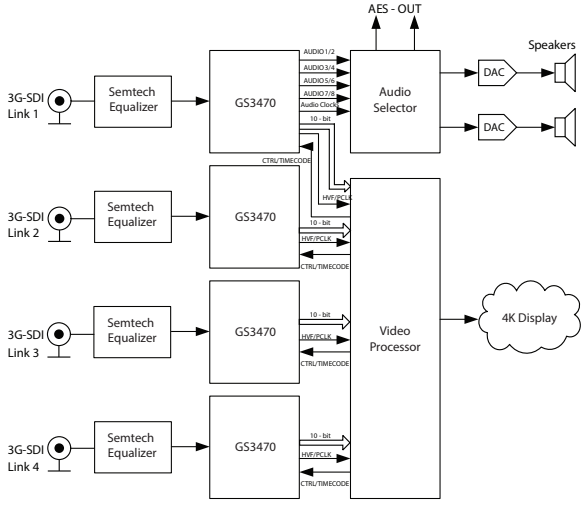
Applications

SDI Interfaces for:

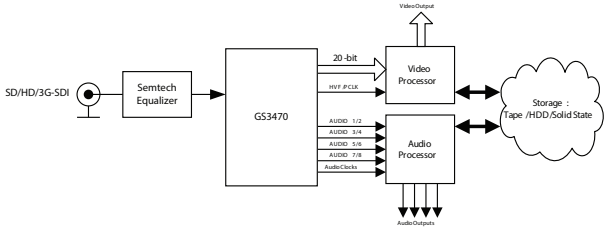
- Monitors
- DVRs
- Video Switchers
- Editing Systems
- Cameras
- Medical Imaging
- Aviation, Military, and Vehicular video systems

LED Wall and Digital Signage Applications

Application: 2160p50/60 (4K) Monitor



Application: Multi-format Video and Audio Processor



Description

The GS3470 is a multi-rate SDI Receiver which includes complete SMPTE processing. The SMPTE processing features can be bypassed to support signals with other coding schemes. Multi-link UHD can be supported when multiple GS3470 devices are used.

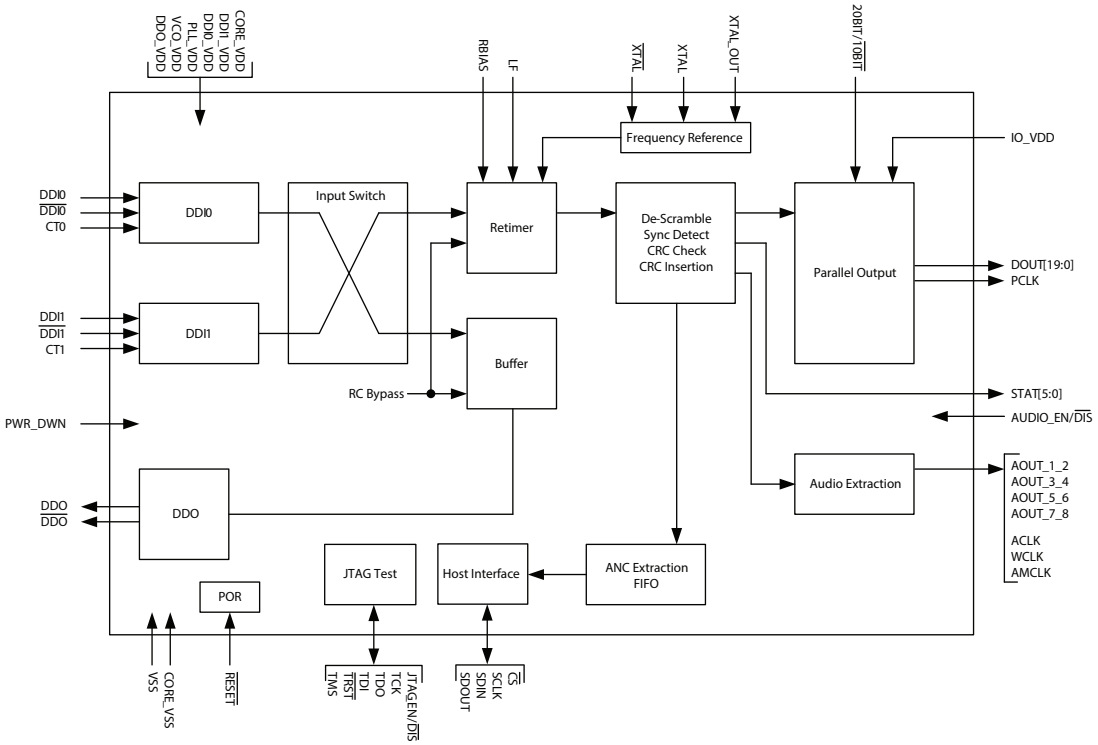
The device features a dual input buffer with a 2x2 MUX. The 2x2 MUX can select between either input for de-serialization and can route either of the two inputs to the serial loopback independently (reclocked or non-reclocked). In addition, the integrated Retimer with an internal VCO provides a wide Input Jitter Tolerance (IJT).

Configurable Power-down modes are available and allows for increased flexibility. Each Power-down mode enables power savings to a varying degree by selectively enabling or disabling key features. Some of the options available in Power-down mode are CSR access, PCLK, retimed DDO loop-through output, and non-retimed DDO loop-through output. Enabling or disabling each of these options will offer power consumption levels to suit the application's requirements.

The device has three other basic modes of operation which include:

- SMPTE mode
- DVB-ASI mode
- Data-Through mode

The GS3470 includes an audio de-embedder and audio clocks are internally generated. Up to eight channels (two audio groups) of serial digital audio may be extracted from the video data stream, in accordance with SMPTE ST 272-C and SMPTE ST 299.



GS3470 Functional Block Diagram

Revision History

Version	ECO	Date	Changes and/or Modifications
8	038819	September 2017	Updated to latest corporate template.
7	038315	September 2017	Updated several register and parameter names throughout Section 4. Updated Figure 4-1, Figure 6-1.
6	037007	May 2017	Updated Table 2-2, Table 2-3, Table 2-4, Table 4-27, Table 5-8. Changed all instances of DBUS to DOUT, and VSS/VEE to A_GND.
5	035144	March 2017	Added Figure 4-25 through Figure 4-30. Updated Section 4.16.1. Updated Table 2-2, Table 2-3, Table 2-4, Table 4-27.
4	033598	October 2016	Updated data sheet to reflect GS3471 modifications.
3	029850	March 2016	Updates to 1.1 Pin Assignment and 2.2 Recommended Operating Conditions.
2	029341	February 2016	Initial release changes.
1	028179	October 2015	Initial release changes.
0	020778	July 2014	New document.

Contents

1. Pin Out

1.1 Pin Assignment

Figure 1-1: Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	$\overline{\text{DDI0}}$	DDI0	CT0	RBIAS	XTAL	$\overline{\text{XTAL}}$	RSVD	PCLK	DOUT18	DOUT17
B	DDI0_VDD	DDI0_VDD	RSVD	RSVD	STAT0	STAT1	IO_VDD	DOUT19	DOUT16	DOUT15
C	PLL_VDD	PLL_VDD	LF	VCO_VDD	STAT2	STAT3	CORE_GND	DOUT12	DOUT14	DOUT13
D	DDI1_VDD	PLL_VDD	A_GND	VCO_VDD	STAT4	STAT5	$\overline{\text{TRST}}$	TDI	CORE_GND	IO_VDD
E	CT1	DDI1_VDD	A_GND	CORE_GND	CORE_VDD	CORE_VDD	TDO	TCK	DOUT10	DOUT11
F	DDI1	A_GND	A_GND	CORE_GND	CORE_GND	CORE_VDD	TMS	SDIN	DOUT8	DOUT9
G	$\overline{\text{DDI1}}$	A_GND	A_GND	CORE_GND	CORE_GND	CORE_VDD	SDOUT	SCLK	CORE_GND	IO_VDD
H	NC	NC	JTAG_EN/$\overline{\text{DIS}}$	WCLK	$\overline{\text{RESET}}$	BIT20/$\overline{\text{BIT10}}$	$\overline{\text{CS}}$	CORE_GND	DOUT6	DOUT7
J	DDO_VDD	DDO_VDD	PWR_DWN	AOUT_1_2	ACLK	AOUT_5_6	CORE_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{DDO}}$	DDO	AUDIO_EN/$\overline{\text{DIS}}$	AOUT_3_4	AMCLK	AOUT_7_8	IO_VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
A1, A2 G1, F1	$\overline{\text{DDI0}}$, DDI0 $\overline{\text{DDI1}}$, DDI1	SDI Input	Serial digital differential input. It is possible to DC-couple to upstream Semtech devices supporting 1.2V outputs. Additionally, devices with 1.8 and 2.5V outputs are supported through a 4.7µF capacitor in series with the $\overline{\text{DDI}}$/DDI input. Connect unused inputs to DDI_VDD through 1kΩ resistors.
A4	RBIAS	Analog Input	External resistor for the bias circuit. Connect to ground through 777Ω resistor.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description	
A5, A6	XTAL, $\overline{\text{XTAL}}$	Analog Input	Input connection for 27MHz crystal. When a reference clock input is used on $\overline{\text{XTAL}}$, do not connect XTAL.	
A8	PCLK	Output	Parallel data bus clock. Please refer to the Output Logic parameters in Table 2-3: DC Electrical Characteristics for logic level threshold and compatibility. Please refer to Table 4-5: GS3470 Output Data Formats for PCLK output rates.	
A7, B3, B4	RSVD	—	These pins are reserved, do not connect.	
B7, D10, G10, K7	IO_VDD	Power	Power connection for digital I/O. Connect to 1.8V or 2.5V DC digital.	
B8, A9, A10, B9, B10, C9, C10, C8, E10, E9, F10, F9, H10, H9, J10, J9, K10, K9, J8, K8	DOUT[19:0]	Output	Parallel data bus. Please refer to the Output Logic parameters in Table 2-3: DC Electrical Characteristics for logic level threshold and compatibility.	
			20-bit mode 20BIT_$\overline{\text{10BIT}}$ = HIGH	SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB_ASI = LOW): DOUT[19:10] — Luma data output for SD and HD data rates; Data Stream 1 for 3G data rate DOUT[9:0] — Chroma data output for SD and HD data rates; Data Stream 2 for 3G data rate Data-Through mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output
			10-bit mode 20BIT_$\overline{\text{10BIT}}$ = LOW (DOUT[19:10])	SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB_ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1&2 for 3G data rate DVB-ASI mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = HIGH): 8/10bit decoded DVB-ASI data for SD data rates Data-Through mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output **Note 1:** When in 10-bit mode, DOUT[9:0] are set to 0. **Note 2:** When in 10-bit mode, leave unused output pins unconnected.
C1, C2, D2	PLL_VDD	Power	Power pins for the Retimer PLL. Connect to 1.2V DC analog.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
C3	LF	Analog Input	Loop Filter component connection. Connect as per Typical Application Circuit.
C4, D4	VCO_VDD	Power	Power pin for the VCO. Connect to RC filter as per Typical Application Circuit. Connect to a 1.2V ±5% analog supply through a 24Ω ±1% resistor. Additionally, connect to ground through a 10µF capacitor.
C7, D9, E4, F4, F5, G4, G5, G9, J7, H8	CORE_GND	Power	Ground pins for digital circuitry. Connect to digital ground.
D3, E3, F2, F3, G2, G3	A_GND	Power	Ground pins for analog circuitry. Connect to analog ground.
D1, E2 B1, B2	DDI1_VDD DDI0_VDD	Power	Power pins for SDI buffer. Connect to 1.2V DC analog.
D6, D5, C6, C5, B6, B5	STAT[5:0]	Digital Output	Multi-function status outputs. See Section 4.11 for more details on assigning signals to STAT pins. Please refer to the Output Logic parameters in Table 2-3: DC Electrical Characteristics for logic level threshold and compatibility. Each of the STAT[5:0] pins can be configured individually to output one of the following signals. See Table 4-7: Output Signals Available on Programmable Multi-Function Pins for Status Signal Selection Codes and Default Output Pins.
D7	$\overline{\text{TRST}}$	Digital Input, Internal Pull-down	JTAG interface reset. Digital active-low reset input. Used to reset the JTAG test sequence. When LOW, the JTAG test sequence is reset. When HIGH, normal operation of the JTAG test sequence resumes.
D8	TDI	Digital Input, Internal Pull-up	JTAG interface Test Data Input. Serial instructions and data are received on this pin.
E1, A3	CT[1:0]	Analog Input	Decoupling for internal SDI termination resistors. Connect as per Typical Application Circuit. When an input is not used, its corresponding CT pin can be left unconnected.
E5, E6, F6, G6	CORE_VDD	Power	Power connection for device core. Connect to 1.2V DC digital.
E7	TDO	Digital Output	JTAG interface Test Data Output. TDO is the serial output for test instructions and data.
E8	TCK	Digital Input	JTAG interface Test Clock input. The test clock input provides the clock for the test logic of this device.
F7	TMS	Digital Input, Internal Pull-up	JTAG interface Test Mode Select input. This signal is decoded by the internal TAP controller to control test operations.
F8	SDIN	Digital Input	Serial Digital Data Input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. When GSPI is not used, SDIN should be tied HIGH or LOW to minimize noise.
G7	SDOUT	Digital Output	Serial Digital Data Output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Active-high output. When GSPI is not used, leave unconnected.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
G8	SCLK	Digital Input	Serial Data Clock input. Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. When GSPI is not used, SCLK should be tied HIGH or LOW to minimize noise.
H1, H2	NC	—	No connect. Pins are not connected internally.
H3	JTAG_EN/$\overline{\text{DIS}}$	Digital Input, Internal Pull-down	JTAG interface reset. Digital active-high to enable JTAG communications. When HIGH, JTAG operational mode is enabled. When LOW, JTAG operational mode is disabled.
H4	WCLK	Output	48kHz word clock for audio. When not used, leave unconnected.
H5	$\overline{\text{RESET}}$	Digital Input, Internal Pull-up	Device reset signal. When LOW, the device will be set to default conditions.
H6	BIT20/$\overline{\text{BIT10}}$	Digital Input, Internal Pull-up	Control signal input. Used to select the output bus width. HIGH = 20-bit, LOW = 10-bit. Please refer to the Input Logic parameters in Table 2-3: DC Electrical Characteristics for logic level threshold and compatibility.
H7	$\overline{\text{CS}}$	Digital Input	Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Active-low input. When GSPI is not used, connect $\overline{\text{CS}}$ to IO_VDD.
J1, J2	DDO_VDD	Power	Power pin for the serial digital output 50Ω buffer. Connect to 1.2V or 1.8V DC analog.
J3	PWR_DWN	Digital Input, Internal Pull-down	When HIGH, places the device in a power-down state.
J4, K4, J6, K6	AOUT_1_2, AOUT_3_4, AOUT_5_6, AOUT_7_8	Output	Serial Audio Outputs. When not in use, leave unconnected.
J5	ACLK	Output	64fs sample clock for audio. When not in use, leave unconnected.
K1, K2	$\overline{\text{DDO}}$, DDO	Digital Output	Differential serial digital outputs. It is possible to DC-couple to downstream Semtech devices supporting 2.5V inputs. When not in use, leave unconnected.
K3	AUDIO_EN/$\overline{\text{DIS}}$	Digital Input, Internal Pull-up	Control signal input. When HIGH, enables audio extraction. When LOW, disables audio extraction. Please refer to the Input Logic parameters in Table 2-3: DC Electrical Characteristics for logic level threshold and compatibility.
K5	AMCLK	Output	Oversampled master clock for audio (128fs, 256fs, 512fs selectable). When not in use, leave unconnected.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +2.8V
Supply Voltage, Analog 1.2V (PLL_VDD, VCO_VDD, DDI_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 1.8V (DDO_VDD)	-0.3V to +2.0V
Input Voltage Range (Digital Inputs)	-0.3V to IO_VDD + 0.3V
Ambient Operating Temperature (T_A)	-20°C to +85°C
Storage Temperature (T_{STG})	-50°C to +125°C
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	3kV

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Temperature Range, Ambient	T_A	—	-20	—	+85	°C
Supply Voltage, Digital Core	CORE_VDD	—	1.14	1.2	1.26	V
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V
		2.5V mode	2.38	2.5	2.63	V
Supply Voltage, PLL	PLL_VDD	—	1.14	1.2	1.26	V
Supply Voltage, VCO	VCO_VDD	—	1.14	1.2	1.26	V
Supply Voltage, Serial Digital Input	DDI0_VDD, DDI1_VDD	—	1.14	1.2	1.26	V
Supply Voltage, CD Buffer	DDO_VDD	1.2V mode	1.14	1.2	1.26	V
		1.8V mode	1.71	1.8	1.89	V
Serial Input Data Rate		—	270	—	2970	Mb/s

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
DDI0_VDD, DDI1_VDD Supply Current	I_{DDI}	1.2V	0.01	0.02	0.03	mA	—
IO_VDD Supply Current	I_{IO}	1.8V	7.4	9.2	10.8	mA	—
		2.5V	12.3	12.5	12.8	mA	—
DDO_VDD Supply Current	I_{DDO}	1.2V	7.4	9.1	10.7	mA	—
		1.8V	7.4	9.1	10.7	mA	—
VCO_VDD Supply Current	I_{VCO}	1.2V	7.0	7.8	9.4	mA	—
PLL_VDD Supply Current	I_{PLL}	1.2V	50.3	63.0	74.5	mA	—
CORE_VDD Supply Current	I_{CORE}	1.2V	17.7	20.3	22.2	mA	—
Total Device Power DDO_VDD = 1.2V IO_VDD = 1.8V (Audio Enabled)	P	10-bit 3GA	160	191	227	mW	—
		10-bit 3GB	135	158	192	mW	—
		20-bit 3GA	137	161	193	mW	—
		20-bit 3GB	154	184	230	mW	—
		10-bit HD	125	148	179	mW	—
		20-bit HD	109	129	170	mW	—
		10/20-bit SD	97	109	141	mW	—
		DVB-ASI	—	103	—	mW	—
		Sleep	3.3	5	11.3	mW	—
		Standby with DDO Retimed	82	105	121	mW	—
Total Device Power DDO_VDD = 1.8V IO_VDD = 2.5V (Audio Enabled)	P	10-bit 3GA	275	287	300	mW	—
		10-bit 3GB	224	230	237	mW	—
		20-bit 3GA	219	228	241	mW	—
		20-bit 3GB	276	286	325	mW	—
		10-bit HD	211	218	221	mW	—
		20-bit HD	165	174	209	mW	—
		10/20-bit SD	125	132	164	mW	—
		DVB-ASI	—	121	—	mW	—
		Sleep	7.1	10.1	16.9	mW	—
		Standby with DDO Retimed	108	127	163	mW	—

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Digital I/O							
Input Logic LOW	V_{IL}	2.5V or 1.8V operation	—	—	0.3 x IO_VDD	V	—
Input Logic HIGH	V_{IH}	2.5V or 1.8V operation	0.7 x IO_VDD	—	—	V	—
Output Logic LOW	V_{OL}	I_{OL} = 8mA,1.8V operation	—	—	0.41	V	—
		I_{OL} = 8mA, 2.5V operation	—	—	0.29	V	—
Output Logic HIGH	V_{OH}	I_{OL} = 8mA,1.8V operation	1.49	—	—	V	—
		I_{OL} = 8mA, 2.5V operation	2.27	—	—	V	—
Serial Input							
Serial Input Common Mode Voltage	—	AC or DC-coupled	0.90	0.96	1.06	V	—
Serial Output							
Serial Output Common Mode Voltage	—	50Ω load	—	DDO_VDD - $V_{swing}/2$	—	V	1

Note:

1. Serial output swing limited when using DDO_VDD = 1.2V.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency: AUDIO_EN = 1, SMPTE mode, IOPROC_EN = 1	—	3G (Level A)	65	67	69	PCLK	—
		3G (Level B)	141	144	147	PCLK	—
		HD	65	67	69	PCLK	—
		SD	37	39	41	PCLK	—
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 1	—	3G (Level A)	28	30	32	PCLK	—
		3G (Level B)	63	65	67	PCLK	—
		HD	25	27	29	PCLK	—
		SD	25	27	29	PCLK	—
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 0	—	3G (Level A)	20	22	24	PCLK	—
		3G (Level B)	47	50	53	PCLK	—
		HD	21	23	25	PCLK	—
		SD	19	21	23	PCLK	—
Device Latency: AUDIO_EN = 0, SMPTE bypass, IOPROC_EN = 0	—	3G (Level A)	11	13	15	PCLK	—
		3G (Level B)	11	13	15	PCLK	—
		HD	11	13	15	PCLK	—
		SD	11	13	15	PCLK	—
Device Latency: DVB-ASI	—	—	12	14	16	PCLK	—
Reset Time	t_{reset}	—	1	—	—	ms	—
Parallel Output							
Parallel Clock Frequency	f_{PCLK}	3G/ HD (10-bit)	—	148.5 or 148.5/ 1.001	—	MHz	—
		HD (20-bit), 10-bit DDR	—	74.25 or 74.25/ 1.001	—	MHz	—
		SD (20-bit), 10-bit DDR	—	13.5	—	MHz	—
		SD (10-bit)	—	27	—	MHz	—

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Parallel Clock Duty Cycle	DC_{PCLK}	—		—	50	—	%	—
Output Data Hold Time (1.8V)	t_{oh}	6pF C_{load}	SPI	1.5	—	—	ns	—
			AUDIO	1.5	—	—	ns	—
		3G 10-bit 6pF C_{load}	DOUT	0.3	—	—	ns	—
			STAT	0.3	—	—	ns	—
		3G 20-bit 6pF C_{load}	DOUT	0.5	—	—	ns	—
			STAT	0.5	—	—	ns	—
		HD 10-bit 6pF C_{load}	DOUT	1.5	—	—	ns	—
			STAT	1.5	—	—	ns	—
		HD 20-bit 6pF C_{load}	DOUT	5.0	—	—	ns	—
			STAT	5.0	—	—	ns	—
		SD 10-bit 6pF C_{load}	DOUT	15.0	—	—	ns	—
			STAT	15.0	—	—	ns	—
		SD 20-bit 6pF C_{load}	DOUT	30.0	—	—	ns	—
			STAT	30.0	—	—	ns	—
Output Data Hold Time (2.5V)	t_{oh}	6pF C_{load}	SPI	1.5	—	—	ns	—
			AUDIO	1.5	—	—	ns	—
		3G 10-bit 6pF C_{load}	DOUT	0.3	—	—	ns	—
			STAT	0.3	—	—	ns	—
		3G 20-bit 6pF C_{load}	DOUT	0.5	—	—	ns	—
			STAT	0.5	—	—	ns	—
		HD 10-bit 6pF C_{load}	DOUT	1.5	—	—	ns	—
			STAT	1.5	—	—	ns	—
		HD 20-bit 6pF C_{load}	DOUT	4.0	—	—	ns	—
			STAT	4.0	—	—	ns	—
		SD 10-bit 6pF C_{load}	DOUT	15.0	—	—	ns	—
			STAT	15.0	—	—	ns	—
		SD 20-bit 6pF C_{load}	DOUT	30.0	—	—	ns	—
			STAT	30.0	—	—	ns	—

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Delay Time (1.8V)	t_{od}	15pF C_{load}	SPI	—	—	28.0	ns	—
			AUDIO	—	—	10.0	ns	—
		3G 10-bit 15pF C_{load}	DOUT	—	—	2.4	ns	—
			STAT	—	—	2.8	ns	—
		3G 20-bit 15pF C_{load}	DOUT	—	—	6.0	ns	—
			STAT	—	—	6.3	ns	—
		HD 10-bit 15pF C_{load}	DOUT	—	—	4.0	ns	—
			STAT	—	—	4.2	ns	—
		HD 20-bit 15pF C_{load}	DOUT	—	—	14.2	ns	—
			STAT	—	—	14.4	ns	—
		SD 10-bit 15pF C_{load}	DOUT	—	—	21.0	ns	—
			STAT	—	—	21.0	ns	—
		SD 20-bit 15pF C_{load}	DOUT	—	—	40.0	ns	—
			STAT	—	—	40.0	ns	—
Output Data Delay Time (2.5V)	t_{od}	15pF C_{load}	SPI	—	—	28.0	ns	—
			AUDIO	—	—	10.0	ns	—
		3G 10-bit 15pF C_{load}	DOUT	—	—	2.3	ns	—
			STAT	—	—	2.8	ns	—
		3G 20-bit 15pF C_{load}	DOUT	—	—	6.0	ns	—
			STAT	—	—	6.3	ns	—
		HD 10-bit 15pF C_{load}	DOUT	—	—	3.8	ns	—
			STAT	—	—	4.2	ns	—
		HD 20-bit 15pF C_{load}	DOUT	—	—	13.0	ns	—
			STAT	—	—	13.5	ns	—
		SD 10-bit 15pF C_{load}	DOUT	—	—	21.0	ns	—
			STAT	—	—	21.0	ns	—
		SD 20-bit 15pF C_{load}	DOUT	—	—	40.0	ns	—
			STAT	—	—	40.0	ns	—
Output Data Rise/Fall Time (1.8V)	t_r/t_f	6pF C_{load}	STAT	—	—	3.1	ns	—
			DOUT	—	—	3.1	ns	—
			AUDIO	—	—	3.3	ns	—

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Rise/Fall Time (2.5V)	t_r/t_f	6pF C_{load}	STAT	—	—	2.1	ns	—
			DOUT	—	—	2.1	ns	—
			AUDIO	—	—	2.2	ns	—
Serial Digital Input								
Serial Input Data Rate	DR_{SDI}	—		0.27	—	2.97	Gb/s	—
Serial Input Swing	ΔV_{DDI}	Differential with 100Ω load		200	400	1000	mV_{ppd}	—
Serial Input Jitter Tolerance	SIJT	Nominal loop bandwidth Square wave mod.		0.8	—	—	UI	—
Serial Digital Output								
Serial Output Data Rate	DR_{DDO}	—		0.27	—	2.97	Gb/s	—
Serial Output Swing	ΔV_{DDO}	Differential with 100Ω load		200	400	1000	mV_{ppd}	2
Serial Output Rise Time 20% ~ 80%	tr_{DDO}	—		—	112	135	ps	—
Serial Output Fall Time 20% ~ 80%	tf_{DDO}	—		—	114	135	ps	—
Rise/ Fall Mismatch		—		—	2	8	ps	—
Serial Output Intrinsic Jitter	t_{OJ}	3G PRBS		0.05	0.06	0.08	UI	3
		HD PRBS		0.03	0.04	0.05	UI	3
		SD PRBS		0.01	0.02	0.03	UI	3
Serial Output Duty Cycle Distortion	DCD_{SDD}	3G		3	5	10	ps	—
		HD		1	5	7	ps	—
		SD		1	2	5	ps	—
Asynchronous Lock Time	—	—		—	—	750	µs	—
Lock Time from Power-up	—	After 20 minutes at -20°C		—	725	—	ms	—

Notes:

1. Serial output swing limited when using DDO_VDD = 1.2V
2. Serial output swing can be adjusted through GSPI.
3. Retiming enabled.

3. Input/Output Circuits

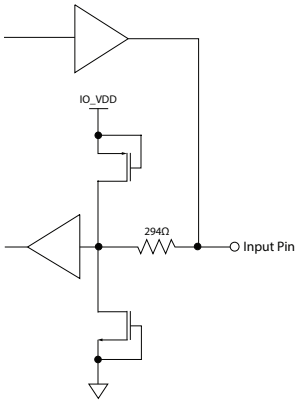


Figure 3-1: Bidirectional Digital Input/Output Pin Configured as an Input (SDIN, $\overline{CS}$, SCLK)

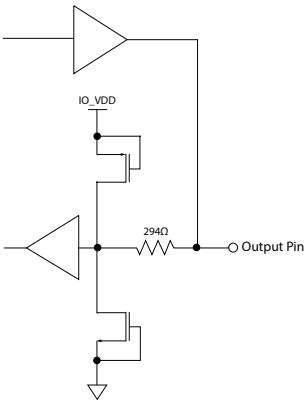


Figure 3-2: Bidirectional Digital Input/Output Pin Configured as an Output (AMCLK, TDO, SDOUT, WCLK, AOUT_1_2, AOUT_3_4, AOUT_5_6, AOUT_7_8, ACLK)

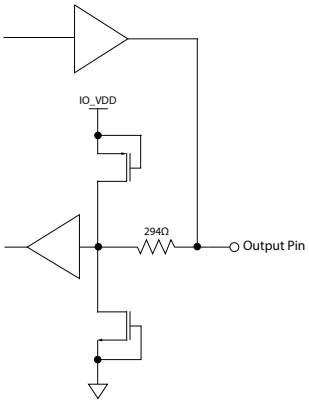


Figure 3-3: Bidirectional Digital Input/Output Pin Configured as an Output with Programmable Drive Strength (DOUT[19:0], PCLK, STAT[5:0])

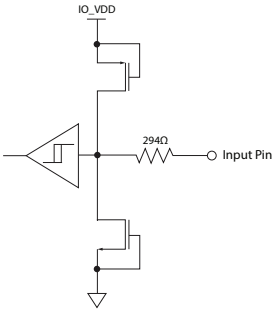


Figure 3-4: Digital Input with Schmitt Trigger and 100kΩ Internal Pull-Up (AUDIO_EN/$\overline{DIS}$, TDI, TMS, $\overline{RESET}$, BIT20/$\overline{BIT10}$)

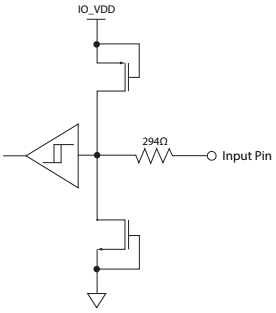


Figure 3-5: Digital Input with Schmitt Trigger and 100kΩ Internal Pull-Down ($\overline{TRST}$, JTAG_EN/$\overline{DIS}$, PWR_DWN)

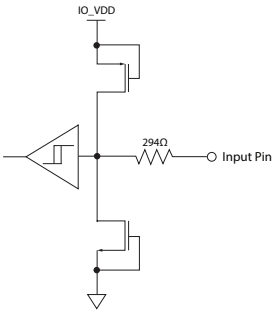


Figure 3-6: Digital Input with Schmitt Trigger (TCK)

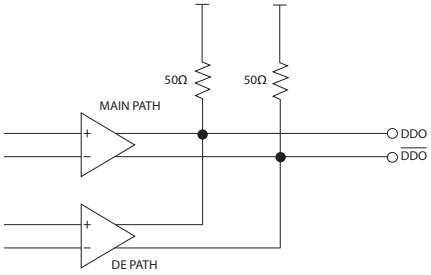


Figure 3-7: DDO/$\overline{\text{DDO}}$

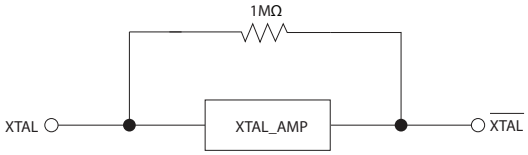


Figure 3-8: XTAL/$\overline{\text{XTAL}}$

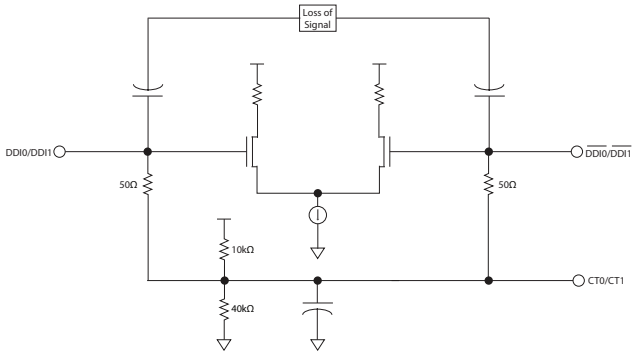


Figure 3-9: DDI0/$\overline{\text{DDI0}}$, DDI1/$\overline{\text{DDI1}}$, CT[1:0]

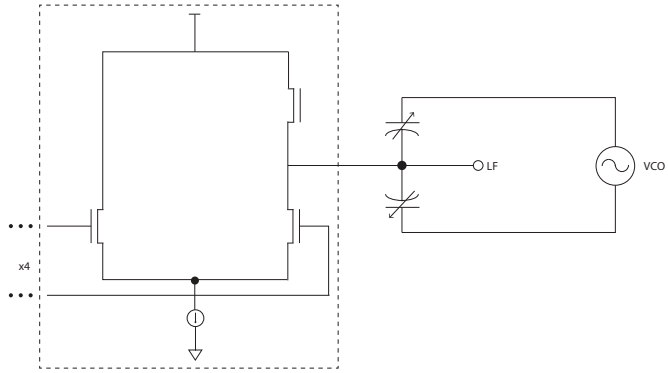


Figure 3-10: LF

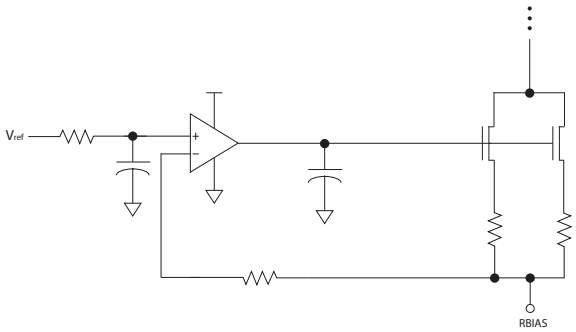


Figure 3-11: RBIAS

4. Detailed Description

4.1 Functional Overview

The GS3470 includes a dual serial digital input buffer with 2x2 MUX, an integrated retimer, serial data loop through output, robust serial-to-parallel conversion, integrated SMPTE video processing, and additional processing functions such as audio extraction, ancillary data extraction, EDH support, and DVB-ASI decoding.

The serial digital input buffer with 2x2 MUX offers a lot of flexibility for use in default and various Power-down modes. From Figure 4-1 below, the top two blocks shown represent input select with loopback, while the bottom two allow input select with separate loopback select.

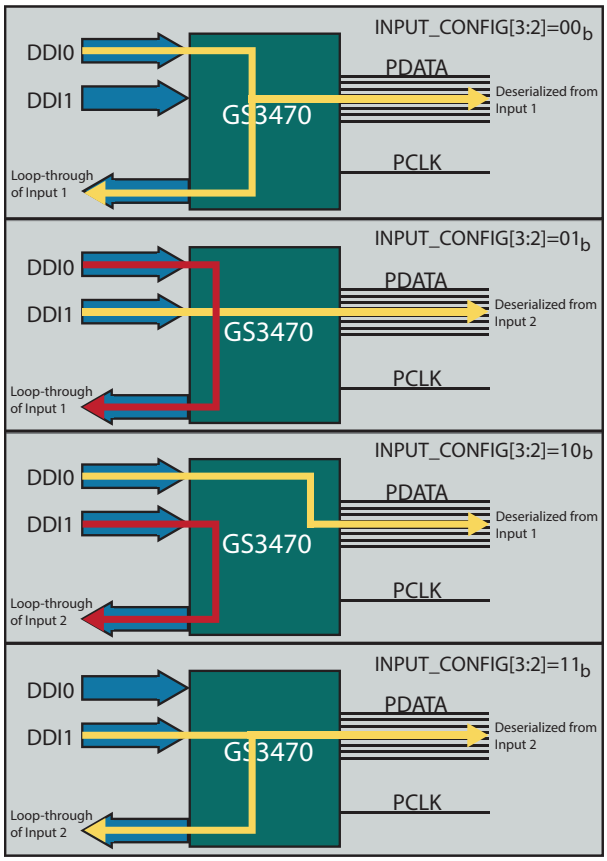


Figure 4-1: Flexible Input Loopback

Expanded and configurable Power-down modes offer increased flexibility by selectively enabling or disabling key features (such as CSR access, PCLK, retimed DDO loop-through output, and non-retimed DDO loop-through output). Figure 4-2 show the various Power-down modes.

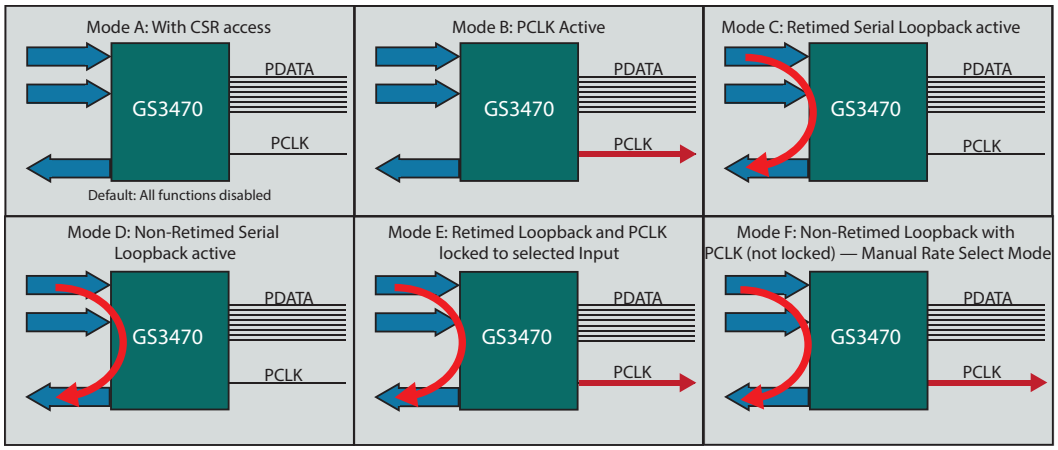


Figure 4-2: Flexible Power Down Modes

The device has three other primary modes of operation which include SMPTE mode, DVB-ASI mode, and Data-Through mode. In SMPTE mode, when receiving a SMPTE compliant SDI input, the GS3470 performs full SMPTE processing, and features a number of data integrity checks and measurement capabilities. The device also supports ancillary data extraction, and can provide entire ancillary data packets through host-accessible registers. Packet detection and error handling features are also offered. All processing features are optional, and may be individually enabled or disabled through register programming. In DVB-ASI mode, sync word detection, alignment, and 8/10bit decoding is applied to the received data stream. While in Data-Through mode, all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

The GS3470 includes an audio de-embedder and audio clocks are internally generated. Up to eight channels (two audio groups) of serial digital audio may be extracted from the video data stream, in accordance with SMPTE ST 272-C and SMPTE ST 299. The output audio formats supported by the device include AES/EBU and I^2S. A variety of audio processing features are provided to ease implementation.

4.2 Device Power-Up

The GS3470 is designed to operate in a multi-voltage environment which allows any power-up sequence to be used. Supply pins can all be powered up in any order.

4.2.1 Power-Down Mode

The *PWR_DWN* pin reduces power to a minimum by disabling various device features. When the *PWR_DWN* pin is de-asserted, the device returns to its previous operating condition within 1 second, without requiring input from the host interface. There are several power-down options which can be configured through GSPI prior to the device going into power-down. Table 4-1 provides a summary of the supported power-down options by accessing the **POWER_DOWN** register.

Table 4-1: Power-down Mode

Power-down Mode	CSR Access	DDO Loop-through Mode	PCLK Mode
Power-down PD_PCLK_ENABLE = 0 SERIAL_LOOPBACK_EN = 0 PD_CSR_ACCESS = 0 RC_BYP = X	No	DDO Disabled	PCLK Disabled
Power-down with CSR Access PD_PCLK_ENABLE = 0 SERIAL_LOOPBACK_EN = 0 PD_CSR_ACCESS = 1 RC_BYP = X	Yes	DDO Disabled	PCLK Disabled
Power-down with PCLK PD_PCLK_ENABLE = 1 SERIAL_LOOPBACK_EN = 0 PD_CSR_ACCESS = X RC_BYP = X	Yes	DDO Disabled	PCLK Enabled
Power-down with DDO PD_PCLK_ENABLE = 0 SERIAL_LOOPBACK_EN = 1 PD_CSR_ACCESS = X RC_BYP = 1	No	DDO Enabled Non-retimed	PCLK Disabled
Power-down with DDO retimed PD_PCLK_ENABLE = 0 SERIAL_LOOPBACK_EN = 1 PD_CSR_ACCESS = X RC_BYP = 0	Yes	DDO Enabled Retimed	PCLK Disabled

Table 4-1: Power-down Mode

Power-down Mode	CSR Access	DDO Loop-through Mode	PCLK Mode
Power-down with DDO/PCLK PD_PCLK_ENABLE = 1 SERIAL_LOOPBACK_EN = 1 PD_CSR_ACCESS = X RC_BYP = 1	Yes	DDO Enabled Non-retimed	PCLK Enabled
Power-down with DDO/PCLK retimed PD_PCLK_ENABLE = 1 SERIAL_LOOPBACK_EN = 1 PD_CSR_ACCESS = X RC_BYP = 0	Yes	DDO Enabled Retimed	PCLK Enabled

Table 4-2: Status Output Support in Power Down Modes

Mode	Rate Detect	Carrier Detect	Lock	All Other Status Outputs
Sleep	N/A	N/A	N/A	N/A
Sleep with DDO not retimed	N/A	N/A	N/A	N/A
Standby with DDO retimed	Available in automatic or manual modes	Analog detect only	Locked status available on STAT outputs	N/A
Standby with PCLK	Available in manual mode only, rate must be set	Analog detect only	N/A	N/A
Standby with PCLK and DDO retimed	Available in automatic or manual modes	Analog detect only	Locked status available on STAT outputs	N/A
Standby with PCLK and DDO not retimed	Available in manual mode only, rate must be set	Analog detect only	N/A	N/A
Standby with CSR access	N/A	Analog detect only	N/A	N/A

4.2.2 Device Reset

Note: On power-up, the device must be reset to operate correctly.

In order to initialize all internal operating conditions to their default states, hold the *RESET* signal LOW for a minimum of t_{reset} = 1ms after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs are driven to a high-impedance state, with the exception of *SDOUT*. *SDOUT* continues normal operation during reset.

GSPI access is restored 10 clock cycles after *RESET* is de-asserted.

All output buffers (including the *PCLK* output), are set to high-impedance in Reset mode (*RESET* = LOW).

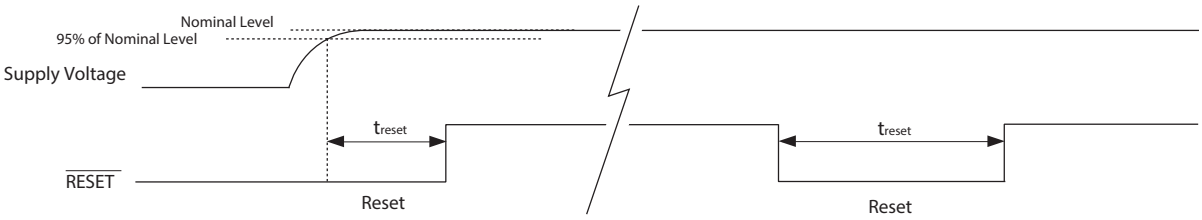


Figure 4-3: Reset Pulse

4.3 Modes of Operation

4.3.1 Auto and Manual Mode

The lock detection algorithm is a continuous process, beginning at device power-up or after a system reset. It continues until the device is powered down or held in reset.

The device first determines if a valid serial digital input signal has been presented to the device. If no valid serial data stream has been detected, the serial data into the device is considered invalid, and the LOCKED signal is LOW.

Once a valid input signal has been detected, the device attempts to detect the presence of either TRS words or DVB-ASI sync words.

By default, the device powers up in Auto mode (the **AUTO_MAN** bit in the host interface is set HIGH). In this mode, the device operating frequency toggles between 3G, HD, and SD rates as it attempts to lock to the incoming data rate. As it searches through rates, PCLK output cycles through 148.5MHz, 74.25MHz, 27MHz, and 13.5MHz. The PCLK output pin can be set to be high-impedance when not locked through GSPI.

When the device is operating in Manual mode (**AUTO_MAN** bit in the host interface register is LOW), the operating frequency needs to be set through the **RATE_SEL_TOP** bits in the host interface. **RATE_SEL_TOP[0]** = **SD/HD** and **RATE_SEL_TOP[1]** = **3G/HD**.

Note: The **SD/HD** bit takes precedence over the **3G/HD** bit, so if the **SD/HD** bit is HIGH, the **3G/HD** bit is ignored.

4.3.2 Low Latency Video Path

The GS3470 has a low latency mode of operation for audio and ancillary data extraction.

Audio can be extracted without incurring any associated delay if the error correction feature and audio packet delete feature are not required. The device will automatically select low latency mode if the **ALL_DEL** CSR bit is set LOW (SD) or **ALL_DEL** CSR bit is set LOW and **ECC_OFF** CSR bit is set HIGH (HD/3G). This means that in low latency mode for audio, ECC errors in the HD/3G audio data packets will not be corrected and no audio packets will be deleted from the data stream after extraction. If either of these features are desired, then a delay will be incurred through the audio extraction blocks. To maintain consistent delay independent of selected features, the **LOW_LATENCY_BYPASS** bit must be set HIGH.

Ancillary data will automatically be extracted without incurring any associated delay if the **ANC_DATA_DEL** CSR bit is set LOW.

4.3.3 SMPTE and SMPTE Bypass Mode

The GS3470 has the ability to run either in SMPTE mode or SMTPE Bypass mode.

In SMPTE mode (**$\overline{\text{SMPTE\_BYPASS}}$** = HIGH), the timing signal generator becomes operational, video signals error detection and SMPTE processing functions are available, and the retimer PLL locks to valid SMPTE video.

In SMPTE Bypass mode (**$\overline{\text{SMPTE\_BYPASS}}$** = LOW), the GS3470 operates either in DVB-ASI mode or Data-Through mode. When operating in SMPTE Bypass mode, none of the SMPTE detection and processing functions are available.

4.3.3.1 Descrambling and Word Alignment

The GS3470 performs NRZI (Non Return to Zero Invert) to NRZ (Non Return to Zero) decoding and data descrambling according to SMPTE ST 424/SMPTE ST 292/SMPTE ST 259-C and word aligns the data to TRS sync words.

When operating in Manual mode (**AUTO_$\overline{\text{MAN}}$** = LOW), the device only carries out SMPTE decoding, descrambling, and word alignment, when the **$\overline{\text{SMPTE_BYPASS}}$** bit is set HIGH and the DVB_ASI bit is set LOW.

When operating in Auto mode (**AUTO_$\overline{\text{MAN}}$** = HIGH), the GS3470 carries out descrambling and word alignment to enable the detection of TRS sync words. When two consecutive valid TRS words (SAV and EAV), with the same bit alignment have been detected, the device word-aligns the data to the TRS ID words.

TRS ID word detection is a continuous process. The device remains in SMPTE mode until TRS ID words fail to be detected.

Note 1: Both 8-bit and 10-bit TRS headers are identified by the device.

Note 2: In 3G Level B mode, the device only supports Data Stream 1 and Data Stream 2 having the same bit width (i.e. both data streams contain 8-bit data, or both data streams contain 10-bit data). If the bit widths between the two data streams are different, the GS3470 cannot word align the input stream. When **$\overline{\text{SMPTE\_BYPASS}}$** is HIGH and the device is set to Auto mode, it will continuously try to lock.