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# GS3590

## Bidirectional 3G-SDI Re-timing Adaptive Cable Equalizer/Cable Driver

## Key Features

- Single bidirectional 75Ω cable interface with on-chip termination
- SMPTE ST 424, ST 292-1 and ST 259 compliant input/output
- Multi-standard operation from 1Mb/s to 2.97Gb/s
- Supports re-timing for DVB-ASI at 270Mb/s and MADI at 125Mb/s
- 3D Input Signal Eye Monitor
- PRBS Generator and Checker
- Automatic cable equalization. Typical equalized cable lengths of Belden 1694A cable:
  - 160m at 2.97Gb/s
  - 240m at 1.485Gb/s
  - 400m at 270Mb/s
- **Cable Equalizer Mode Features:**
  - Manual or automatic power-down on loss of signal
  - Programmable carrier detect with squelch threshold adjustment
  - Manual and automatic Cable Equalizer bypass
- **Cable Driver Mode Features:**
  - Wide swing control
  - Pre-emphasis to compensate for significant insertion loss between device output and BNC
  - Manual or automatic power-down on loss of signal
  - Manual or automatic Mute or Disable on LOS
- **Trace Equalizer Features:**
  - Integrated 100Ω, differential input termination
  - Manual or automatic power-down on loss of signal
  - Adjustable carrier detect threshold
  - DC-coupling from 1.2V to 2.5V CML logic
  - Trace Equalization to compensate for up to 60" FR4 at 2.97Gb/s
  - Automatic input offset compensation
- **Trace Driver Features:**
  - Integrated 100Ω, differential output termination
  - DC-coupling from 1.2V to 2.5V CML logic
  - Trace Driver data output pre-emphasis to compensate for up to 60" FR4 at 2.97Gb/s
  - Manual or automatic Mute or Disable on LOS
- **CDR features:**
  - Manual or automatic rate modes
  - Manual or automatic Re-timer Bypass
  - Wide-range Loop Bandwidth control
  - Re-timing at the following data rates: 125Mb/s, 270Mb/s, 1.485Gb/s, and 2.97Gb/s. This includes the f/1.001 rates.
- **Additional Features:**
  - Single 1.8V power supply for analogue and digital core
  - 2.5V for Cable Driver output supply
  - 1.2V, 1.8V, or 2.5V for Trace Driver output supply
  - GSPI serial control and monitoring interface
  - Four configurable GPIO pins for control or status monitoring
  - Wide operating temperature range: -40°C to +85°C
  - Small 6mm x 4mm 40-pin QFN
  - Pb-free/Halogen-free/RoHS & WEEE compliant package
  - Pin compatible with the GS12090

## Applications

SMPTE ST 424, SMPTE ST 292, SMPTE ST 259 interfaces requiring switching between cable equalizing or cable driving functionality. Typical applications: Cameras, Switchers, Distribution Amplifiers and Routers.

## Description

The GS3590 is a low-power, configurable multi-rate re-timing Cable Equalizer/Cable Driver supporting rates up to 3G-SDI. It can be configured to equalize or drive signals over 75Ω coaxial cable. It includes DC restoration to compensate for the DC content of SMPTE pathological test patterns. Since the GS3590 is a re-timing device, extremely low output jitter is achievable even at extended cable/trace lengths.

The integrated Eye Monitor provides non-disruptive mission mode analysis of the post-equalized input signal. The 256x128 resolution scan matrix allows accurate signal analysis to speed-up prototyping and enable field analysis.

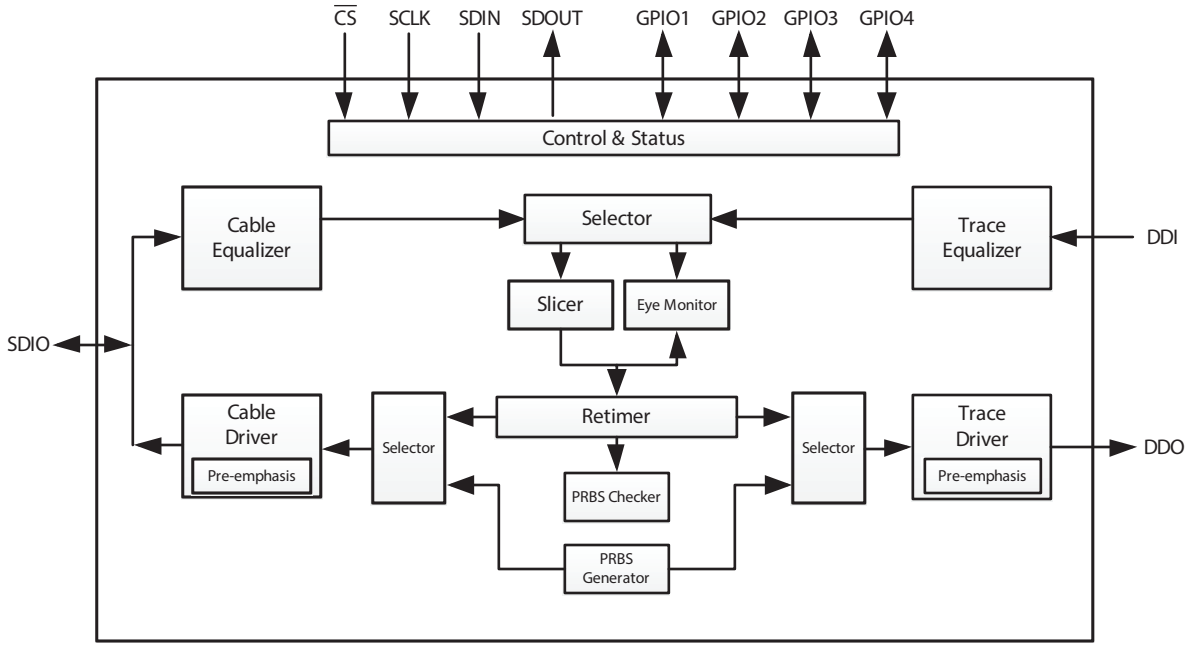
Built-in macros enable customizable cross section analysis and quick horizontal and vertical eye opening measurements.

With high phase consistency between scans and configurable space and time thresholds, algorithms can be deployed in the field to analyse long-term signal quality variation (Bathtub Plot) to reduce costly system installation debug time for intermittent errors.

Each output has highly configurable pre-emphasis and swing controls to compensate for long trace and connector losses.

Additionally, automatic and user selectable output slew rate control is provided for the Cable Equalizer output.

The GS3590 is pin compatible with the GS12090 Bidirectional 12G-SDI Re-timing Adaptive Cable Equalizer/Cable Driver.




**GS3590 Functional Block Diagram**

## Revision History

| Version | ECO | PCN | Date | Changes and/or Modifications |
|---|---|---|---|---|
| 4 | 038524 | — | September 2017 | Updated values in Table 2-2 and Table 2-3. |
| 3 | 037845 | — | July 2017 | Added Section 4.8.4. |
| 2 | 037327 | — | June 2017 | Updated Section 4.10.13, and added Section 4.10.12. |
| 1 | 034374 | — | December 2016 | Updates as described in the GS3590 Errata (PDS-061458, ECO-034375). |
| 0 | 033713 | — | October 2016 | New Document. |

## Contents

# 1. Pin Out

## 1.1 GS3590 Pin Assignment

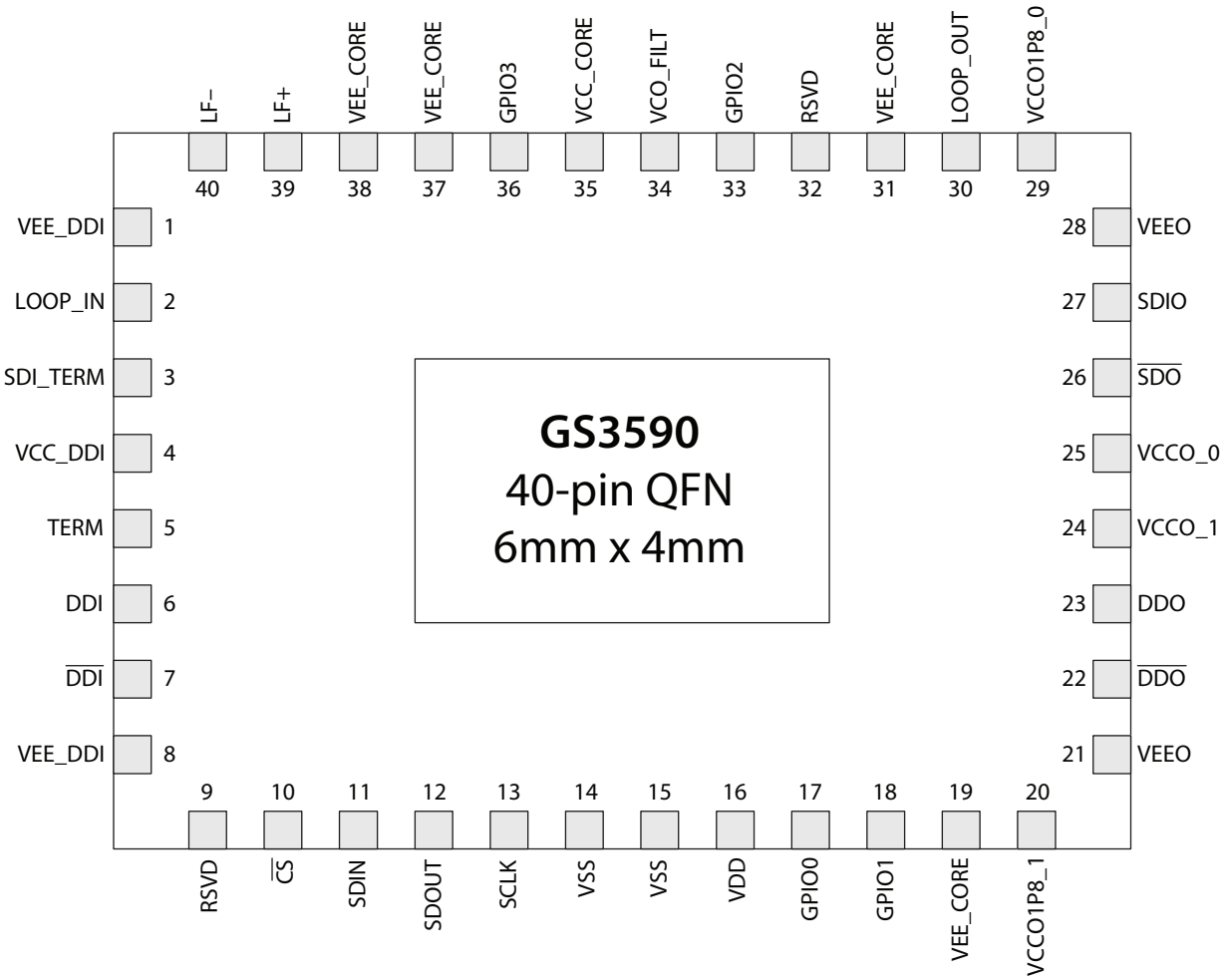



**Figure 1-1: GS3590 Pin Assignment**

# 1.2 GS3590 Pin Descriptions

### Table 1-1: GS3590 Pin Descriptions

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 1, 8 | VEE_DDI | Power | Most negative power supply connection for the Cable Equalizer and Trace Equalizer.<br>Connect to ground. |
| 2 | LOOP_IN | Input | Single-ended CML input with internal 75Ω termination. Connect to LOOP_OUT (pin 30) through a capacitor (see Section 6.1 Typical Application Circuit for recommended values). |
| 3 | SDI_TERM | — | Input Common Mode termination. Decouple to ground (see Section 6.1 Typical Application Circuit for recommended values). |
| 4 | VCC_DDI | Power | Most positive power supply connection for the Trace and Cable Equalizer.<br>Connect to 1.8V. |
| 5 | TERM | — | Input Common Mode termination. Decouple to ground (see Section 6.1 Typical Application Circuit for recommended values). |
| 6, 7 | DDI, $\overline{\text{DDI}}$ | Input | Serial digital differential input. Differential CML input with internal 100Ω termination. |
| 9, 32 | RSVD | — | These pins may be left floating. Please contact your Semtech FAE for additional information on circuit compatibility with the GS3590. |
| 10 | $\overline{\text{CS}}$ | Digital Input | Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port.<br>1.8V CMOS input with 100kΩ pull-up.<br>Active-low input.<br>Refer to Section 4.10.1 for more details. |
| 11 | SDIN | Digital Input | Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port.<br>1.8V CMOS input with 100kΩ pull-down.<br>Refer to Section 4.10.2 for more details. |
| 12 | SDOUT | Digital Output | Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port.<br>1.8V CMOS output.<br>Refer to Section 4.10.3 for more details. |
| 13 | SCLK | Digital Input | Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port.<br>1.8V CMOS input with 100kΩ pull-down.<br>Refer to Section 4.10.4 for more details. |
| 14, 15 | VSS | Power | Most negative power supply for digital core logic.<br>Connect to ground. |
| 16 | VDD | Power | Most positive power supply connection for digital core logic.<br>Connect to 1.8V. |

## Table 1-1: GS3590 Pin Descriptions (Continued)

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 17 | GPIO0 | Digital Input/Output | Multi-function Control/Status Input/Output 0.<br>Default function:<br>Direction = Output<br>Signal = High indicates LOS (Loss of Signal, inverse of Carrier Detect)<br>Pin is 1.8V CMOS I/O, please refer to GPIO0_CFG for more information on how to configure GPIO0. |
| 18 | GPIO1 | Digital Input/Output | Multi-function Control/Status Input/Output 1.<br>Default function:<br>Direction = Output<br>Signal = High indicates PLL is locked<br>Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1. |
| 19, 31, 37, 38 | VEE_CORE | Power | Most negative power supply connection for the analogue core.<br>Connect to ground. |
| 20 | VCCO1P8_1 | Power | Most positive power supply connection for Trace Driver pre-driver.<br>Connect to 1.8V. |
| 21, 28 | VEEO | Power | Most negative power supply connection for the output drivers.<br>Connect to ground. |
| 22, 23 | $\overline{\text{DDO}}$, DDO | Output | Differential CML output with two internal 50Ω pull-ups.<br>In cable equalizer mode, the data signal or PRBS Generator can be selected for this output. |
| 24 | VCCO_1 | Power | Most positive power supply connection for the DDO/ $\overline{\text{DDO}}$ output driver.<br>Connect to 1.2V – 2.5V. |
| 25 | VCCO_0 | Power | Most positive power supply connection for the SDIO/$\overline{\text{SDO}}$ output driver.<br>Connect to 2.5V. |
| 26 | $\overline{\text{SDO}}$ | Output | Single-ended CML output buffer with internal 75Ω pull-up. Decouple to ground (see Section 6.1 Typical Application Circuit for recommended values). |
| 27 | SDIO | Output | Single-ended bidirectional CML buffer with internal 75Ω pull-up.<br>In cable driver mode, the data signal or PRBS Generator can be selected for this output. |
| 29 | VCCO1P8_0 | Power | Most positive power supply connection for Cable Driver pre-driver.<br>Connect to 1.8V. |
| 30 | LOOP_OUT | Output | Single-ended CML output. Connect to LOOP_IN (pin 2) through a capacitor (see Section 6.1 Typical Application Circuit for recommended values). |

## Table 1-1: GS3590 Pin Descriptions (Continued)

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 33 | GPIO2 | Digital Input/Output | Multi-function Control/Status Input/Output 2.<br>Default function:<br>Direction = Input<br>Signal = Set HIGH to put device in sleep<br>Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2. |
| 34 | VCO_FILT | Passive | VCO filter capacitor connection. Decouple to ground. See Section 6.1 Typical Application Circuit for recommended values. |
| 35 | VCC_CORE | Power | Most positive power supply connection for the analogue core.<br>Connect to 1.8V. |
| 36 | GPIO3 | Digital Input/Output | Multi-function Control/Status Input/Output 3.<br>Default function:<br>Direction = Input<br>Signal = Set HIGH to put device in cable driver mode<br>Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3. |
| 39 | LF+ | Passive | Loop filter capacitor connection. Connect to pin 40 through a capacitor (see Section 6.1 Typical Application Circuit for recommended values). |
| 40 | LF- | Passive | Loop filter capacitor connection. Connect to pin 39 through a capacitor (see Section 6.1 Typical Application Circuit for recommended values). |
| Tab | — | — | Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation. It is not recommended to connect the device ground pins to the central paddle. |

# 2. Electrical Characteristics

## 2.1 Absolute Maximum Ratings

### Table 2-1: Absolute Maximum Ratings

| Parameter | | Value |
|---|---|---|
| Supply Voltage—Core ($V_{CC\_DDI}$, $V_{CC\_CORE}$, $V_{DD}$) | | -0.5V to +2.2V |
| Supply Voltage—Output Driver | $V_{CCO\_0}$ | -0.5V to +2.8V |
| | $V_{CCO\_1}$ | -0.5V to +2.8V |
| Input ESD Voltage (any pin) | | 3kV HBM |
| Storage Temperature Range ($T_S$) | | -50°C to +125°C |
| Input Voltage Range (SDIO) | | -0.3 to ($V_{CCO\_0}$ + 0.3)V |
| Input Voltage Range (GPIO2, GPIO3) | | -0.3 to ($V_{CC\_CORE}$ + 0.3)V |
| Input Voltage Range ($\overline{CS}$, SDIN, SCLK, VSS, VDD, GPIO0, GPIO1) | | -0.3 to ($V_{DD}$ +0.3)V |
| Solder Reflow Temperature | | 260°C |

**Note:** Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

# 2.2 DC Electrical Characteristics

## Table 2-2: DC Electrical Characteristics

$T_A$ = -40°C to +85°C, unless otherwise shown.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Bi-Directional Characteristics (Applicable to Both Modes) | | | | | | | |
| Supply Voltage | $V_{CC\_DDI}$, $V_{CC\_CORE}$, $V_{DD}$ | — | 1.71 | 1.8 | 1.89 | V | — |
| DDI Input and DDO Output Termination | | Differential | — | 100 | — | Ω | — |
| SDIO Bi-directional Termination | | Between SDIO and GND | — | 75 | — | Ω | — |
| $\overline{SDO}$ Output Termination | | Between $\overline{SDO}$ and GND | — | 75 | — | Ω | — |
| Supply Current—Analogue Core | $I_{CC\_CORE}$ | CDR Unlocked During Rate Search | — | 182 | — | mA | — |
| | | PRBS Generator Enabled | — | 119 | — | mA | 2, 3 |
| | | PRBS Checker Enabled | — | 60 | — | mA | 2 |
| | | Eye Monitor Enabled | — | 54 | — | mA | 2 |
| Supply Current—Digital Logic | $I_{DD}$ | — | — | 16 | 20 | mA | — |
| Input Voltage—Digital Pins ($\overline{CS}$, SDIN, SCLK, GPIO[0:3]) | $V_{IH}$ | — | 0.65* $V_{DD}$ | — | $V_{DD}$ | V | — |
| | $V_{IL}$ | — | 0 | — | 0.35* $V_{DD}$ | V | — |
| Output Voltage—Digital Pins (SDOUT, GPIO[0:3]) | $V_{OH}$ | $I_{OH}$ = -5mA | VDD - 0.45 | — | — | V | — |
| | $V_{OL}$ | $I_{OL}$ = +5mA | — | — | 0.45 | V | — |
| Cable Equalizer Mode Characteristics | | | | | | | |
| Supply Voltage—Trace Driver | $V_{CCO\_1}$ | | 1.14 | 1.2 | 1.26 | V | — |
| | | | 1.71 | 1.8 | 1.89 | V | — |
| | | | 2.38 | 2.5 | 2.63 | V | — |

## Table 2-2: DC Electrical Characteristics (Continued)

$T_A$ = -40°C to +85°C, unless otherwise shown.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Power | $P_D$ | $V_{CCO\_1}$ = 1.2V, Output Swing = 400mV$_{ppd}$, DDO/$\overline{DDO}$ enabled | — | 430 | — | mW | 1 |
| | | $V_{CCO\_1}$ = 1.8V, Output Swing = 400mV$_{ppd}$, DDO/$\overline{DDO}$ enabled | — | 440 | — | mW | 1 |
| | | $V_{CCO\_1}$ = 1.8V, Output Swing = 800mV$_{ppd}$, DDO/$\overline{DDO}$ enabled | — | 455 | — | mW | 1 |
| | | $V_{CCO\_1}$ = 2.5V, Output Swing = 400mV$_{ppd}$, DDO/$\overline{DDO}$ enabled | — | 445 | — | mW | 1 |
| | | $V_{CCO\_1}$ = 2.5V, Output Swing = 800mV$_{ppd}$, DDO/$\overline{DDO}$ enabled | — | 470 | — | mW | 1 |
| Supply Current—Trace Driver | $I_{CCO\_1}$ | $V_{CCO\_1}$ = 1.2V, Output Swing = 400mV$_{ppd}$ | — | 10 | 17 | mA | 1 |
| | | $V_{CCO\_1}$ = 1.8V, Output Swing = 400mV$_{ppd}$ | — | 10 | 17 | mA | 1 |
| | | $V_{CCO\_1}$ = 1.8V, Output Swing = 800mV$_{ppd}$ | — | 20 | 30 | mA | 1 |
| | | $V_{CCO\_1}$ = 2.5V, Output Swing = 400mV$_{ppd}$ | — | 10 | 17 | mA | 1 |
| | | $V_{CCO\_1}$ = 2.5V, Output Swing = 800mV$_{ppd}$ | — | 20 | 30 | mA | 1 |
| Supply Current — Trace Driver Pre Driver | $I_{CCO\_1P8\_1}$ | Output Swing = 800mV$_{pp}$ | — | 25 | 32 | mA | — |
| Supply Current — $V_{CCO\_0}$ | $I_{CCO\_0}$ | $V_{CCO\_0}$ = 2.5V, Output Swing = 800mV$_{ppd}$ | — | 13 | 18 | mA | — |
| Supply Current— Cable Equalizer | $I_{CC\_SDI}$ | — | — | 55 | 75 | mA | — |
| Supply Current— Analogue Core | $I_{CC\_CORE}$ | CDR Locked to Rate | — | 125 | 161 | mA | — |
| DDO Output Common Mode Voltage | $V_{CMOUT}$ | — | — | $V_{CMOUT}$ = $V_{CCO\_1}$ - $\Delta V_{DDO}/2$ | — | V | — |

## Table 2-2: DC Electrical Characteristics (Continued)

$T_A$ = -40°C to +85°C, unless otherwise shown.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Cable Driver Mode Characteristics** | | | | | | | |
| Supply Voltage — Cable Driver | $V_{CCO\_0}$ | — | 2.38 | 2.5 | 2.63 | V | — |
| Power | $P_D$ | $V_{CCO\_0}$ = 2.5V, Output Swing = 800mV$_{pp}$, DDO/$\overline{DDO}$ disabled | — | 375 | — | mW | 1 |
| | | $V_{CCO\_0}$ = 2.5V, Output Swing = 800mV$_{pp}$ with max pre-emphasis, DDO/$\overline{DDO}$ disabled | — | 390 | — | mW | — |
| Supply Current— Cable Driver | $I_{CCO\_0}$ | $V_{CCO\_0}$ = 2.5V, Output Swing = 800mV$_{pp}$ | — | 25 | 36 | mA | 1 |
| | | $V_{CCO\_0}$ = 2.5V, Output Swing = 800mV$_{pp}$, with max pre-emphasis | — | 30 | 38 | mA | — |
| Supply Current — Cable Driver Pre Driver | $I_{CCO1P8\_0}$ | Output Swing = 800mV$_{pp}$ | — | 20 | 30 | mA | — |
| Supply Current— Analogue Core | $I_{CC\_CORE}$ | CDR Locked to Rate | — | 120 | 164 | mA | — |
| Supply Current — Trace Equalizer | $I_{CC\_DDI}$ | — | — | 20 | 32 | mA | — |
| DDI Input Common Mode Voltage | $V_{CMIN}$ | — | 0.94 | $V_{CC\_DDI}$ - 0.1V | 2.525 | V | 4 |
| **Sleep Mode** | | | | | | | |
| Sleep | | Cable Equalizer mode | — | 80 | — | mW | — |
| Sleep | | Cable Driver mode | — | 45 | — | mW | — |

**Notes:**

1. Pre-emphasis is disabled.
2. Current listed is an increase to $I_{CC\_CORE}$ when stated condition is true.
3. Selected clock source = VCO free running.
4. When the Trace Equalizer is AC-coupled, the input common mode is $V_{CC\_DDI}$ – 0.1V. 0.94V is the worst case when the Trace Equalizer is DC-coupled to upstream driver running from 1.2V supply. 2.525V is the worst case when the Trace Equalizer is DC-coupled to upstream driver running from 2.5V supply.

# 2.3 AC Electrical Characteristics

### Table 2-3: AC Electrical Characteristics

$V_{CC\_DDI}$, $V_{CC\_CORE}$, $V_{DD}$ = +1.8V ±5% and $V_{CCO\_0}$, $V_{CCO\_1}$ = +2.5V ±5%, $T_A$ = -40°C to +85°C, unless otherwise shown.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Bi-Directional Characteristics (Applicable to Both Modes) | | | | | | | |
| Serial Input Data Rate | $DR_{DDI}$, $DR_{SDIO}$ | — | 0.001 | — | 2.97 | Gb/s | 12 |
| Return Loss | | 5MHz to 1.485GHz | — | — | -17 | dB | 1 |
| | | 1.485GHz to 2.97GHz | — | — | -12 | dB | 1 |
| PLL Loop Bandwidth (for 0.2UI jitter and 50% edge density) | $BW_{LOOP(125Mb/s)}$ | Setting 0.0625x | — | 5 | — | kHz | 5 |
| | | Setting 0.125x | — | 10 | — | kHz | 5 |
| | | Setting 0.25x | — | 19 | — | kHz | 5 |
| | | Setting 0.5x (Default) | — | 38 | — | kHz | 5 |
| | | Setting 1.0x | — | 75 | — | kHz | 5 |
| | $BW_{LOOP(270Mb/s)}$ | Setting 0.0625x | — | 10 | — | kHz | 5 |
| | | Setting 0.125x | — | 20 | — | kHz | 5 |
| | | Setting 0.25x | — | 40 | — | kHz | 5 |
| | | Setting 0.5x | — | 80 | — | kHz | 5 |
| | | Setting 1.0x (Default) | — | 158 | — | kHz | 5 |
| | $BW_{LOOP(1.485Gb/s)}$ | Setting 0.0625x | — | 55 | — | kHz | 5 |
| | | Setting 0.125x | — | 110 | — | kHz | 5 |
| | | Setting 0.25x | — | 220 | — | kHz | 5 |
| | | Setting 0.5x (Default) | — | 438 | — | kHz | 5 |
| | | Setting 1.0x | — | 875 | — | kHz | 5 |
| | $BW_{LOOP(2.97Gb/s)}$ | Setting 0.0625x | — | 110 | — | kHz | 5 |
| | | Setting 0.125x | — | 220 | — | kHz | 5 |
| | | Setting 0.25x | — | 440 | — | kHz | 5 |
| | | Setting 0.5x (Default) | — | 0.88 | — | MHz | 5 |
| | | Setting 1.0x | — | 1.75 | — | MHz | 5 |
| Cable Equalizer Mode Characteristics | | | | | | | |
| BNC Input Voltage Swing | $V_{SDIO}$ | — | 720 | 800 | 880 | $mV_{pp}$ | 3 |
| Differential Output Voltage Swing | $\Delta V_{DDO}$ | 200mV | 150 | 200 | 250 | $mV_{ppd}$ | 7 |
| | | 800mV | 600 | 800 | 1000 | $mV_{ppd}$ | 8 |
| DDO, $\overline{DDO}$, Rise/Fall Time | $t_{riseDDO}$, $t_{fallDDO}$ | All rates | — | — | 40 | ps | 11 |
| DDO Mismatch in Rise/Fall Time | | — | — | — | 8 | ps | 11 |
| DDO Duty Cycle Distortion DDO, $\overline{DDO}$ | | — | — | — | 10 | ps | — |
| PLL Lock Time— Asynchronous | $t_{ALOCK}$ | — | — | 75 | — | ms | 6 |

## Table 2-3: AC Electrical Characteristics (Continued)

$V_{CC\_DDI}$, $V_{CC\_CORE}$, $V_{DD}$ = +1.8V ±5% and $V_{CCO\_0}$, $V_{CCO\_1}$ = +2.5V ±5%, $T_A$ = -40°C to +85°C, unless otherwise shown.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Serial Data Output Jitter (DDO) | $t_{OJ(125Mb/s)}$ | Belden 1694A: 400m | — | 0.02 | 0.1 | UI | 2 |
| | $t_{OJ(270Mb/s)}$ | Belden 1694A: 400m | — | 0.02 | 0.1 | UI | 2 |
| | $t_{OJ(1.485Gb/s)}$ | Belden 1694A: 240m | — | 0.02 | 0.1 | UI | 2 |
| | $t_{OJ(2.97Gb/s)}$ | Belden 1694A: 160m | — | 0.04 | 0.1 | UI | 2 |
| Cable Driver Mode Characteristics | | | | | | | |
| Differential Input Voltage Swing | $\Delta V_{DDI}$ | — | 200 | — | 800 | $mV_{ppd}$ | — |
| BNC Output Voltage Swing | $V_{SDIO}$, $V_{\overline{SDO}}$ | — | 720 | 800 | 880 | $mV_{pp}$ | 4 |
| Input Trace Equalization | | 3G | — | 60 | — | Inches | 13dB, 9 |
| | | HD | — | 60 | — | Inches | 6dB, 9 |
| | | SD | — | 60 | — | Inches | 3dB, 9 |
| | | MADI | — | 60 | — | Inches | 3dB, 9 |
| Intrinsic Input Jitter Tolerance | IIJT | MADI/SD/HD/3G | 0.8 | 0.95 | — | UI | — |
| PLL Lock Time—Asynchronous | $t_{ALOCK}$ | Referenceless with MADI rate detection disabled | — | — | 16.7 | ms | 6 |
| | | Referenceless with MADI rate detection enabled | — | — | 32 | ms | 6 |
| PLL Lock Time—Synchronous | $t_{SLOCK}$ | SD | — | — | 10 | µs | 6 |
| | | HD/3G | — | — | 5 | µs | 6 |
| SDIO, $\overline{SDO}$ Rise/Fall Time | $t_{riseSDIO}$, $t_{fallSDIO}$ | SD/MADI | 400 | — | 1000 | ps | — |
| | | HD/3G | — | — | 70 | ps | — |
| | | Bypass | — | — | 40 | ps | — |
| SDIO Mismatch in Rise/Fall Time | | SD/MADI | — | — | 100 | ps | — |
| | | HD/3G | — | — | 20 | ps | — |
| SDIO Eye Cross Shift (SDIO, $\overline{SDO}$) | | SD/MADI | — | — | 5 | % | — |
| | | HD/3G | — | — | 8 | % | — |
| SDIO Overshoot | | — | — | — | 10 | % | — |

## Table 2-3: AC Electrical Characteristics (Continued)

$V_{CC\_DDI}$, $V_{CC\_CORE}$, $V_{DD}$ = +1.8V ±5% and $V_{CCO\_0}$, $V_{CCO\_1}$ = +2.5V ±5%, $T_A$ = -40°C to +85°C, unless otherwise shown.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Serial Data Output Jitter (SDIO) | $t_{OJ(125Mb/s)}$ | BW = default, Pattern = PRBS | — | 0.015 | 0.08 | UI | 2, 10 |
| | $t_{OJ(270Mb/s)}$ | | — | 0.035 | 0.08 | UI | 2, 10 |
| | $t_{OJ(1.485Gb/s)}$ | | — | 0.025 | 0.08 | UI | 2, 10 |
| | $t_{OJ(2.97Gb/s)}$ | | — | 0.04 | 0.08 | UI | 2, 10 |
| | $t_{OJ(Bypass)}$ | | — | 0.1 | 0.2 | UI | 2, 10 |

**Notes:**

1. Values achieved with Semtech evaluation board and connector.
2. Measured using a clean input source.
3. Default value for CFG_EQ_INPUT_LAUNCH_SWING_COMP parameter in control register 0x18. The default parameter value is $80_d$ ($50_h$).
4. Default Cable Driver swing Setting.
5. Please see PLL_LOOP_ BANDWIDTH_ 1 for the full range of loop bandwidth settings.
6. Please see Section 4.4.3.1 for the further definition on Synchronous and Asynchronous Lock Time.
7. Output driver setting of 8.
8. Output driver setting of 36.
9. Trace insertion loss was measured with FR4 material using 7 mil strip-line traces using a PRBS23 signal.
10. Measured under minimal trace loss conditions.
11. Rise/fall time was measured between 80% and 20%.
12. When in Cable Equalizer Mode, the rise/fall time of signals at the source should not be more than 62ns.

**Note:** For GSPI Timing see Table 4-12: GSPI Timing Parameters.

# 3. Input/Output Circuits

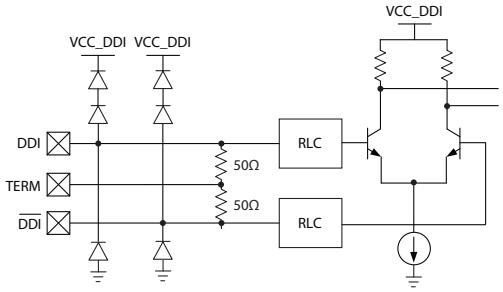



**Figure 3-1: DDI, $\overline{\text{DDI}}$**

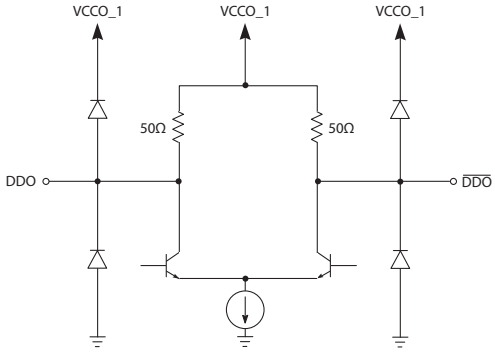



**Figure 3-2: DDO/$\overline{\text{DDO}}$**

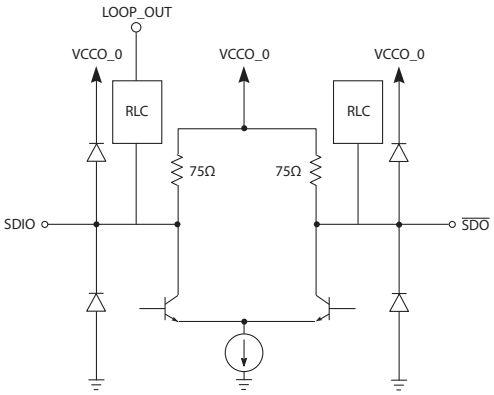



**Figure 3-3: SDIO, $\overline{\text{SDO}}$**

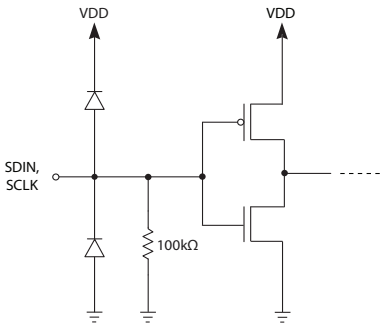



**Figure 3-4: SDIN, SCLK**

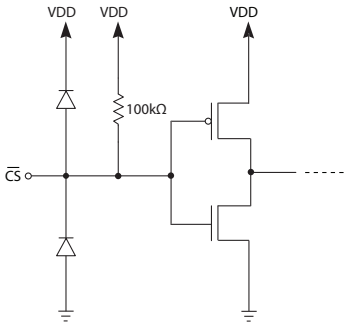



**Figure 3-5: Chip Select ($\overline{CS}$)**

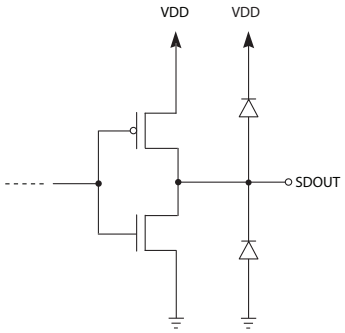



**Figure 3-6: SDOUT**

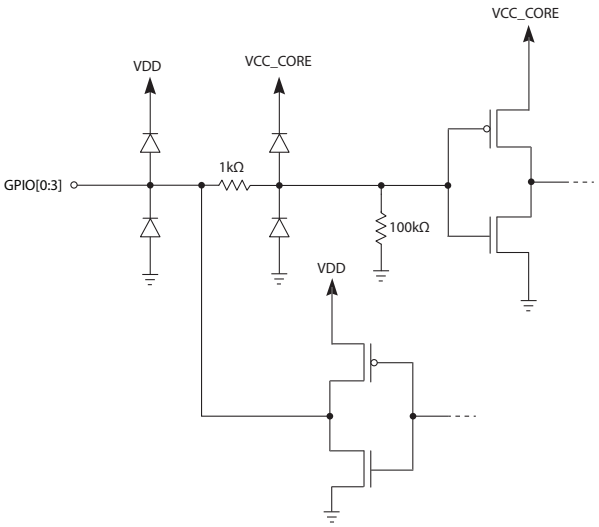



**Figure 3-7: GPIO[0:3]**

# 4. Detailed Description

## 4.1 Device Description

The GS3590 features a 75Ω internally-terminated bidirectional SDIO port, which can be set as SMPTE-compliant Cable Driver, or Cable Equalizer. In addition to the SDIO port, there is a 100Ω differential Trace Driver to transmit the incoming SDI signal to the system and a 100Ω differential Trace Equalizer to receive the outgoing signal from the system. The bidirectional mode can be controlled through the host interface, or the *GPIO* pin. The Cable Driver has amplitude and pre-emphasis control to compensate for significant insertion loss between device output and BNC. The Trace Driver also has amplitude and pre-emphasis control which can compensate for 15dB of insertion loss at 1.485GHz. The pre-emphasis control is two-dimensional in both the Cable Driver and Trace Driver, where both pre-emphasis pulse amplitude and width adjustments can be made to help optimize for interconnect mismatches such as vias and connectors. The Trace Equalizer has boost control, which can compensate for 17dB of insertion loss at 1.485GHz.

### 4.1.1 Bidirectional Mode Control

The bidirectional mode of the GS3590 can be controlled through the GPIO or the host interface.

By default the device is in pin control mode and *GPIO3* is the control input pin. To put the device in Cable Equalizer Mode drive this pin LOW. To put the device in Cable Driver Mode drive this pin HIGH.

In addition to GPIO control, the host can set the direction mode through the host interface using the **CTRL_DIRECTION_SEL_MODE** and **CTRL_DIRECTION_SEL** parameters in register 0x14. To use the host interface to control the direction mode, first choose host interface select mode by writing $1_b$ to **CTRL_DIRECTION_SEL_MODE** (default = $0_b$ pin mode). Once the device is in host interface select mode, the host can put the device in cable equalizer mode by writing $0_b$ to the **CTRL_DIRECTION_SEL** control parameter (default = $1_b$ cable driver mode).

### 4.1.2 Sleep Mode

To enable low-power operation, the GS3590 has Manual and Automatic Sleep Mode control.

The default mode is Automatic Sleep Mode on LOS (Loss Of Signal). The device can also be manually put into Sleep Mode. When the device is in Sleep Mode, all the core blocks are powered-down, except the host interface and carrier detect circuits. The SDIO Cable Driver output buffer is always disabled (powered-down) in sleep mode, while the DDO Trace Driver can be disabled or muted.

The **CTRL_AUTO_SLEEP** and **CTRL_MANUAL_SLEEP** parameters in register 0x3, control the sleep mode of the device. The default value of the **CTRL_AUTO_SLEEP** parameter is $1_b$ (Auto Sleep). While in Auto Sleep Mode, the **CTRL_MANUAL_SLEEP** parameter has no effect. To enable host control of the sleep mode, set the **CTRL_AUTO_SLEEP** parameter to $0_b$ for Manual Sleep Control. To prevent the device from entering sleep, set the **CTRL_MANUAL_SLEEP** parameter to $0_b$ (not sleep). To manually configure the device to sleep, set the **CTRL_MANUAL_SLEEP** parameter to $1_b$ (sleep).

The device can also be manually made to sleep through the *GPIO* pins. The default *GPIO* pin to control sleep is *GPIO2* (pin 33). Drive this pin HIGH to make the device sleep.

Section 4.7 describes the PRBS Generator function. If the device's PRBS Generator is intended to be used without a valid input signal, the device should be manually set to not sleep as described above. Without a valid input signal, an LOS status will be generated and the device will enter sleep mode and the PRBS block will be disabled. For a description of LOS thresholds and settings, see Section 4.2.3 and Section 4.3.2.

# 4.2 Cable Equalizer

When the GS3590 is operating in Cable Equalizer Mode, it can automatically adjust its gain to equalize and restore SMPTE-compliant signals received over different lengths of coaxial cable having loss characteristics similar to Belden 8281 or 1694A. With the default settings, the device will automatically equalize MADI at 125Mb/s and most common SMPTE compliant signals between SD at 270Mb/s and 3G-SDI at 2.97Gb/s and bypass signals below 125Mb/s.

The GS3590 features programmable Launch Swing Compensation, Squelch Threshold Adjust, and Bypass, all of which can be set through the device's host interface.

The equalized or bypassed signal is then routed to the serial digital re-timer (CDR) block.

## 4.2.1 Cable Equalizer Bypass

With the default settings, the device will automatically bypass signals below 125Mb/s. During Equalizer Bypass Mode, the device supports low data rate and slow edge signals such as SMPTE310 and AES3id. The rise/fall times must not exceed 62ns. These signals will not be re-timed by the CDR block. The following two methods allow the user to force the signal to bypass the equalization and DC restoration stages:

1. Via the host interface, by setting **CTRL_CEQ_AUTO_BYPASS** to $0_b$, and **CTRL_CEQ_MANUAL_BYPASS** to $1_b$ in register 0x17.

2. Via the *GPIO[0:3]* pin (see Section 4.9).

## 4.2.2 Upstream Launch Swing Compensation

The GS3590 Cable Equalizer has an automatic gain control circuit, that is optimized on the assumption that the Cable Driver in the upstream device is SMPTE-compliant and has a launch swing of $800mV_{pp}$ ±10%. When the source amplitude is known to be non-SMPTE compliant, a compensation adjustment can be made in the GS3590. The GS3590 can adjust for launch swings in the range of 250mV to 1V in approximately $50mV_{ppd}$ increments. Upstream launch swing compensation can be adjusted through the **CFG_EQ_INPUT_LAUNCH_SWING_COMP** parameter in control register 0x18. The default parameter value is $80_d$ ($50_h$), which corresponds to a nominal launch swing of $800mV_{ppd}$.

## 4.2.3 Carrier Detect, Squelch Control, and Loss of Signal

The GS3590 Cable Equalizer has highly-configurable carrier detection and squelching capability. The carrier detection can be made more robust against spurious signals and noise at the inputs and the squelch control can be configured and enabled to reduce false outputs to low level signals such as crosstalk.

The GS3590 reports two separate carrier detect parameters—**STAT_PRI_CD** and **STAT_SEC_CD**. They are described in Section 4.2.3.1 and Section 4.2.3.2 respectively.

**Note:** The parameters referred to within Section 4.2.3 to Section 4.2.3.2 are linked to their respective registers in Table 4-1.

### 4.2.3.1 Primary Carrier Detection (STAT_PRI_CD) Configuration

Primary carrier detection (**STAT_PRI_CD**) can be configured for higher stability by filtering-out longer transients or glitches. This can be achieved by increasing the sampling window over which the signal is sampled and the number of samples required to assert or de-assert it.

There are three configuration parameters that control assertion or de-assertion of **STAT_PRI_CD**:

- **CFG_CD_FILTER_SAMPLE_WIN**
- **CFG_FILTER_DEASSERT_CNT**
- **CFG_CD_FILTER_ASSERT_CNT**

See Figure 4-1 for a visual representation of the **STAT_PRI_CD** configuration parameters.

With the default values in place:

- An assertion (setting HIGH) of **STAT_PRI_CD** will take place after a valid signal is present for ~6.5ms
- A de-assertion (setting LOW) of **STAT_PRI_CD** will take place after loss of a valid signal for ~96ms

If the application requires any adjustment of the sampling window, assertion count, or de-assertion count, please consult the following equations to calculate the associated time to assert or de-assert **STAT_PRI_CD**.

**STAT_PRI_CD** de-assert time:

- ***(1.6µs) * (CFG_CD_FILTER_SAMPLE_WIN + 1) * CFG_CD_FILTER_DEASSERT_CNT***

**STAT_PRI_CD** assert time:

- ***(1.6µs) * (CFG_CD_FILTER_SAMPLE_WIN + 1) * CFG_CD_FILTER_ASSERT_CNT***

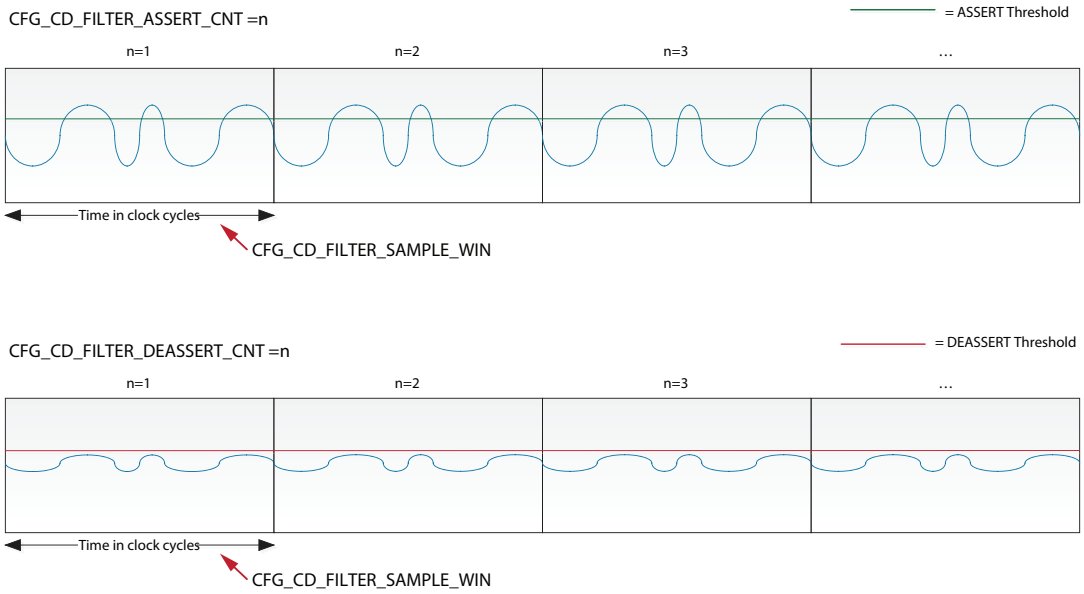



**Figure 4-1: STAT_PRI_CD Configuration Parameters**

### 4.2.3.2 Secondary Carrier Detection (STAT_SEC_CD) Configuration

The secondary carrier detection signal acts as an additional carrier detection which can be further filtered through squelch controls. It also serves as the control signal for Mute on LOS (Loss Of Signal) and Disable on LOS. Please refer to Section 4.8.7 to Section 4.8.7.3 for further information on this.

If the application requires the use of squelch settings, start by setting the following:

- **CFG_SEC_CD_INCL_CLI_SQUELCH** = 1

Once this parameter is set, the device will apply squelch based on the settings found within the following parameters:

- **CFG_CLI_SQUELCH_THRESHOLD**
- **CFG_CLI_SQUELCH_HYSTERESIS**

The device will use these parameters to determine squelch status and set that within **STAT_CLI_SQUELCH**. Based off of this, secondary carrier detection can be described as:

- **STAT_SEC_CD** = inverse of (**STAT_CLI_SQUELCH** & **STAT_PRI_CD**).

To help detail how the device determines the state of Squelch, we define the following variables:

- CLI = **STAT_CABLE_LEN_INDICATION**
- THR = **CFG_CLI_SQUELCH_THRESHOLD**
- HYS = **CFG_CLI_SQUELCH_HYSTERESIS**
- SQL = **STAT_CLI_SQUELCH**

The following rules define the state of SQL.
**Note:** If the cable equalizer is in bypass (**STAT_CEQ_BYPASS** = 1), the device will set SQL to 0.

- If CLI > (THR + HYS), the device will set SQL to 1, otherwise:
- If CLI < (THR - HYS), the device will set SQL to 0, otherwise:
- If CLI ≥ (THR - HYS) and CLI ≤ (THR + HYS), SQL remains unchanged.
- If SQL = 1, the device will not indicate lock and the trace driver state will be defined by output state control parameters settings, see Section 4.8.7 for more details.

## Table 4-1: Cable Equalizer Status and Configuration Parameters

| Register Address$_h$ and Name | Parameter Name | Parameter Description |
|---|---|---|
| 15, CARR_ DET_CFG | CFG_SEC_CD_INCL_CLI_SQUELCH | Enables or disables squelch control. |
| 16, SQUELCH_ PARAMETERS | CFG_CLI_SQUELCH_THRESHOLD | Used to tune the squelch threshold based on the tolerance requirements of the application. |
| | CFG_CLI_SQUELCH_HYSTERESIS | Used to tune the squelch hysteresis based on the tolerance requirements of the application. |
| 20, CD_FILTER_ DELAYS_0 | CFG_CD_FILTER_SAMPLE_WIN | Primary carrier detect sampling window size. |
| 21, CD_FILTER_ DELAYS_1 | CFG_CD_FILTER_DEASSERT_CNT | Primary carrier detect de-assertion count. |
| 22, CD_FILTER_ DELAYS_2 | CFG_CD_FILTER_ASSERT_CNT | Primary carrier detect assertion count. |
| 84, STICKY_ COUNTS_0 | STAT_CNT_PRI_CD_CHANGES | A counter showing the number of times the primary Carrier Detect signal changed. |
| | STAT_CNT_SEC_CD_CHANGES | A counter showing the number of times the secondary Carrier Detect signal changed. |
| 86, CURRENT_ STATUS_0 | STAT_CLI_SQUELCH | Cable equalizer Squelch status. |
| 87, CURRENT_ STATUS_1 | STAT_PRI_CD | Primary filtered carrier detect of the analogue carrier detect signal. |
| | STAT_SEC_CD | Secondary filtered carrier detect of the analogue carrier detect signal. |
| 88, EQ_GAIN_IND | STAT_CABLE_LEN_INDICATION | SDIO cable length indication when in cable equalizer mode. |

# 4.3 Trace Equalizer

The GS3590 features a differential input buffer with 100Ω differential input termination, which includes a Trace Equalizer that can be configured to compensate for up to 60" of 7mil strip-line in FR4 at 2.97Gb/s.

**Note:** The parameters referred to within Section 4.3 to Section 4.3.2 are linked to their respective registers in Table 4-2.

The differential input signal can be either DC-coupled or AC-coupled, and is capable of operation with any binary coded signal between 1Mb/s and 2.97Gb/s.

The input circuit is compatible with industry standard CML differential transmitters when DC-coupled using industry standard 100Ω differential termination circuitry.

The Trace Equalizer includes an automatic input offset compensation circuit. This reduces offset-induced data jitter in the link due to asymmetric performance of DC-coupled upstream differential drivers. The input offset compensation circuit also improves the input sensitivity of the Trace Equalizer.

## 4.3.1 Input Trace Equalization

The Trace Equalizer can compensate for up to 17dB of insertion loss at 1.485GHz in 8 increments, which can be adjusted through the **CFG_TREQ0_BOOST** parameter in control register 0x1E. The default value of **CFG_TREQ0_BOOST** is ($0_h$), which corresponds to the minimum equalization boost level.

Please refer to Figure 4-2 for recommended boost setting.

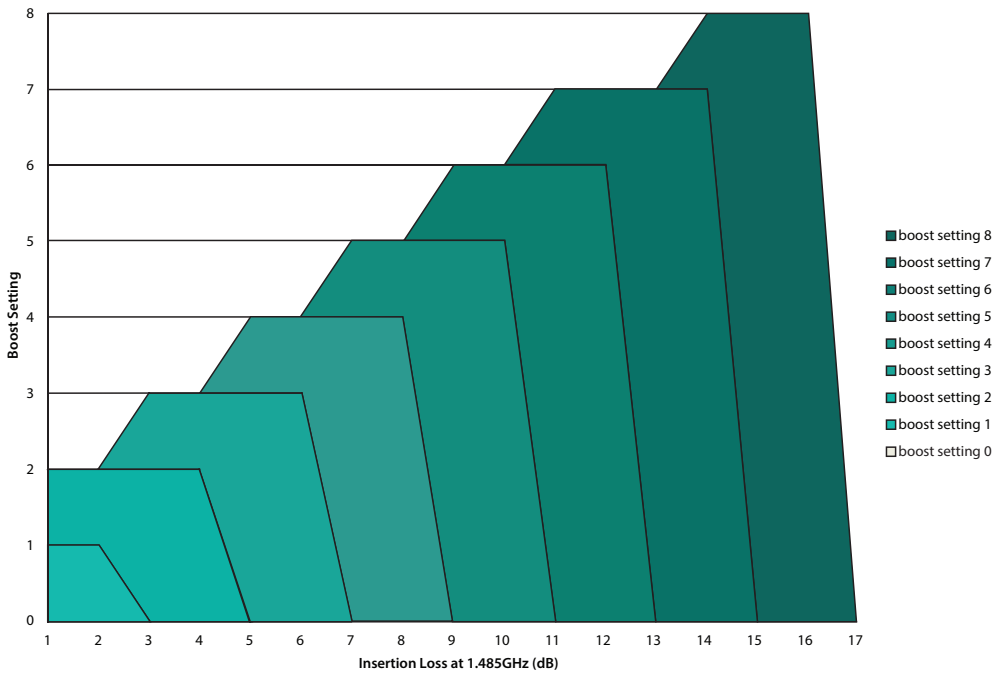



**Figure 4-2: GS3590 Trace EQ Boost Setting Recommendation**

By default at power up or after system reset, the trace equalizer is configured to compensate for up to 3" of 7mil strip-line in FR4 material at high-frequencies.

**Note:** Although not a requirement, launch swing of $800mV_{ppd}$ is recommended for trace lengths longer than 5".

## 4.3.2 CD (Carrier Detect) and LOS (Loss of Signal)

LOS is the complement of CD and is used by various automatic control modes including mute on LOS, which will be covered in the output section of this document.

The default settings of the Trace Equalizer Carrier Detection sub-block should satisfy most applications; however the Carrier Detection mechanism in the Trace Equalizer is highly-configurable and allows the system designer to optimize the sensitivity and hysteresis of Carrier Detection mechanism to meet specific system requirements.

The trace equalizer Carrier Detect is reported by status parameter **STAT_PRI_CD** in register 0x87.

The first CD control parameter is **CFG_TREQ0_CD_BOOST** in register 0x1E. This parameter determines the method and therefore the level of equalization to be used on the input signal routed to the Carrier Detection sub-block. The default value is $0_b$, which maximizes the level of equalization. Alternatively, the designer can choose to have this signal equalized at the same level as the main signal routed to the CDR by setting **CFG_TREQ0_CD_BOOST** to $1_b$. The setting of this parameter has no impact on the main signal routed to the CDR.

The last two CD control parameters can be found in register 0x1F. Parameters **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TRE0Q_CD_DEASSERT_THRESH** set the Carrier Detect assert and de-assert thresholds to the input signal, which also defines the hysteresis of CD signal.

The default values of **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TREQ0_CD_DEASSERT_THRESH** are $4_d$ and $3_d$ respectively. With the default settings, the minimum launch swing needed to assert the carrier detect is 200mV and it will be de-asserted when the signal level falls below 150mV.

The **STAT_PRI_CD** (Carrier Detect) parameter will be set to $0_b$ and the LOS will be set to $1_b$ whenever a new signal at the input does not exceed the assert threshold, or an existing signal falls below the de-assert threshold. The result is that the device will not indicate lock, and the outputs will mute (assuming Mute on LOS is left to its default value in the **CONTROL_OUTPUT_MUTE** register—0x49). See Section 4.8.7 for more details.

Given a differential input trace with 17dB of insertion loss at 1.485GHz and **CFG_TREQ_CD_BOOST** = $0_b$, Figure 4-3 illustrates the relationship between launch swing voltage, and minimum threshold setting to assert or de-asset Carrier Detect at all rates up to threshold setting at 2.97Gb/s.

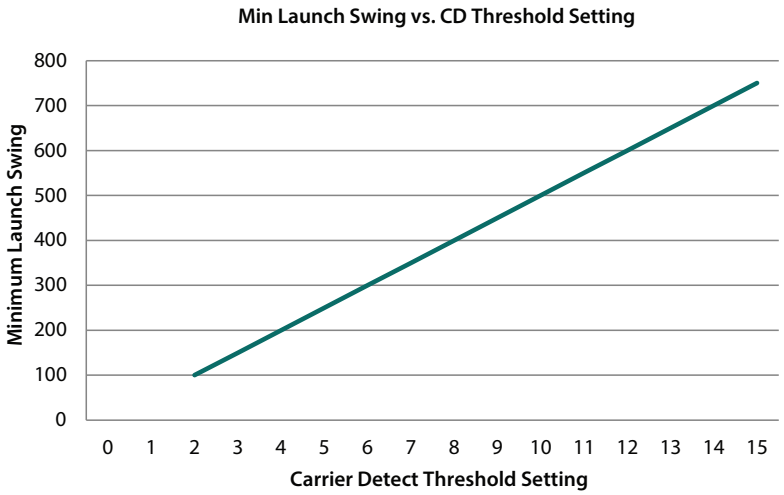



**Figure 4-3: Input Voltage Vs. Carrier Detect Threshold Setting**

### Table 4-2: Trace Equalizer Status and Configuration Parameters

| Register Address$_h$ and Name | Parameter Name | Description |
|---|---|---|
| 84, STICKY_ COUNTS_0 | STAT_CNT_PRI_CD_CHANGES | A counter showing the number of times the primary Carrier Detect signal changed. |
| 87, CURRENT_ STATUS_1 | STAT_PRI_CD | Primary filtered carrier detect of the analogue carrier detect signal. |
| 1F, TREQ0_CD_ HYSTERESIS | CFG_TREQ0_CD_ASSERT_THRESH | Sets the Carrier Detect assert threshold. |
| | CFG_TREQ0_CD_DEASSERT_THRESH | Sets the Carrier Detect de-assert threshold. |
| 1E, TREQ0_ INPUT_BOOST | CFG_TREQ0_BOOST | Sets the Trace Equalizer boost level. |
| | CFG_TREQ0_CD_BOOST | Selects the boost method of the CD signal. |

# 4.4 Serial Digital Re-timer (CDR)

The GS3590 includes an integrated CDR, whose purpose is to lock to a valid incoming signal from the Cable Equalizer stage (when operating in cable equalizer mode) or the Trace Equalizer stage (when operating in cable driver mode) and produce a lower jitter signal at the Cable Driver or Trace Driver outputs. The CDR has the ability to lock to any of the following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), and 3G-SDI (2.97Gb/s). This includes the f/1.001 rates.

The default settings of the re-timer block are optimal for most applications. However, the following controls allow the user to customize the behaviour of the re-timer: LBW control, Automatic and Manual Rate Detection.

**Note:** The parameters referred to within Section 4.4.1 to Section 4.4.2 are linked to their respective registers in Table 4-4: CDR Control and Status Parameters. For a complete list of registers and functions, please see Section 5.