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# GS4901B/GS4900B SD Clock and Timing Generator with GENLOCK

## Key Features

### Video Clock Synthesis

- Pre-programmed for 4 video clock periods (14.32 MHz, 27 MHz, 36 MHz, and 54 MHz)
- Accuracy of free-running clock frequency limited only by crystal reference
- One differential and two single-ended video clock outputs
- Each clock may be individually delayed for skew control
- Video output clock may be directly connected to Gennum's serializers for a SMPTE-compliant SDI output

### Audio Clock Synthesis (GS4901B only)

- Three audio clock outputs
- Generates any audio clock up to 512*96kHz
- Pre-programmed for 7 audio clocks

### Timing Generation

- Generates up to 8 timing signals at a time
- Choose from 9 pre-programmed timing signals: H and V sync and blanking, F Sync, F Digital, AFS (GS4901B only), Display Enable, 10FID, and up to 4 user-defined timing signals
- Pre-programmed to generate timing for 9 different video formats

### Genlock Capability

- Clocks may be free-running or genlocked to an input reference with a variable offset step size of 100-200ps (depending on exact clock frequency)
- Variable timing offset step size of 100-200ps up to one frame
- Output may be cross-locked to a different input reference
- Freeze operation on loss of reference
- Optional crash or drift lock on application of reference
- Automatic input format detection

### General Features

- Reduces design complexity and saves board space - 9mm x 9mm package plus crystal reference replaces multiple VCXOs, PLLs and timing generators
- Pb-free and RoHS Compliant
- Low power operation typically 300mW
- 1.8V core and 1.8V or 3.3V I/O power supplies
- 64-PIN QFN package

## Applications

- Video cameras; Digital audio and/or video recording/play back devices; Digital audio and/or video processing devices; Computer/video displays; DVD/MPEG devices; Digital Set top boxes; Video projectors; High definition video systems; Multi-media PC applications

## Description

The GS4901B is a highly flexible, digitally controlled clock synthesis circuit and timing generator with genlock capability. It can be used to generate video and audio clocks and timing signals, and allows multiple devices to be genlocked to an input reference.

The GS4900B includes all the features of the GS4901B, but does not offer audio clocks or AFS pulse generation.

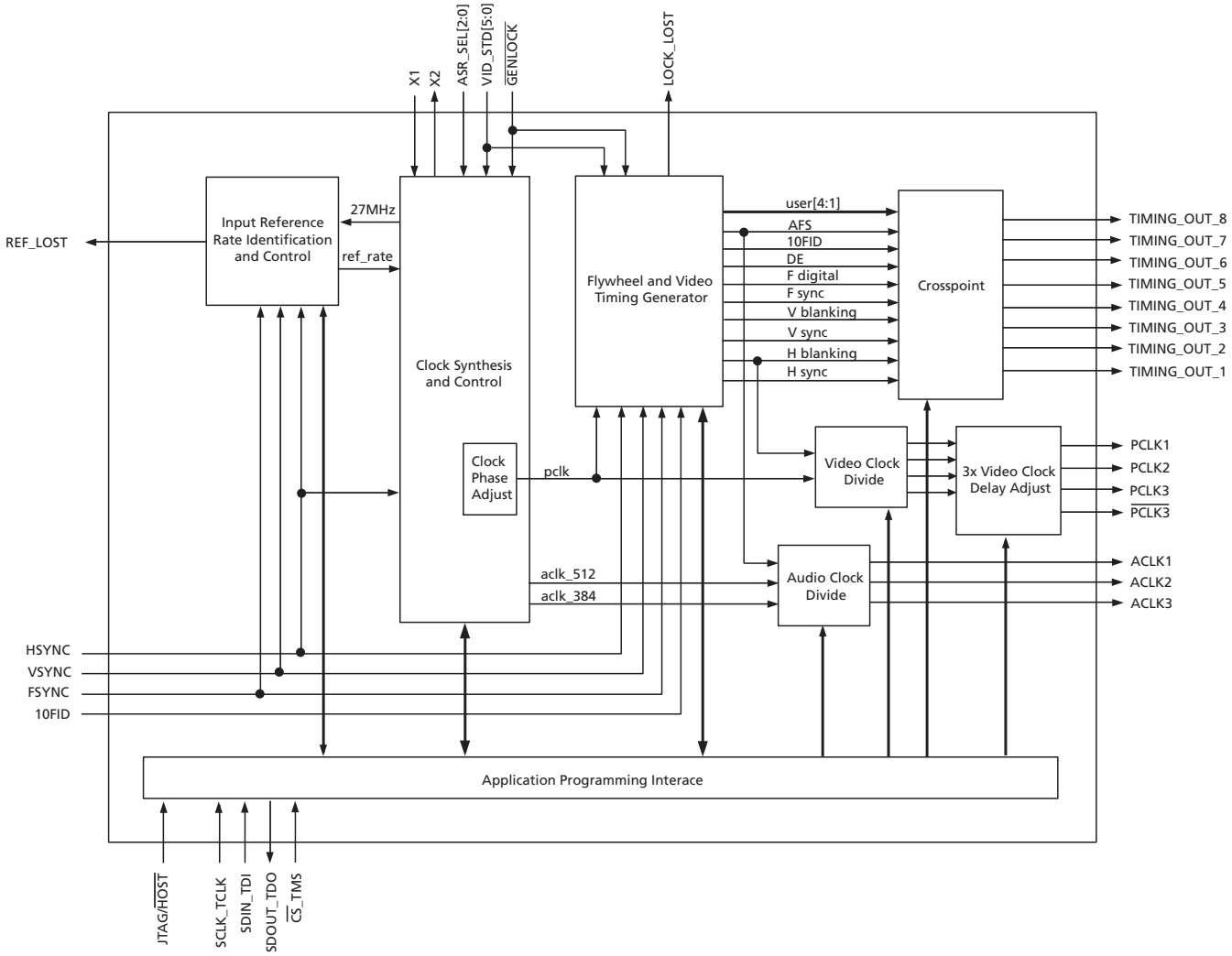
The GS4901B/GS4900B will recognize input reference signals conforming to 36 different video standards, and will genlock the output timing information to the incoming reference. The GS4901B/GS4900B supports cross-locking, allowing the output to be genlocked to an incoming reference that is different from the output video standard selected.

The user may select to output one of 4 different video sample clock rates. The chosen clock frequency can be further divided using internal dividers, and is available on two video clock outputs and one LVDS video clock output pair. The video clocks are frequency and phased-locked to the horizontal timing reference, and can be individually delayed with respect to the timing outputs for clock skew control.

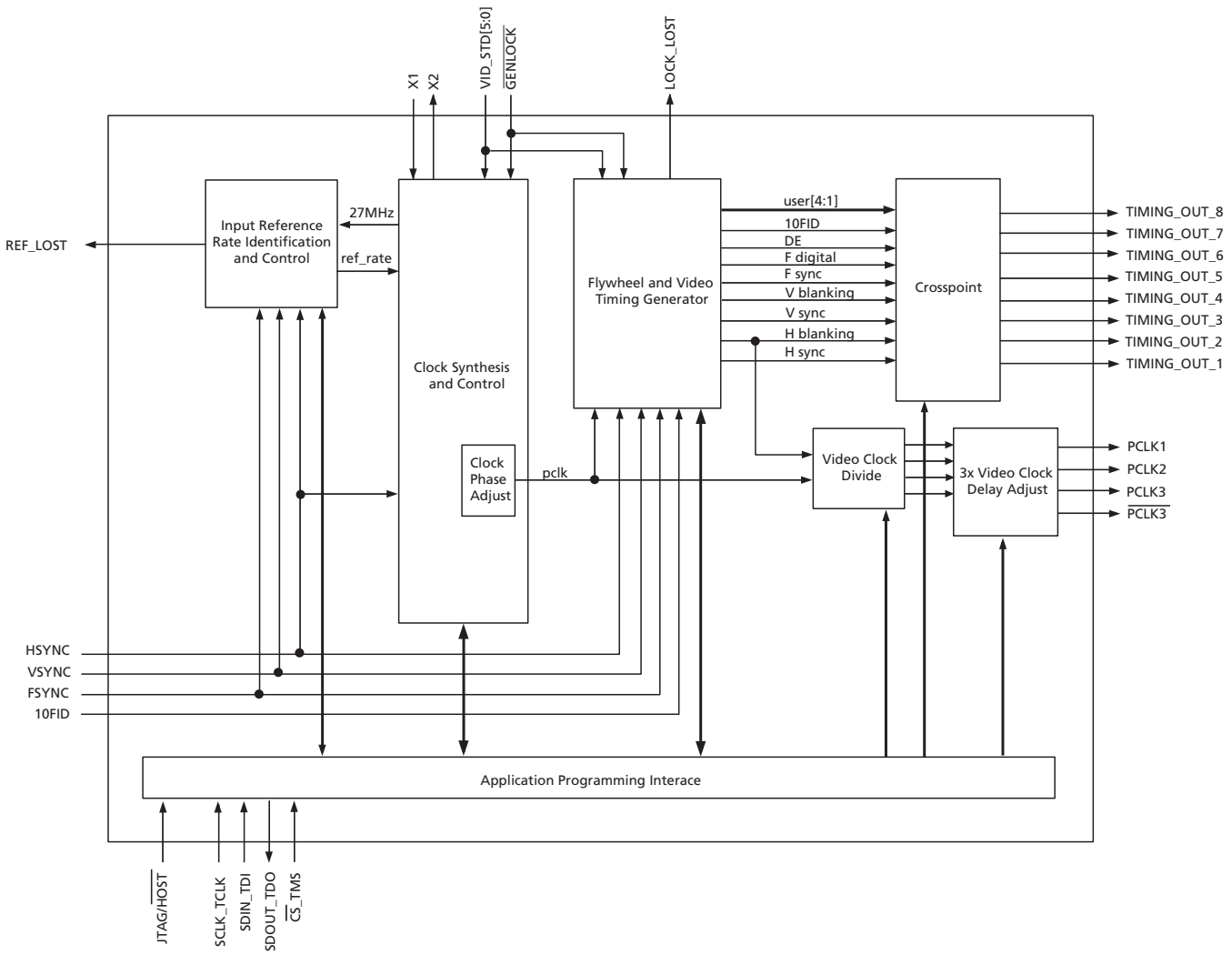
Eight user-selectable timing outputs are provided that can automatically produce the following timing signals for 9 different video formats: HSync, Hblanking, VSync, Vblanking, F sync, F digital, AFS (GS4901B only), DE, and 10FID. These timing outputs may be locked to the input reference signal for genlock timing and may be phase adjusted via internal registers.

In addition, the GS4901B provides three audio sample clock outputs that can produce audio clocks up to 512fs with fs ranging from 9.7kHz to 96kHz. Audio to video phasing is accomplished by an external 10FID input reference, a 10FID signal specified via internal registers, or a user-programmed audio frame sequence.

The GS4901B/GS4900B is Pb-free, and the encapsulation compound does not contain halogenated flame retardant (RoHS Compliant).




**GS4901B Functional Block Diagram**




**GS4900B Functional Block Diagram**

# Contents

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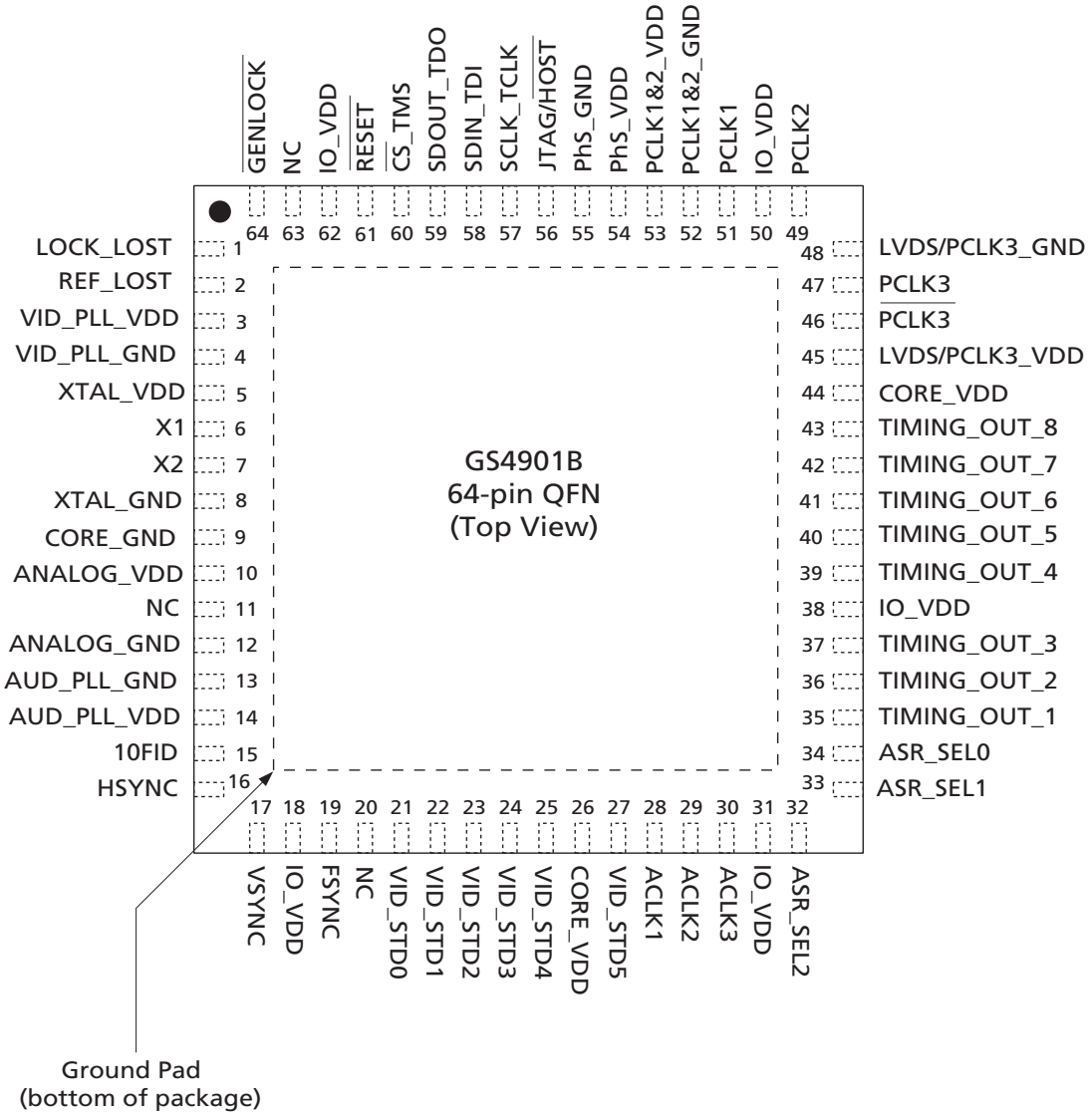
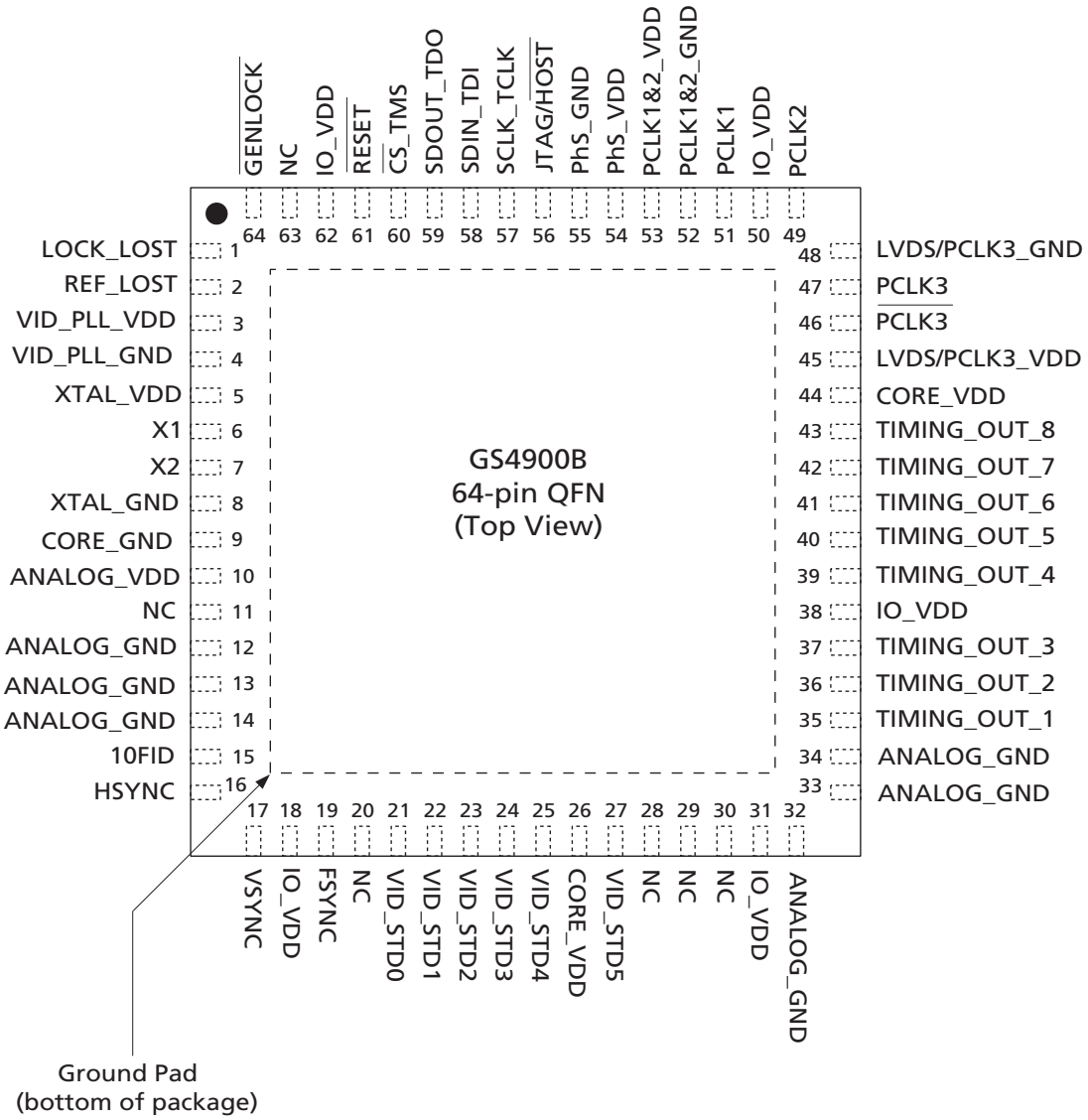
# 1. Pin Out

## 1.1 GS4901B Pin Assignment



## 1.2 GS4900B Pin Assignment



## 1.3 Pin Descriptions

**Table 1-1: Pin Descriptions**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 1 | LOCK_LOST | Non Synchronous | Output | STATUS SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>This pin will be HIGH if the output is not genlocked to the input.<br>The GS4901B/GS4900B monitors the output pixel/line counters, as well as the internal lock status from the genlock block and asserts LOCK_LOST HIGH if it is determined that the output is not genlocked to the input. This pin will be LOW if the device successfully genlocks the output clock and timing signals to the input reference.<br>If LOCK_LOST is LOW, the reference timing generator outputs will be phase locked to the detected reference signal, producing an output in accordance with the video standard selected by the VID_STD[5:0] pins. |
| 2 | REF_LOST | Non Synchronous | Output | STATUS SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>This pin will be HIGH if:<br>• No input reference signal is applied to the device; or<br>• The input reference applied does not meet the minimum/maximum timing requirements described in Section 3.5.2 on page 44.<br>This pin will be LOW otherwise.<br>If the reference signal is removed when the device is in Genlock mode, REF_LOST will go HIGH and the GS4901B/GS4900B will enter Freeze mode (see Section 3.2.1.2 on page 39). |
| 3 | VID_PLL_VDD | – | Power Supply | Most positive power supply connection for the video clock synthesis internal block. Connect to +1.8V DC. |
| 4 | VID_PLL_GND | – | Power Supply | Ground connection for the video clock synthesis internal block. Connect to GND. |
| 5 | XTAL_VDD | – | Power Supply | Most positive power supply connection for the crystal buffer. Connect to either +1.8V DC or +3.3V DC.<br>NOTE: Connect to +3.3V for minimum output PCLK jitter. |
| 6 | X1 | Non Synchronous | Input | ANALOG SIGNAL INPUT<br>Connect to a 27MHz crystal or a 27MHz external clock source. See Figure 1-1. |
| 7 | X2 | Non Synchronous | Output | ANALOG SIGNAL OUTPUT<br>Connect to a 27MHz crystal, or leave this pin open circuit if an external clock source is applied to pin 6. See Figure 1-1. |
| 8 | XTAL_GND | – | Power Supply | Ground connection for the crystal buffer. Connect to GND. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 9 | CORE_GND | – | Power Supply | Ground connection for core and I/O. Solder to the ground plane of the application board.<br>NOTE: The CORE_GND pin should be soldered to the same main ground plane as the exposed ground pad on the bottom of the device. |
| 10 | ANALOG_VDD | – | Power Supply | Most positive power supply connection for the analog input block. Connect to +1.8V DC. |
| 11, 20, 63 | NC | – | – | Do not connect. |
| 12 | ANALOG_GND | – | Power Supply | Ground connection for the analog input block. Connect to GND. |
| 13 | AUD_PLL_GND (GS4901B only) | – | Power Supply | Ground connection for the audio clock synthesis internal block. Connect to GND. |
| | ANALOG_GND (GS4900B only) | – | Power Supply | Ground connection for the analog input block. Connect to GND. |
| 14 | AUD_PLL_VDD (GS4901B only) | – | Power Supply | Most positive power supply connection for the audio clock synthesis internal block. Connect to +1.8V DC. |
| | ANALOG_GND (GS4900B only) | – | Power Supply | Ground connection for the analog input block. Connect to GND. |
| 15 | 10FID | Non Synchronous | Input | REFERENCE SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>The 10FID external reference signal is applied to this pin by the application layer. 10FID defines the field in which the video and audio clock phase relationship is defined according to SMPTE 318-M. It is also used to define a 3:2 video cadence.<br>NOTE: If the input reference format does not include a 10 Field ID signal, this pin should be held LOW. See Section 3.4.2 on page 42. |
| 16 | HSYNC | Non Synchronous | Input | REFERENCE SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>The HSYNC external reference signal is applied to this pin by the application layer. When the GS4901B/GS4900B is operating in Genlock mode, the device senses the polarity of the HSYNC input automatically, and references to the leading edge.<br>This signal must adhere to one of the 36 defined video standards supported by the device. In this mode of operation, the HSYNC input provides a horizontal scanning reference signal.<br>The HSYNC signal may have analog timing, such as from a sync separator, or may be digital such as from an SDI deserializer. Section 1.4 on page 19 describes the 36 video formats recognized by the GS4901B/GS4900B. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 17 | VSYNC | Non Synchronous | Input | REFERENCE SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>The VSYNC external reference signal is applied to this pin by the application layer. When the GS4901B/GS4900B is operating in Genlock mode, the device senses the polarity of the VSYNC input automatically, and references to the leading edge.<br>This signal must adhere to one of the 36 defined video standards supported by the device. In this mode of operation, the VSYNC input provides a vertical scanning reference signal.<br>The VSYNC signal may have analog timing, such as from a sync separator, or may be digital such as from an SDI deserializer. Section 1.4 on page 19 describes the 36 video formats recognized by the GS4901B/GS4900B. |
| 18, 31, 38, 50, 62 | IO_VDD | – | Power Supply | Most positive power supply connection for the digital I/O signals. Connect to either +1.8V DC or +3.3V DC.<br>NOTE: All five IO_VDD pins must be powered by the same voltage. |
| 19 | FSYNC | Non Synchronous | Input | REFERENCE SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>The FSYNC external reference signal is applied to this pin by the application layer.<br>The first field is defined as the field in which the first broad pulse (also known as serration) is in the first half of a line. The FSYNC signal should be set HIGH during the first field for sync-based references.<br>Then this signal must adhere to one of the 36 defined video standards supported by the device. In this mode of operation, the FSYNC input provides an odd/even field input reference.<br>The FSYNC signal may have analog timing, such as from a sync separator, or may be digital such as from an SDI deserializer. Section 1.4 on page 19 describes the 36 video formats recognized by the GS4901B/GS4900B.<br>For blanking-based references, the FSYNC signal should be set HIGH during the second field.<br>NOTE: If the input reference format does not include an F sync signal, this pin should be held LOW. |
| 27, 25, 24, 23, 22, 21 | VID_STD[5:0] | Non Synchronous | Input | CONTROL SIGNAL INPUTS<br>Signal levels are LVCMOS/LVTTL compatible.<br>Video Standard Select.<br>Used to select the desired video format for video clock and timing signal generation.<br>4 different video sample clocks, as well as 9 different video format timing signal outputs may be selected using these pins.<br>NOTE: The VID_STD[5:4] pins should be grounded by the application layer since these pins are not required to select output video standards 1 to 10.<br>For details on the supported video standards and video clock frequency selection, please see Section 1.4 on page 19. |
| 26, 44 | CORE_VDD | – | Power Supply | Most positive power supply connection for the digital core. Connect to +1.8V DC. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 28, 29, 30 | ACLK1<br>ACLK2<br>ACLK3<br>(GS4901B only) | – | Output | CLOCK SIGNAL OUTPUTS<br>Signal levels are LVCMOS/LVTTL compatible.<br>Audio output clock signals.<br>ACLK1, ACLK2, and ACLK3 present audio sample rate clock outputs to the application layer.<br>By default, after system reset, the audio clock output pins of the device provide clock signals as follows:<br>ACLK1 = 256fs<br>ACLK2 = 64fs<br>ACLK3 = fs, where fs is the fundamental sampling frequency.<br>The fundamental sampling frequency is selected using ASR_SEL[2:0]. Additional sampling frequencies may be programmed in the host interface.<br>It is also possible to select different division ratios for each of the audio clock outputs by programming designated registers in the host interface. Clock outputs of 512fs, 384fs, 256fs, 192fs, 128fs, 64fs, fs and z bit are selectable on a pin-by-pin basis.<br>NOTE: ACLK1-3 will have a 50% duty cycle, unless fs is selected as 96kHz and the host interface is configured such that one of the three ACLK pins is set to output a clock signal at 192fs or 384fs. If this is the case, then a 512fs clock will have a 33% duty cycle.<br>These signals will be high impedance when ASR_SEL[2:0] = 000b. |
| | NC<br>(GS4900B only) | – | – | Do not connect. |
| 32, 33, 34 | ASR_SEL[2:0]<br>(GS4901B only) | Non Synchronous | Input | CONTROL SIGNAL INPUTS<br>Signal levels are LVCMOS/LVTTL compatible.<br>Audio Sample Rate Select.<br>Used to select the fundamental sampling frequency, fs, of the audio clock outputs. See Table 3-7.<br>When ASR_SEL[2:0] = 000b, audio clock generation will be disabled and the ACLK1 to ACLK3 pins will be high impedance. In this case, AUD_PLL_VDD (pin 14) may be connected to GND to minimize noise and power consumption. |
| | ANALOG_GND<br>(GS4900B only) | – | Power Supply | Ground connection for the analog input block. Connect to GND. |
| 35 | TIMING_OUT_1 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 23 for signal descriptions.<br>NOTE: Default output is H Sync.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 36 | TIMING_OUT_2 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 23 for signal descriptions.<br>NOTE: Default output is H blanking.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 37 | TIMING_OUT_3 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 23 for signal descriptions.<br>NOTE: Default output is V Sync.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 39 | TIMING_OUT_4 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 23 for signal descriptions.<br>NOTE: Default output is V blanking.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 40 | TIMING_OUT_5 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 23 for signal descriptions.<br>NOTE: Default output is F Sync.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 41 | TIMING_OUT_6 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 23 for signal descriptions.<br>NOTE: Default output is F digital.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 42 | TIMING_OUT_7 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 23 for signal descriptions.<br>NOTE: Default output is 10 Field ID (10FID).<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 43 | TIMING_OUT_8 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 23 for signal descriptions.<br>NOTE: Default output is Display Enable (DE).<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 45 | LVDS/PCLK3_VDD | – | Power Supply | Most positive power supply connection for PCLK3 output circuitry and LVDS driver. Connect to +1.8V DC. |
| 46, 47 | $\overline{\text{PCLK3}}$, PCLK3 | – | Output | CLOCK SIGNAL OUTPUTS<br>Signal levels are LVDS compatible.<br>Differential video clock output signal.<br>PCLK3/$\overline{\text{PCLK3}}$ present a differential video sample rate clock output to the application layer.<br>By default, after system reset, this output will operate at the fundamental frequency determined by the setting of the VID_STD[5:0] pins. It is possible to define other non-standard fundamental clock rates using the host interface.<br>It is also possible to select different division ratios for the PCLK3/$\overline{\text{PCLK3}}$ outputs by programming designated registers in the host interface. A clock output of the fundamental rate, fundamental rate ÷2, or fundamental rate ÷4 may be selected.<br>The PCLK3/$\overline{\text{PCLK3}}$ outputs will be high impedance when VID_STD[5:0] = 00h. |
| 48 | LVDS/PCLK3_GND | – | Power Supply | Ground connection for PCLK3 output circuitry and LVDS driver. Connect to GND. |
| 49 | PCLK2 | – | Output | CLOCK SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Video clock output signal.<br>PCLK2 presents a video sample rate clock output to the application layer.<br>By default, after system reset, the PCLK2 output pin will operate at the fundamental frequency determined by the setting of the VID_STD[5:0] pins. It is possible to define other non-standard fundamental clock rates using the host interface.<br>It is also possible to select different division ratios for the PCLK2 output by programming designated registers in the host interface. A clock output of the fundamental rate, fundamental rate ÷2, or fundamental rate ÷4 may be selected.<br>By setting designated registers in the host interface, the current drive capability of this pin may be set high or low. By default, the current drive will be low.<br>The PCLK2 output will be held LOW when VID_STD[5:0] = 00h. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 51 | PCLK1 | – | Output | CLOCK SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Video clock output signal.<br>PCLK1 presents a video sample rate clock output to the application layer.<br>By default, after system reset, the PCLK1 output pin will operate at the fundamental frequency determined by the setting of the VID_STD[5:0] pins. It is possible to define other non-standard fundamental clock rates using the host interface.<br>It is also possible to select different division ratios for the PCLK1 output by programming designated registers in the host interface. A clock output of the fundamental rate, fundamental rate ÷2, or fundamental rate ÷4 may be selected.<br>By setting designated registers in the host interface, the current drive capability of this pin may be set high or low. By default, the current drive will be low.<br>The PCLK1 output will be held LOW when VID_STD[5:0] = 00h. |
| 52 | PCLK1&2_GND | – | Power Supply | Ground connection for PCLK1&2 circuitry. Connect to GND. |
| 53 | PCLK1&2_VDD | – | Power Supply | Most positive power supply connection for PCLK1&2 circuitry. Connect to +1.8V DC. |
| 54 | PhS_VDD | – | Power Supply | Most positive power supply connection for the video clock phase shift internal block. Connect to +1.8V DC. |
| 55 | PhS_GND | – | Power Supply | Ground connection for the video clock phase shift internal block. Connect to GND. |
| 56 | JTAG/$\overline{\text{HOST}}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to select JTAG Test Mode or Host Interface Mode.<br>When set HIGH, $\overline{\text{CS}}$_TMS, SCLK_TCLK, SDOUT_TDO, and SDIN_TDI are configured for JTAG boundary scan testing.<br>When set LOW, $\overline{\text{CS}}$_TMS, SCLK_TCLK, SDOUT_TDO, and SDIN_TDI are configured as GSPI pins for normal host interface operation. |
| 57 | SCLK_TCLK | Non Synchronous | Input | SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Serial Data Clock / Test Clock.<br>All JTAG / Host Interface address and data are shifted into/out of the device synchronously with this clock.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>SCLK_TCLK operates as the host interface serial data clock, SCLK.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>SCLK_TCLK operates as the JTAG test clock, TCLK. |

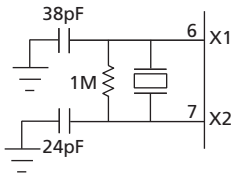
**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 58 | SDIN_TDI | Synchronous with SCLK_TCLK | Input | SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Serial Data Input / Test Data Input.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>SDIN_TDI operates as the JTAG test data input, TDI. |
| 59 | SDOUT_TDO | Synchronous with SCLK_TCLK | Output | SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Serial Data Output / Test Data Output.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>SDOUT_TDO operates as the JTAG test data output, TDO. |
| 60 | $\overline{\text{CS}}$_TMS | Synchronous with SCLK_TCLK | Input | SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Chip Select / Test Mode Select.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>$\overline{\text{CS}}$_TMS operates as the host interface chip select, $\overline{\text{CS}}$, and is active LOW.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>$\overline{\text{CS}}$_TMS operates as the JTAG test mode select, TMS, and is active HIGH. |
| 61 | $\overline{\text{RESET}}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to reset the internal operating conditions to their default settings or to reset the JTAG test sequence.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>When asserted LOW, all host registers and functional blocks will be set to their default conditions. All input and output signals will become high impedance, except PCLK1 and PCLK2, which will be set LOW.<br>When set HIGH, normal operation of the device will resume.<br>The user must hold this pin LOW during power-up and for a minimum of 500 uS after the last supply has reached its operating voltage.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>When asserted LOW, all host registers and functional blocks will be set to their default conditions and the JTAG test sequence will be held in reset.<br>When set HIGH, normal operation of the JTAG test sequence will resume. |

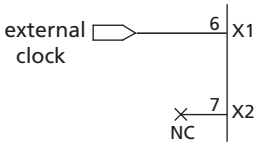
**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 64 | $\overline{\text{GENLOCK}}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selects Genlock mode or Free Run mode.<br>When this pin is set LOW and the device has successfully genlocked the output to the input reference, the device will enter Genlock mode. The video clock and timing outputs will be frequency and phase locked to the detected reference signal.<br>When this pin is set HIGH, the video clock and the reference-timing generator will free-run.<br>By default, the GS4901B's audio clocks will be genlocked to the output video clock regardless of the setting of this pin.<br>NOTE: The user must apply a reference to the input of the device prior to setting $\overline{\text{GENLOCK}}$ = LOW. If the $\overline{\text{GENLOCK}}$ pin is set LOW and no reference signal is present, the generated clock and timing outputs of the device may correspond to the internal default settings of the chip until a reference is applied. |
| – | Ground Pad | – | – | Ground pad on bottom of package must be soldered to main ground plane of PCB. |

External Crystal Connection




External Clock Source Connection




Notes:

1. Capacitor values listed represent the total capacitance, including discrete capacitance and parasitic board capacitance.

2. X1 serves as an input, which may alternatively accept a 27MHz clock source. To accomodate this, mismatched capacitor values are recommended.

Figure 1-1: XTAL1 and XTAL2 Reference Circuits

## 1.4 Pre-Programmed Recognized Video Standards

Table 1-2 describes the video standards recognized by the GS4901B/GS4900B. The device will automatically recognize VID_STD[5:0] = 1 to 10. In order to enable the device to recognize and lock to any of the HD reference formats defined by VID_STD[5:0] = 11 to 38, the user must set the corresponding bit LOW in the Reference_Standard_Disable register, located at address 11h-13h of the host interface. In addition, the user must set the HD_Reference_Enable bit of register 82h[7] HIGH.

Please see the descriptions of the Reference_Standard_Disable and HD_Reference_Enable registers in Section 3.10.3 on page 67.

If an HD reference format is left disabled in the Reference_Standard_Disable register, or if the HD_Reference_Enable bit is not set HIGH in register 82h, the device will NOT recognize this format should it be applied to the input of the device.

The user may select VID_STD[5:0] = 1 or 3-10 ONLY as output formats.

If desired, the external VID_STD[5:0] pins may be ignored by setting bit 1 of the Video_Control register, and the video standard may instead be selected via the VID_STD[5:0] register of the host interface (see Section 3.10.3 on page 67). Although the external VID_STD[5:0] pins will be ignored in this case, they should not be left floating.

NOTE: VID_STD[5:4] should always be set LOW by the application layer since these pins are not required to select output video standards 1 to 10.

**Table 1-2: Recognized Video Standards**

| VID_STD [5:0] | System Nomenclature | Video PCLK Frequency (MHz) | PCLKS / Total Line | Total Lines / Frame | PCLKS / Active Line | H Sync Width (Clocks) | H Sync Polarity | V Sync Width (Lines) | V Sync Polarity | Active Lines / Frame | Scan Format Standard |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | PCLK1&2 =LOW. PCLK3/$\overline{\text{PCLK3}}$ = High Impedance | – | – | – | – | – | – | – | – | – | – |
| 1 | 4fsc 525 / 2:1 interlace | 14.32 | 910 | 525 | 768 | 67 | negative | 3 | negative | 486 | SMPTE 244M |
| 2* | Composite PAL 625 / 2:1 interlace / 25 | – | – | 625 | – | – | negative | 2.5 | negative | 576 | – |
| 3 | 601 525 / 2:1 interlace | 27 | 1716 | 525 | 1440 | 127 | negative | 3 | negative | 486 | SMPTE 125M/267M |
| 4‡ | 601 625 / 2:1 interlace | 27 | 1728 | 625 | 1440 | 127 | negative | 2.5 | negative | 576 | ITU-R BT.601-5 |
| 5 | 601 – 18MHz 525 / 2:1 interlace | 36 | 2288 | 525 | 1920 | 169 | negative | 3 | negative | 486 | SMPTE 267M |
| 6‡ | 601 – 18 MHz 625 / 2:1 interlace | 36 | 2304 | 625 | 1920 | 169 | negative | 2.5 | negative | 576 | ITU-R BT.601-5 |
| 7 | 720x486/59.94/2:1 interlace | 54 | 3432 | 525 | 2880 | 252 | negative | 3 | negative | 486 | SMPTE RP174 / SMPTE 347M |
| 8‡ | 720x576/50/2:1 interlace | 54 | 3456 | 625 | 2880 | 252 | negative | 2.5 | negative | 576 | ITU-R BT.799 / SMPTE 347M |
| 9 | 720x483/59.94/1:1 progressive | 54 | 1716 | 525 | 1440 | 127 | negative | 6 | negative | 483 | SMPTE 293M / SMPTE 347M |
| 10 | 720x576/50/1:1 progressive | 54 | 1728 | 625 | 1440 | 127 | negative | 5 | negative | 576 | ITU-R BT.1358 / SMPTE 347M |
| 11* | 1280x720/60/1:1 progressive | 74.25 | 1650 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 12* | 1280x720/59.94/1:1 progressive | 74.175 | 1650 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |

**Table 1-2: Recognized Video Standards (Continued)**

| VID_STD [5:0] | System Nomenclature | Video PCLK Frequency (MHz) | PCLKS / Total Line | Total Lines / Frame | PCLKS / Active Line | H Sync Width (Clocks) | H Sync Polarity | V Sync Width (Lines) | V Sync Polarity | Active Lines / Frame | Scan Format Standard |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 13* | 1280/720/50/1:1 progressive | 74.25 | 1980 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 14* | 1280x720/30/1:1 progressive | 74.25 | 3300 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 15* | 1280x720/29.97/1:1 progressive | 74.175 | 3300 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 16* | 1280x720/25/1:1 progressive | 74.25 | 3960 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 17* | 1280x720/24/1:1 progressive | 74.25 | 4125 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 18* | 1280x720/23.98/1:1 progressive | 74.175 | 4125 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 19* | 1920x1035/60/2:1 interlace | 74.25 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1035 | SMPTE 260M |
| 20* | 1920x1035/59.94/2:1 interlace | 74.175 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1035 | SMPTE 260M |
| 21* | 1920x1080/60/1:1 progressive | 148.5 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 22* | 1920x1080/59.94/1:1 progressive | 148.35 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 23* | 1920x1080/50/1:1 progressive | 148.5 | 2640 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 24* | Reserved | – | – | – | – | – | – | – | – | – | – |
| 25* | 1920x1080/60/2:1 interlace | 74.25 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 26* | 1920x1080/59.94/2:1 interlace | 74.175 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |

**Table 1-2: Recognized Video Standards (Continued)**

| VID_STD [5:0] | System Nomenclature | Video PCLK Frequency (MHz) | PCLKS / Total Line | Total Lines / Frame | PCLKS / Active Line | H Sync Width (Clocks) | H Sync Polarity | V Sync Width (Lines) | V Sync Polarity | Active Lines / Frame | Scan Format Standard |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 27* | 1920x1080/50/2:1 interlace | 74.25 | 2640 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 28* | Reserved | – | – | – | – | – | – | – | – | – | – |
| 29* | 1920x1080/30/1:1 progressive | 74.25 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 30* | 1920x1080/30/PsF | 74.25 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |
| 31* | 1920x1080/29.97/1:1 progressive | 74.175 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 32* | 1920x1080/29.97/PsF | 74.175 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |
| 33* | 1920x1080/25/1:1 progressive | 74.25 | 2640 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 34* | 1920x1080/25/PsF | 74.25 | 2640 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |
| 35* | 1920x1080/24/1:1 progressive | 74.25 | 2750 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 36* | 1920x1080/24/PsF | 74.25 | 2750 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |
| 37* | 1920x1080/23.98/1:1 progressive | 74.175 | 2750 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 38* | 1920x1080/23.98/PsF | 74.175 | 2750 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |

* VID_STD[5:0] = 2 and 11-38 are recognized as input references only. In addition, VID_STD[5:0] = 11-38 must be enabled in the Reference_Standard_Disable register and the HD_Reference_Enable bit of register 82h[7] must be set HIGH before they will be recognized by the device.

‡ When VID_STD = 4, 6, or 8, the Vblanking output pulse width is 2 lines too long for field 1 and 1 line too short for field 2 when compared to the digital timing defined in ITU-R BT.656 and ITU-R BT.799.

## 1.5 Output Timing Signals

Table 1-3 describes the output timing signals available to the user via pins TIMING_OUT_1 to TIMING_OUT_8. The user may output any of the signals listed below on each pin by programming the Output_Select registers beginning at address 43h of the host interface.

**Table 1-3: Output Timing Signals**

| Signal Name | Description | Default Output Pin |
|---|---|---|
| H Sync | The H Sync signal has a leading edge at the start of the horizontal sync pulse. Its width is determined by the selected video standard (see Table 1-2).<br>In Genlock mode the leading edge of the output H Sync signal is nominally simultaneous with the half amplitude point of the reference HSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 36).<br>By default, after system reset, the polarity of the H Sync signal output will be active LOW. The polarity may be selected as active HIGH by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 67). | TIMING_OUT_1 |
| H Blanking | The H Blanking signal is used to indicate the portion of the video line not containing active video data.<br>The H Blanking signal will be LOW (default polarity) for the portion of the video line containing valid video samples. The signal will be LOW at the first valid pixel of the line, and HIGH after the last valid pixel of the line.<br>The H Blanking signal remains HIGH throughout the horizontal blanking period.<br>The width of this signal will be determined by the selected video standard (see Table 1-2).<br>When in Genlock mode, the output H Blanking signal will be phase locked to the reference HSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 36).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 67). | TIMING_OUT_2 |
| V Sync | The V Sync timing signal has a leading edge at the start of the vertical sync pulse. Its width is determined by the selected video standard (see Table 1-2).<br>The leading edge of V Sync is nominally simultaneous with the leading edge of the first broad pulse.<br>When in Genlock mode, the output V Sync signal will be phase locked to the reference VSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 36).<br>By default, after system reset, the polarity of the V Sync signal output will be active LOW. The polarity may be selected as active HIGH by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 67). | TIMING_OUT_3 |

**Table 1-3: Output Timing Signals (Continued)**

| Signal Name | Description | Default Output Pin |
|---|---|---|
| V Blanking | The V Blanking signal is used to indicate the portion of the video field/frame not containing active video lines.<br>The V Blanking signal will be LOW (default polarity) for the portion of the field/frame containing valid video data, and will be HIGH throughout the vertical blanking period.<br>The width of this signal will be determined by the selected video standard (see Table 1-2).<br>When in Genlock mode, the output V Blanking signal will be phase locked to the reference VSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 36).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 67).<br>NOTE: When VID_STD = 4, 6, or 8, the Vblanking output pulse width is 2 lines too long for field 1 and 1 line too short for field 2 when compared to the digital timing defined in ITU-R BT.656 and ITU-R BT.799. | TIMING_OUT_4 |
| F Sync | The F Sync signal is used to indicate field 1 and field 2 for interlaced video formats.<br>The F Sync signal will be HIGH (default polarity) for the entire period of field 1. It will be LOW for all lines in field 2 and for all lines in progressive scan systems.<br>The width and timing of this signal will be determined by the V Sync parameters of the selected video standard (see Table 1-2). The F Sync signal always changes state on the leading edge of V Sync.<br>When in Genlock mode, the output F Sync signal will be phase locked to the reference FSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 36).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 67). | TIMING_OUT_5 |
| F Digital | F Digital is used in digital interlaced standards to indicate field 1 and field 2.<br>The F Digital changes state at the leading edge of every V Blanking pulse. It will be LOW (default polarity) for the entire period of field 1 and for all lines in progressive scan systems. It will be HIGH for all lines in field 2 .<br>The width and timing of this signal will be determined by the timing parameters of the selected video standard (see Table 1-2).<br>When in Genlock mode, the output F Digital signal will be phase locked to the reference FSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 36).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 67). | TIMING_OUT_6 |

**Table 1-3: Output Timing Signals (Continued)**

| Signal Name | Description | Default Output Pin |
|---|---|---|
| 10 Field Identification | The 10 Field Identification (10FID) signal is used to indicate the 10-field sequence for 29.97Hz, 30Hz, 59.94Hz and 60Hz video standards. It will be LOW for output standards with other frame rates.<br>The sequence defines the phase relationship between film frames and video frames, so that cadence may be maintained in mixed format environments.<br>The 10FID signal will be HIGH (default polarity) for one line at the start of the 10-field sequence. It will be LOW for all other lines. The signal's rising and falling edges will be simultaneous with the leading edge of the H Sync output signal.<br>Alternatively, by setting bit 4 of the Video_Control register (see Section 3.10.3 on page 67), the 10FID output signal may be configured to go HIGH (default polarity) on the leading edge of the H Sync output on line 1 of the first field in the 10 field sequence, and be reset LOW on the leading edge of the H Sync pulse of the first line of the second field in the 10 field sequence.<br>When in Genlock mode, the output 10FID signal will be phase locked to the 10FID reference input. If a 10FID input is not provided to the device, the user must configure the 10FID output using register 1Ah of the host interface (see Section 3.8.1 on page 58).<br>For applications involving audio, this signal may be used in place of the AFS signal if the format selected is appropriate for a 10 field AFS repetition rate, and the desired phase relationship of audio to video clock phasing coincides with the desired film frame cadence.<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 67).<br>Please see Section 3.8.1 on page 58 for more detail on the 10FID output signal. | TIMING_OUT_7 |
| Display Enable | The Display Enable (DE) signal is used to indicate the display enable for graphic display interfaces.<br>This signal will be HIGH (default polarity) whenever pixel information is to be displayed on the display device (i.e. whenever both H Blanking and V Blanking are in the active video state)<br>The width and timing of this signal will be determined by the timing parameters of the selected video standard (see Table 1-2).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 67). | TIMING_OUT_8 |