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GS4911B/GS4910B HD/SD/Graphics Clock and Timing Generator with GENLOCK

Key Features

Video Clock Synthesis

- Generates any video or graphics clock up to 165MHz
- Pre-programmed for 8 video and 13 graphics clocks
- Accuracy of free-running clock frequency limited only by crystal reference
- One differential and two single-ended video/graphics clock outputs
- Each clock may be individually delayed for skew control
- Video output clock may be directly connected to Gennum's serializers for a SMPTE-compliant HD-SDI output

Audio Clock Synthesis (GS4911B only)

- Three audio clock outputs
- Generates any audio clock up to 512*96kHz
- Pre-programmed for 7 audio clocks

Timing Generation

- Generates up to 8 timing signals at a time
- Choose from 9 pre-programmed timing signals: H and V sync and blanking, F Sync, F Digital, AFS (GS4911B only), Display Enable, 10FID, and up to 4 user-defined timing signals
- Pre-programmed to generate timing for 35 different video formats and 13 different graphic display formats

Genlock Capability

- Clocks may be free-running or genlocked to an input reference with a variable offset step size of 100-200ps (depending on exact clock frequency)
- Variable timing offset step size of 100-200ps up to one frame
- Output may be cross-locked to a different input reference
- Freeze operation on loss of reference
- Optional crash or drift lock on application of reference
- Automatic input format detection

General Features

- Reduces design complexity and saves board space - 9mm x 9mm package plus crystal reference replaces multiple VCXOs, PLLs and timing generators
- Pb-free and RoHS Compliant
- Low power operation typically 300mW
- 1.8V core and 1.8V or 3.3V I/O power supplies
- 64-PIN QFN package

Applications

- Video cameras; Digital audio and/or video recording/play back devices; Digital audio and/or video processing devices; Computer/video displays; DVD/MPEG devices; Digital Set top boxes; Video projectors; High definition video systems; Multi-media PC applications

Description

The GS4911B is a highly flexible, digitally controlled clock synthesis circuit and timing generator with genlock capability. It can be used to generate video and audio clocks and timing signals, and allows multiple devices to be genlocked to an input reference.

The GS4910B includes all the features of the GS4911B, but does not offer audio clocks or AFS pulse generation.

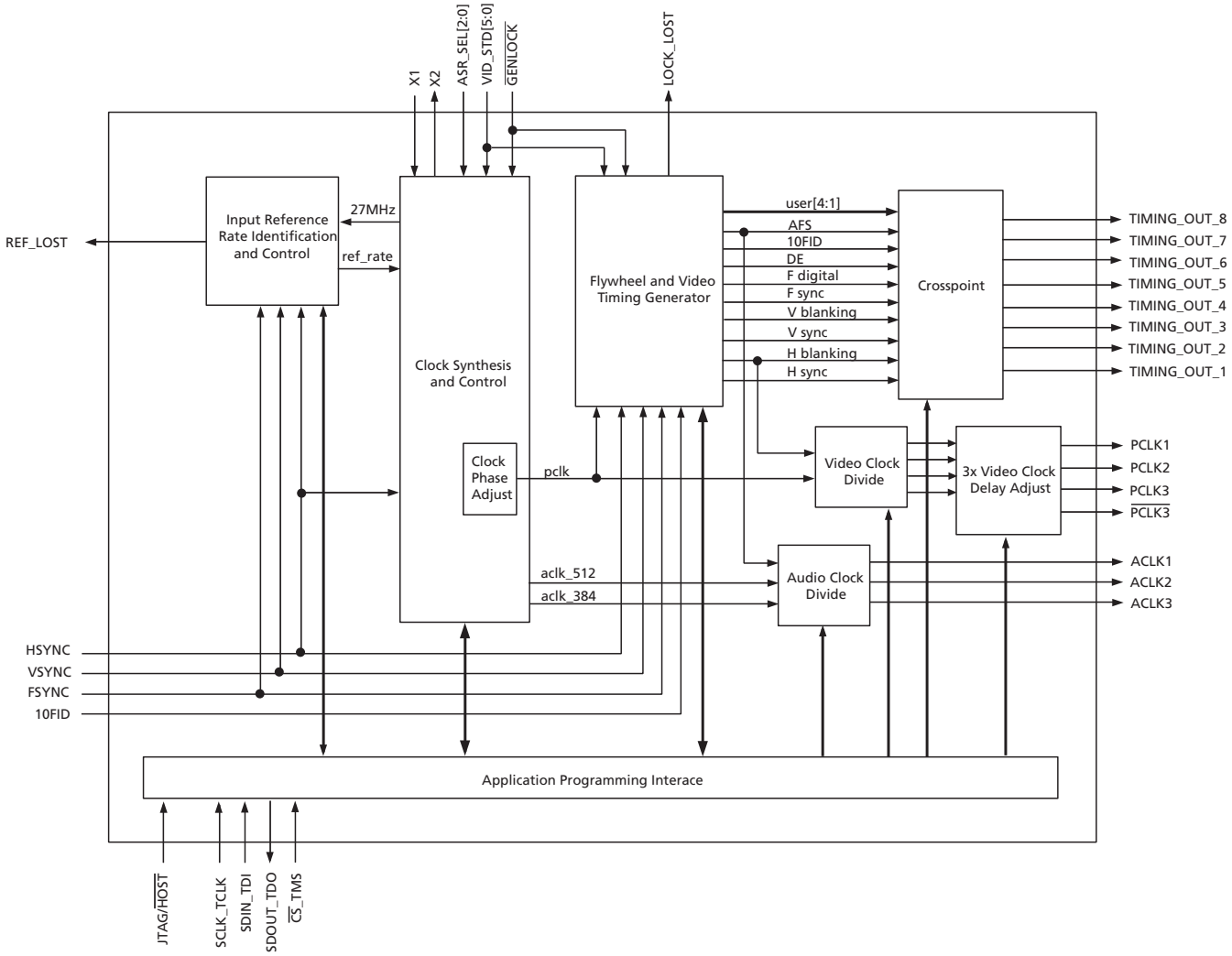
The GS4911B/GS4910B will recognize input reference signals conforming to 36 different video standards and 16 different graphic formats, and will genlock the output timing information to the incoming reference. The GS4911B/GS4910B supports cross-locking, allowing the output to be genlocked to an incoming reference that is different from the output video standard selected.

The user may select to output one of 8 different video sample clock rates or 13 different graphic display clock rates, or may program any clock frequency between 13.5MHz and 165MHz. The chosen clock frequency can be further divided using internal dividers, and is available on two video clock outputs and one LVDS video clock output pair. The video clocks are frequency and phased-locked to the horizontal timing reference, and can be individually delayed with respect to the timing outputs for clock skew control.

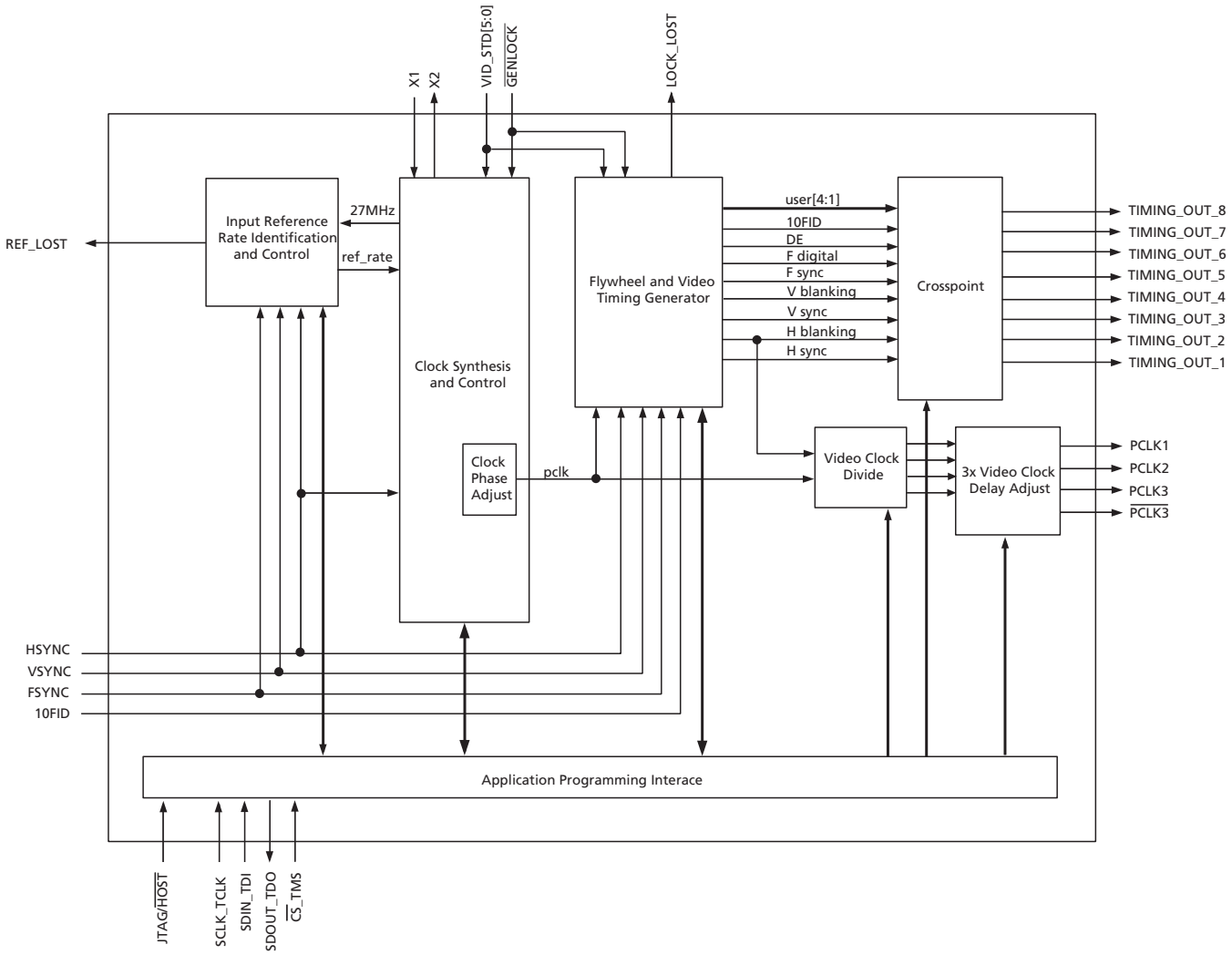
Eight user-selectable timing outputs are provided that can automatically produce the following timing signals for 35 different video formats and 13 different graphics formats: HSync, Hblanking, VSync, Vblanking, F sync, F digital, AFS (GS4911B only), DE, and 10FID. These timing outputs may be locked to the input reference signal for genlock timing and may be phase adjusted via internal registers.

In addition, the GS4911B provides three audio sample clock outputs that can produce audio clocks up to 512fs with fs ranging from 9.7kHz to 96kHz. Audio to video phasing is accomplished by an external 10FID input reference, a 10FID signal specified via internal registers, or a user-programmed audio frame sequence.

The GS4911B/GS4910B is Pb-free, and the encapsulation compound does not contain halogenated flame retardant (RoHS Compliant).



GS4911B Functional Block Diagram



GS4910B Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
5	151938	–	June 2009	Updated document with new template.
4	144904	–	April 2007	Corrected H_Offset value in 3.2.1.1 Genlock Timing Offset.
3	141424	40495	August 2006	Updated terminal width to 0.25+/-0.05 on Package Dimensions and pin 1 ID change to 45° chamfer.
2	139291	38723	April 2006	Corrected description and formulas for loop bandwidth. Converted to Data Sheet. Clarified setting of VID_STD in Extended Audio Mode. Updated power consumption of GS4910B.
1	138866	37792	December 2005	Corrected phrasing regarding user-programmable outputs. Added note on V Blanking output width for VID_STD=4, 6, 8. Corrected ESD protection to 1kV.
0	138004	–	November 2005	New document.

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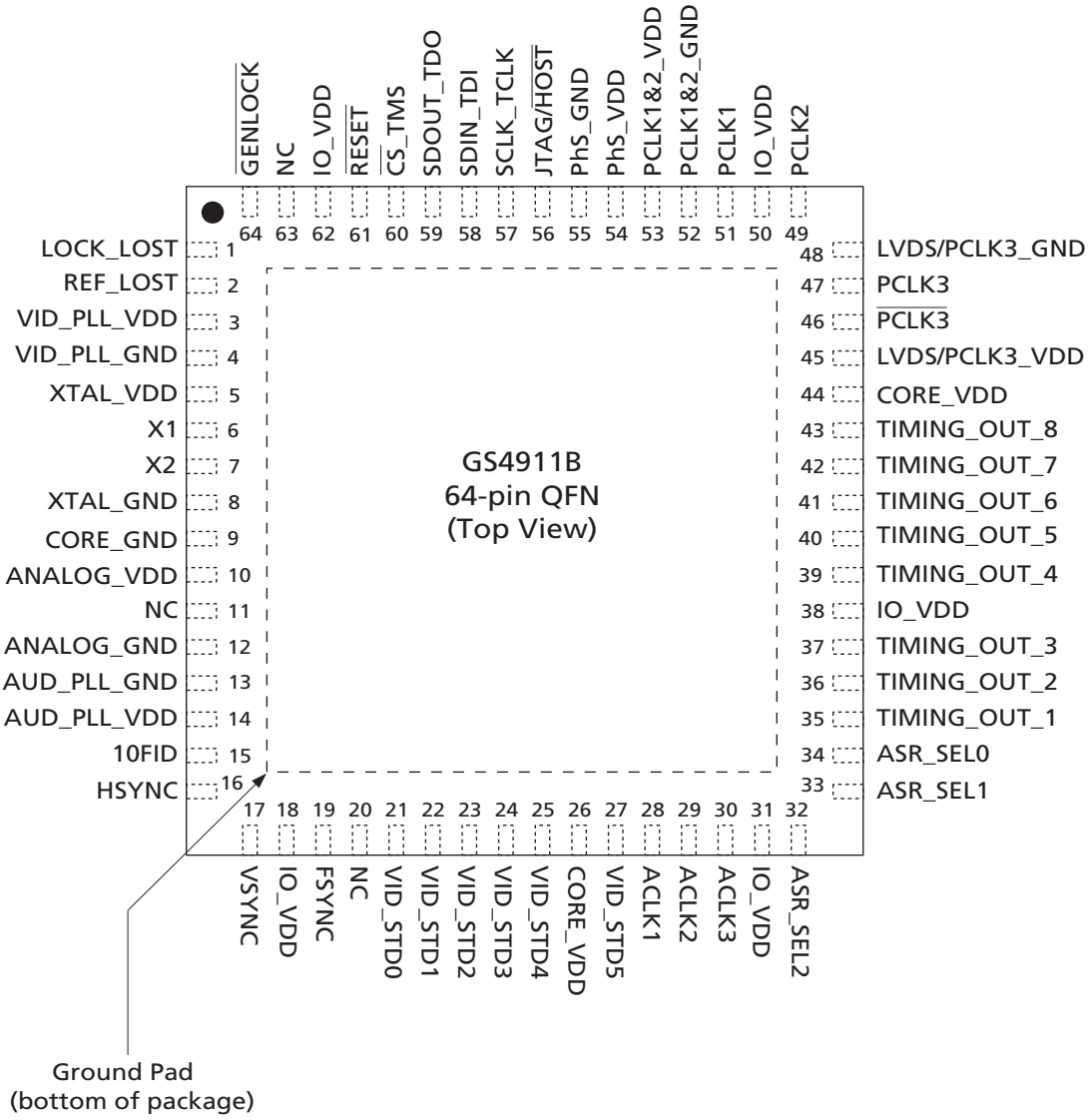
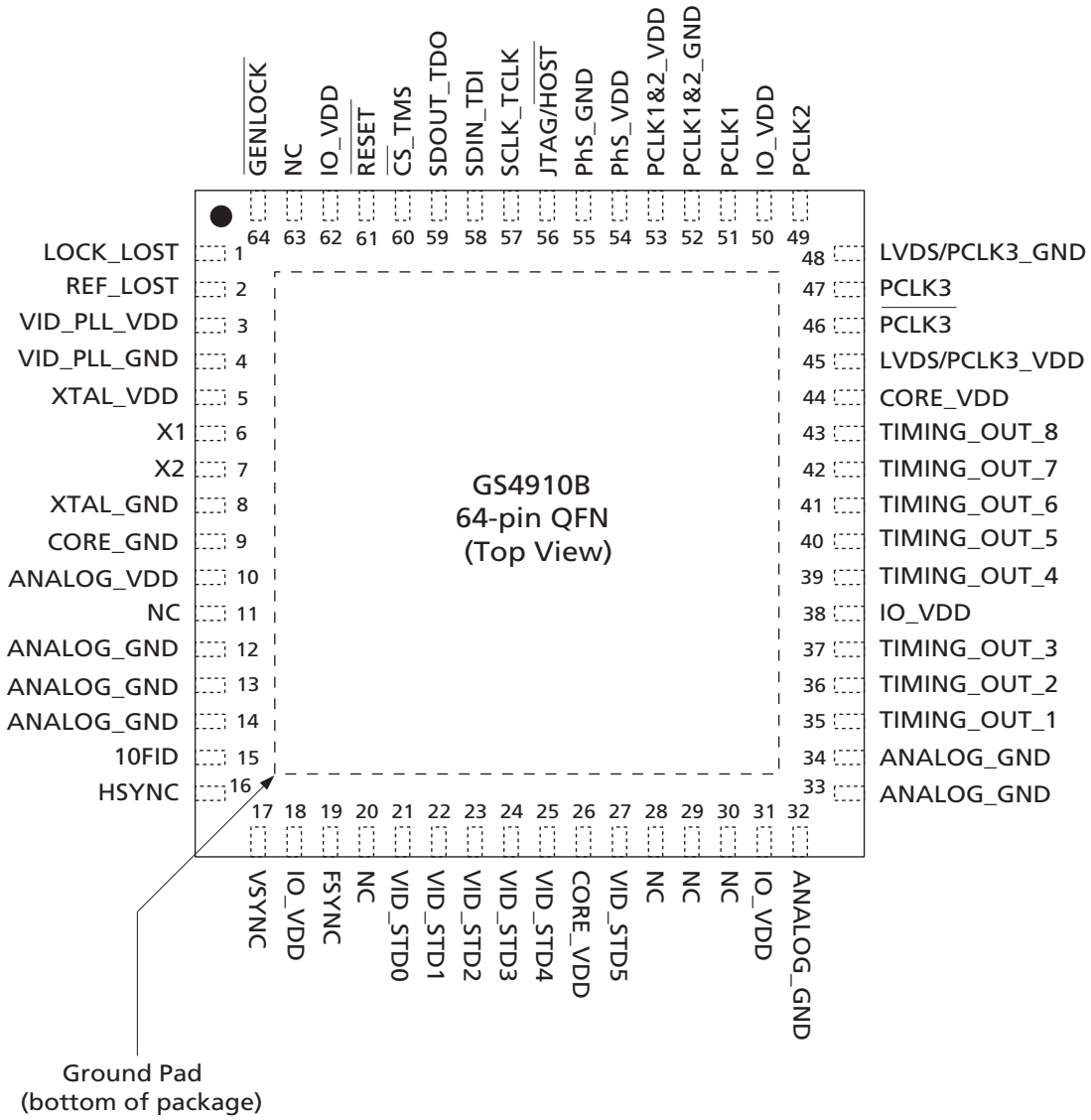


1.2 GS4910B Pin Assignment



1.3 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	LOCK_LOST	Non Synchronous	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be HIGH if the output is not genlocked to the input. The GS4911B/GS4910B monitors the output pixel/line counters, as well as the internal lock status from the genlock block and asserts LOCK_LOST HIGH if it is determined that the output is not genlocked to the input. This pin will be LOW if the device successfully genlocks the output clock and timing signals to the input reference. If LOCK_LOST is LOW, the reference timing generator outputs will be phase locked to the detected reference signal, producing an output in accordance with the video standard selected by the VID_STD[5:0] pins.
2	REF_LOST	Non Synchronous	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. This pin will be HIGH if: • No input reference signal is applied to the device; or • The input reference applied does not meet the minimum/maximum timing requirements described in Section 3.5.2 on page 46. This pin will be LOW otherwise. If the reference signal is removed when the device is in Genlock mode, REF_LOST will go HIGH and the GS4911B/GS4910B will enter Freeze mode (see Section 3.2.1.2 on page 41).
3	VID_PLL_VDD	–	Power Supply	Most positive power supply connection for the video clock synthesis internal block. Connect to +1.8V DC.
4	VID_PLL_GND	–	Power Supply	Ground connection for the video clock synthesis internal block. Connect to GND.
5	XTAL_VDD	–	Power Supply	Most positive power supply connection for the crystal buffer. Connect to either +1.8V DC or +3.3V DC. NOTE: Connect to +3.3V for minimum output PCLK jitter.
6	X1	Non Synchronous	Input	ANALOG SIGNAL INPUT Connect to a 27MHz crystal or a 27MHz external clock source. See Figure 1-1.
7	X2	Non Synchronous	Output	ANALOG SIGNAL OUTPUT Connect to a 27MHz crystal, or leave this pin open circuit if an external clock source is applied to pin 6. See Figure 1-1.
8	XTAL_GND	–	Power Supply	Ground connection for the crystal buffer. Connect to GND.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
9	CORE_GND	–	Power Supply	Ground connection for core and I/O. Solder to the ground plane of the application board. NOTE: The CORE_GND pin should be soldered to the same main ground plane as the exposed ground pad on the bottom of the device.
10	ANALOG_VDD	–	Power Supply	Most positive power supply connection for the analog input block. Connect to +1.8V DC.
11, 20, 63	NC	–	–	Do not connect.
12	ANALOG_GND	–	Power Supply	Ground connection for the analog input block. Connect to GND.
13	AUD_PLL_GND (GS4911B only)	–	Power Supply	Ground connection for the audio clock synthesis internal block. Connect to GND.
	ANALOG_GND (GS4910B only)	–	Power Supply	Ground connection for the analog input block. Connect to GND.
14	AUD_PLL_VDD (GS4911B only)	–	Power Supply	Most positive power supply connection for the audio clock synthesis internal block. Connect to +1.8V DC.
	ANALOG_GND (GS4910B only)	–	Power Supply	Ground connection for the analog input block. Connect to GND.
15	10FID	Non Synchronous	Input	REFERENCE SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. The 10FID external reference signal is applied to this pin by the application layer. 10FID defines the field in which the video and audio clock phase relationship is defined according to SMPTE 318-M. It is also used to define a 3:2 video cadence. NOTE: If the input reference format does not include a 10 Field ID signal, this pin should be held LOW. See Section 3.4.2 on page 44.
16	HSYNC	Non Synchronous	Input	REFERENCE SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. The HSYNC external reference signal is applied to this pin by the application layer. When the GS4911B/GS4910B is operating in Genlock mode, the device senses the polarity of the HSYNC input automatically, and references to the leading edge. If the user wishes to select one of the pre-programmed video and/or timing output signals provided by the device, then this signal must adhere to one of the 36 defined video or 16 different graphics display standards supported by the device. In this mode of operation, the HSYNC input provides a horizontal scanning reference signal. The HSYNC signal may have analog timing, such as from a sync separator, or may be digital such as from an SDI deserializer. Section 1.4 on page 20 describes the 36 video formats and 16 graphic formats recognized by the GS4911B/GS4910B.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
17	VSYNC	Non Synchronous	Input	REFERENCE SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. The VSYNC external reference signal is applied to this pin by the application layer. When the GS4911B/GS4910B is operating in Genlock mode, the device senses the polarity of the VSYNC input automatically, and references to the leading edge. If the user wishes to select one of the pre-programmed video and/or timing output signals provided by the device, then this signal must adhere to one of the 36 defined video or 16 different graphics display standards supported by the device. In this mode of operation, the VSYNC input provides a vertical scanning reference signal. The VSYNC signal may have analog timing, such as from a sync separator, or may be digital such as from an SDI deserializer. Section 1.4 on page 20 describes the 36 video formats and 16 graphic formats recognized by the GS4911B/GS4910B.
18, 31, 38, 50, 62	IO_VDD	–	Power Supply	Most positive power supply connection for the digital I/O signals. Connect to either +1.8V DC or +3.3V DC. NOTE: All five IO_VDD pins must be powered by the same voltage.
19	FSYNC	Non Synchronous	Input	REFERENCE SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. The FSYNC external reference signal is applied to this pin by the application layer. The first field is defined as the field in which the first broad pulse (also known as serration) is in the first half of a line. The FSYNC signal should be set HIGH during the first field for sync-based references. If the user wishes to select one of the pre-programmed video and/or timing output signals provided by the device, then this signal must adhere to one of the 36 defined video or 16 different graphics display standards supported by the device. In this mode of operation, the FSYNC input provides an odd/even field input reference. The FSYNC signal may have analog timing, such as from a sync separator, or may be digital such as from an SDI deserializer. Section 1.4 on page 20 describes the 36 video formats and 16 graphic formats recognized by the GS4911B/GS4910B. For blanking-based references, the FSYNC signal should be set HIGH during the second field. NOTE: If the input reference format does not include an F sync signal, this pin should be held LOW.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
27, 25, 24, 23, 22, 21	VID_STD[5:0]	Non Synchronous	Input	CONTROL SIGNAL INPUTS Signal levels are LVCMOS/LVTTL compatible. Video Standard Select. Used to select the desired video/graphic display format for video clock and timing signal generation. 8 different video and 13 different graphic sample clocks, as well as 35 different video format and 13 different graphic format timing signal outputs may be selected using these pins. For details on the supported video standards and video clock frequency selection, please see Section 1.4 on page 20.
26, 44	CORE_VDD	–	Power Supply	Most positive power supply connection for the digital core. Connect to +1.8V DC.
28, 29, 30	ACLK1 ACLK2 ACLK3 (GS4911B only)	–	Output	CLOCK SIGNAL OUTPUTS Signal levels are LVCMOS/LVTTL compatible. Audio output clock signals. ACLK1, ACLK2, and ACLK3 present audio sample rate clock outputs to the application layer. By default, after system reset, the audio clock output pins of the device provide clock signals as follows: ACLK1 = 256fs ACLK2 = 64fs ACLK3 = fs, where fs is the fundamental sampling frequency. The fundamental sampling frequency is selected using ASR_SEL[2:0]. Additional sampling frequencies may be programmed in the host interface. It is also possible to select different division ratios for each of the audio clock outputs by programming designated registers in the host interface. Clock outputs of 512fs, 384fs, 256fs, 192fs, 128fs, 64fs, fs and z bit are selectable on a pin-by-pin basis. NOTE: ACLK1-3 will have a 50% duty cycle, unless fs is selected as 96kHz and the host interface is configured such that one of the three ACLK pins is set to output a clock signal at 192fs or 384fs. If this is the case, then a 512fs clock will have a 33% duty cycle. These signals will be high impedance when ASR_SEL[2:0] = 000b.
	NC (GS4910B only)	–	–	Do not connect.
32, 33, 34	ASR_SEL[2:0] (GS4911B only)	Non Synchronous	Input	CONTROL SIGNAL INPUTS Signal levels are LVCMOS/LVTTL compatible. Audio Sample Rate Select. Used to select the fundamental sampling frequency, fs, of the audio clock outputs. See Table 3-7. When ASR_SEL[2:0] = 000b, audio clock generation will be disabled and the ACLK1 to ACLK3 pins will be high impedance. In this case, AUD_PLL_VDD (pin 14) may be connected to GND to minimize noise and power consumption.
	ANALOG_GND (GS4910B only)	–	Power Supply	Ground connection for the analog input block. Connect to GND.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
35	TIMING_OUT_1	Synchronous with PCLK1 ~ PCLK3	Output	TIMING SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Selectable timing output. Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4911B only); USER_1~4. See Section 1.5 on page 26 for signal descriptions. NOTE: Default output is H Sync. The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low. This signal will be high impedance when VID_STD[5:0] = 00h.
36	TIMING_OUT_2	Synchronous with PCLK1 ~ PCLK3	Output	TIMING SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Selectable timing output. Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4911B only); USER_1~4. See Section 1.5 on page 26 for signal descriptions. NOTE: Default output is H blanking. The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low. This signal will be high impedance when VID_STD[5:0] = 00h.
37	TIMING_OUT_3	Synchronous with PCLK1 ~ PCLK3	Output	TIMING SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Selectable timing output. Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4911B only); USER_1~4. See Section 1.5 on page 26 for signal descriptions. NOTE: Default output is V Sync. The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low. This signal will be high impedance when VID_STD[5:0] = 00h.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
39	TIMING_OUT_4	Synchronous with PCLK1 ~ PCLK3	Output	TIMING SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Selectable timing output. Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4911B only); USER_1~4. See Section 1.5 on page 26 for signal descriptions. NOTE: Default output is V blanking. The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low. This signal will be high impedance when VID_STD[5:0] = 00h.
40	TIMING_OUT_5	Synchronous with PCLK1 ~ PCLK3	Output	TIMING SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Selectable timing output. Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4911B only); USER_1~4. See Section 1.5 on page 26 for signal descriptions. NOTE: Default output is F Sync. The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low. This signal will be high impedance when VID_STD[5:0] = 00h.
41	TIMING_OUT_6	Synchronous with PCLK1 ~ PCLK3	Output	TIMING SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Selectable timing output. Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4911B only); USER_1~4. See Section 1.5 on page 26 for signal descriptions. NOTE: Default output is F digital. The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low. This signal will be high impedance when VID_STD[5:0] = 00h.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
42	TIMING_OUT_7	Synchronous with PCLK1 ~ PCLK3	Output	TIMING SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Selectable timing output. Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4911B only); USER_1~4. See Section 1.5 on page 26 for signal descriptions. NOTE: Default output is 10 Field ID (10FID). The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low. This signal will be high impedance when VID_STD[5:0] = 00h.
43	TIMING_OUT_8	Synchronous with PCLK1 ~ PCLK3	Output	TIMING SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Selectable timing output. Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4911B only); USER_1~4. See Section 1.5 on page 26 for signal descriptions. NOTE: Default output is Display Enable (DE). The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low. This signal will be high impedance when VID_STD[5:0] = 00h.
45	LVDS/PCLK3_VDD	–	Power Supply	Most positive power supply connection for PCLK3 output circuitry and LVDS driver. Connect to +1.8V DC.
46, 47	$\overline{\text{PCLK3}}$, PCLK3	–	Output	CLOCK SIGNAL OUTPUTS Signal levels are LVDS compatible. Differential video clock output signal. PCLK3/$\overline{\text{PCLK3}}$ present a differential video sample rate clock output to the application layer. By default, after system reset, this output will operate at the fundamental frequency determined by the setting of the VID_STD[5:0] pins. It is possible to define other non-standard fundamental clock rates using the host interface. It is also possible to select different division ratios for the PCLK3/$\overline{\text{PCLK3}}$ outputs by programming designated registers in the host interface. A clock output of the fundamental rate, fundamental rate ÷2, or fundamental rate ÷4 may be selected. The PCLK3/$\overline{\text{PCLK3}}$ outputs will be high impedance when VID_STD[5:0] = 00h.
48	LVDS/PCLK3_GND	–	Power Supply	Ground connection for PCLK3 output circuitry and LVDS driver. Connect to GND.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
49	PCLK2	–	Output	CLOCK SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Video clock output signal. PCLK2 presents a video sample rate clock output to the application layer. By default, after system reset, the PCLK2 output pin will operate at the fundamental frequency determined by the setting of the VID_STD[5:0] pins. It is possible to define other non-standard fundamental clock rates using the host interface. It is also possible to select different division ratios for the PCLK2 output by programming designated registers in the host interface. A clock output of the fundamental rate, fundamental rate ÷2, or fundamental rate ÷4 may be selected. By setting designated registers in the host interface, the current drive capability of this pin may be set high or low. By default, the current drive will be low. It must be set high if the clock rate is greater than 100MHz. The PCLK2 output will be held LOW when VID_STD[5:0] = 00h.
51	PCLK1	–	Output	CLOCK SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Video clock output signal. PCLK1 presents a video sample rate clock output to the application layer. By default, after system reset, the PCLK1 output pin will operate at the fundamental frequency determined by the setting of the VID_STD[5:0] pins. It is possible to define other non-standard fundamental clock rates using the host interface. It is also possible to select different division ratios for the PCLK1 output by programming designated registers in the host interface. A clock output of the fundamental rate, fundamental rate ÷2, or fundamental rate ÷4 may be selected. By setting designated registers in the host interface, the current drive capability of this pin may be set high or low. By default, the current drive will be low. It must be set high if the clock rate is greater than 100MHz. The PCLK1 output will be held LOW when VID_STD[5:0] = 00h.
52	PCLK1&2_GND	–	Power Supply	Ground connection for PCLK1&2 circuitry. Connect to GND.
53	PCLK1&2_VDD	–	Power Supply	Most positive power supply connection for PCLK1&2 circuitry. Connect to +1.8V DC.
54	PhS_VDD	–	Power Supply	Most positive power supply connection for the video clock phase shift internal block. Connect to +1.8V DC.
55	PhS_GND	–	Power Supply	Ground connection for the video clock phase shift internal block. Connect to GND.

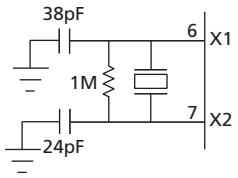
Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
56	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{\text{CS}}$_TMS, SCLK_TCLK, SDOUT_TDO, and SDIN_TDI are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SCLK_TCLK, SDOUT_TDO, and SDIN_TDI are configured as GSPI pins for normal host interface operation.
57	SCLK_TCLK	Non Synchronous	Input	SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Clock / Test Clock. All JTAG / Host Interface address and data are shifted into/out of the device synchronously with this clock. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): SCLK_TCLK operates as the host interface serial data clock, SCLK. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): SCLK_TCLK operates as the JTAG test clock, TCLK.
58	SDIN_TDI	Synchronous with SCLK_TCLK	Input	SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Input / Test Data Input. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): SDIN_TDI operates as the JTAG test data input, TDI.
59	SDOUT_TDO	Synchronous with SCLK_TCLK	Output	SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Output / Test Data Output. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): SDOUT_TDO operates as the JTAG test data output, TDO.
60	$\overline{\text{CS}}$_TMS	Synchronous with SCLK_TCLK	Input	SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip Select / Test Mode Select. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): $\overline{\text{CS}}$_TMS operates as the host interface chip select, $\overline{\text{CS}}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): $\overline{\text{CS}}$_TMS operates as the JTAG test mode select, TMS, and is active HIGH.

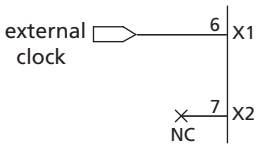
Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
61	$\overline{\text{RESET}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to their default settings or to reset the JTAG test sequence. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): When asserted LOW, all host registers and functional blocks will be set to their default conditions. All input and output signals will become high impedance, except PCLK1 and PCLK2, which will be set LOW. When set HIGH, normal operation of the device will resume. The user must hold this pin LOW during power-up and for a minimum of 500 uS after the last supply has reached its operating voltage. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): When asserted LOW, all host registers and functional blocks will be set to their default conditions and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence will resume.
64	$\overline{\text{GENLOCK}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Selects Genlock mode or Free Run mode. When this pin is set LOW and the device has successfully genlocked the output to the input reference, the device will enter Genlock mode. The video clock and timing outputs will be frequency and phase locked to the detected reference signal. When this pin is set HIGH, the video clock and the reference-timing generator will free-run. By default, the GS4911B's audio clocks will be genlocked to the output video clock regardless of the setting of this pin. NOTE: The user must apply a reference to the input of the device prior to setting $\overline{\text{GENLOCK}}$ = LOW. If the $\overline{\text{GENLOCK}}$ pin is set LOW and no reference signal is present, the generated clock and timing outputs of the device may correspond to the internal default settings of the chip until a reference is applied.
–	Ground Pad	–	–	Ground pad on bottom of package must be soldered to main ground plane of PCB.

External Crystal Connection



External Clock Source Connection



Notes:

1. Capacitor values listed represent the total capacitance, including discrete capacitance and parasitic board capacitance.

2. X1 serves as an input, which may alternatively accept a 27MHz clock source. To accomodate this, mismatched capacitor values are recommended.

Figure 1-1: XTAL1 and XTAL2 Reference Circuits

1.4 Pre-Programmed Recognized Video and Graphics Standards

Table 1-2 describes the video and graphics standards automatically recognized by the GS4911B/GS4910B. Any one of the 36 different video formats and 16 different graphic display formats listed below can be applied to the GS4911B/GS4910B and automatically detected by the reference format detector. Moreover, each format, with the exception of VID_STD[5:0] = 2, 52, 53, or 54, is available for output on the timing output pins by setting the VID_STD[5:0] pins.

In addition to the pre-programmed video standards listed in Table 1-2, custom output timing signals may be generated by the GS4911B/GS4910B. The custom timing parameters are programmed in the host interface when VID_STD[5:0] is set to 62 (see Section 3.10 on page 74).

Setting VID_STD[5:0] to 63 will cause the device to produce an output format with identical timing to the detected input reference.

If desired, the external VID_STD[5:0] pins may be ignored by setting bit 1 of the Video_Control register, and the video standard may instead be selected via the VID_STD[5:0] register of the host interface (see Section 3.12.3 on page 79). Although the external VID_STD[5:0] pins will be ignored in this case, they should not be left floating.

Table 1-2: Recognized Video and Graphics Standards

VID_STD [5:0]	System Nomenclature	Video PCLK Frequency (MHz)	PCLKS / Total Line	Total Lines / Frame	PCLKS / Active Line	H Sync Width (Clocks)	H Sync Polarity	V Sync Width (Lines)	V Sync Polarity	Active Lines / Frame	Scan Format Standard
0	PCLK1&2 =LOW. PCLK3/$\overline{\text{PCLK3}}$ = High Impedance	–	–	–	–	–	–	–	–	–	–
1	4fsc 525 / 2:1 interlace	14.32	910	525	768	67	negative	3	negative	486	SMPTE 244M
2*	Composite PAL 625 / 2:1 interlace / 25	–	–	625	–	–	negative	2.5	negative	576	–
3	601 525 / 2:1 interlace	27	1716	525	1440	127	negative	3	negative	486	SMPTE 125M/267M
4‡	601 625 / 2:1 interlace	27	1728	625	1440	127	negative	2.5	negative	576	ITU-R BT.601-5
5	601 – 18MHz 525 / 2:1 interlace	36	2288	525	1920	169	negative	3	negative	486	SMPTE 267M
6‡	601 – 18 MHz 625 / 2:1 interlace	36	2304	625	1920	169	negative	2.5	negative	576	ITU-R BT.601-5
7	720x486/59.94/2:1 interlace	54	3432	525	2880	252	negative	3	negative	486	SMPTE RP174 / SMPTE 347M
8‡	720x576/50/2:1 interlace	54	3456	625	2880	252	negative	2.5	negative	576	ITU-R BT.799 / SMPTE 347M
9	720x483/59.94/1:1 progressive	54	1716	525	1440	127	negative	6	negative	483	SMPTE 293M / SMPTE 347M
10	720x576/50/1:1 progressive	54	1728	625	1440	127	negative	5	negative	576	ITU-R BT.1358 / SMPTE 347M
11	1280x720/60/1:1 progressive	74.25	1650	750	1280	80	tri	5	negative	720	SMPTE 296M
12	1280x720/59.94/1:1 progressive	74.175	1650	750	1280	80	tri	5	negative	720	SMPTE 296M

Table 1-2: Recognized Video and Graphics Standards (Continued)

VID_STD [5:0]	System Nomenclature	Video PCLK Frequency (MHz)	PCLKS / Total Line	Total Lines / Frame	PCLKS / Active Line	H Sync Width (Clocks)	H Sync Polarity	V Sync Width (Lines)	V Sync Polarity	Active Lines / Frame	Scan Format Standard
13	1280/720/50/1:1 progressive	74.25	1980	750	1280	80	tri	5	negative	720	SMPTE 296M
14	1280x720/30/1:1 progressive	74.25	3300	750	1280	80	tri	5	negative	720	SMPTE 296M
15	1280x720/29.97/1:1 progressive	74.175	3300	750	1280	80	tri	5	negative	720	SMPTE 296M
16	1280x720/25/1:1 progressive	74.25	3960	750	1280	80	tri	5	negative	720	SMPTE 296M
17	1280x720/24/1:1 progressive	74.25	4125	750	1280	80	tri	5	negative	720	SMPTE 296M
18	1280x720/23.98/1:1 progressive	74.175	4125	750	1280	80	tri	5	negative	720	SMPTE 296M
19	1920x1035/60/2:1 interlace	74.25	2200	1125	1920	80	tri	5	negative	1035	SMPTE 260M
20	1920x1035/59.94/2:1 interlace	74.175	2200	1125	1920	80	tri	5	negative	1035	SMPTE 260M
21	1920x1080/60/1:1 progressive	148.5	2200	1125	1920	80	tri	5	negative	1080	SMPTE 274M
22	1920x1080/59.94/1:1 progressive	148.35	2200	1125	1920	80	tri	5	negative	1080	SMPTE 274M
23	1920x1080/50/1:1 progressive	148.5	2640	1125	1920	80	tri	5	negative	1080	SMPTE 274M
24	Reserved	–	–	–	–	–	–	–	–	–	–
25	1920x1080/60/2:1 interlace	74.25	2200	1125	1920	80	tri	5	negative	1080	SMPTE 274M
26	1920x1080/59.94/2:1 interlace	74.175	2200	1125	1920	80	tri	5	negative	1080	SMPTE 274M

Table 1-2: Recognized Video and Graphics Standards (Continued)

VID_STD [5:0]	System Nomenclature	Video PCLK Frequency (MHz)	PCLKS / Total Line	Total Lines / Frame	PCLKS / Active Line	H Sync Width (Clocks)	H Sync Polarity	V Sync Width (Lines)	V Sync Polarity	Active Lines / Frame	Scan Format Standard
27	1920x1080/50/2:1 interlace	74.25	2640	1125	1920	80	tri	5	negative	1080	SMPTE 274M
28	Reserved	–	–	–	–	–	–	–	–	–	–
29	1920x1080/30/1:1 progressive	74.25	2200	1125	1920	80	tri	5	negative	1080	SMPTE 274M
30	1920x1080/30/PsF	74.25	2200	1125	1920	80	tri	5	negative	1080	SMPTE RP 211
31	1920x1080/29.97/1:1 progressive	74.175	2200	1125	1920	80	tri	5	negative	1080	SMPTE 274M
32	1920x1080/29.97/PsF	74.175	2200	1125	1920	80	tri	5	negative	1080	SMPTE RP 211
33	1920x1080/25/1:1 progressive	74.25	2640	1125	1920	80	tri	5	negative	1080	SMPTE 274M
34	1920x1080/25/PsF	74.25	2640	1125	1920	80	tri	5	negative	1080	SMPTE RP 211
35	1920x1080/24/1:1 progressive	74.25	2750	1125	1920	80	tri	5	negative	1080	SMPTE 274M
36	1920x1080/24/PsF	74.25	2750	1125	1920	80	tri	5	negative	1080	SMPTE RP 211
37	1920x1080/23.98/1:1 progressive	74.175	2750	1125	1920	80	tri	5	negative	1080	SMPTE 274M
38	1920x1080/23.98/PsF	74.175	2750	1125	1920	80	tri	5	negative	1080	SMPTE RP 211
39	640 x 480 VGA @ 60 Hz	25.2	800	525	640	96	negative	2	negative	480	IBM Standard
40	640 x 480 VGA @ 75 Hz	31.5	840	500	640	64	negative	3	negative	480	VESA VDMT75HZ
41	640 x 480 VGA @ 85 Hz	36	832	509	640	56	negative	3	negative	480	VESA VDMTPROP
42	800 x 600 SVGA @ 60 Hz	40.00	1056	628	800	128	positive	4	positive	600	VESA VG900602

Table 1-2: Recognized Video and Graphics Standards (Continued)

VID_STD [5:0]	System Nomenclature	Video PCLK Frequency (MHz)	PCLKS / Total Line	Total Lines / Frame	PCLKS / Active Line	H Sync Width (Clocks)	H Sync Polarity	V Sync Width (Lines)	V Sync Polarity	Active Lines / Frame	Scan Format Standard
43	800 x 600 SVGA @ 75 Hz	49.5	1056	625	800	80	positive	3	positive	600	VESA VDMT75HZ
44	800 x 600 SVGA @ 85 Hz	56.25	1048	631	800	64	positive	3	positive	600	VESA VDMTPROP
45	1024 x 768 XGA @ 60 Hz	65	1344	806	1024	136	negative	6	negative	768	VESA VG901101A
46	1024 x 768 XGA @ 75 Hz	78.75	1312	800	1024	96	positive	3	positive	768	VESA VDMT75HZ
47	1024 x 768 XGA @ 85 Hz	94.5	1376	808	1024	96	negative	3	positive	768	VESA VDMTPROP
48	1280 x 1024 SXGA @ 60 Hz	108.00	1688	1066	1280	112	positive	3	positive	1024	VESA VDMTREV
49	1280 x 1024 SXGA @ 75 Hz	135.00	1688	1066	1280	144	negative	3	positive	1024	VESA VDMT75HZ
50	1280 x 1024 SXGA @ 85 Hz	157.5	1728	1072	1280	160	negative	3	positive	1024	VESA VDMTPROP
51†	1600 x 1200 UXGA @ 60 Hz	162	2160	1250	1600	192	negative	3	positive	1200	VESA VDMTPROP
52*	1600 x 1200 UXGA @ 75 Hz	–	–	1250	–	–	negative	3	positive	1200	–
53*	1600 x 1200 UXGA @ 85 Hz	–	–	1250	–	–	negative	3	positive	1200	–
54*	2048 x 1536 QXGA @ 60 Hz	–	–	1589	–	–	negative	3	positive	1536	–
55 - 61	Reserved	–	–	–	–	–	–	–	–	–	–
62	Custom format only (Section 3.10 on page 74)	–	–	–	–	–	–	–	–	–	–

Table 1-2: Recognized Video and Graphics Standards (Continued)

VID_STD [5:0]	System Nomenclature	Video PCLK Frequency (MHz)	PCLKS / Total Line	Total Lines / Frame	PCLKS / Active Line	H Sync Width (Clocks)	H Sync Polarity	V Sync Width (Lines)	V Sync Polarity	Active Lines / Frame	Scan Format Standard
63	Automatic Output Standard follows Input Standard	–	–	–	–	–	–	–	–	–	–

* VID_STD[5:0] = 2, 52, 53, and 54 are recognized as input references only. To generate clock and timing signals for these standards use the device's custom format capability.

† The LOCK_LOST output signal will be unstable when attempting to genlock to an input reference corresponding to VID_STD[5:0] = 51, although the device does achieve lock. To correct this, the user can program register address 27h = 38d.

‡ When VID_STD = 4, 6, or 8, the Vblanking output pulse width is 2 lines too long for field 1 and 1 line too short for field 2 when compared to the digital timing defined in ITU-R BT.656 and ITU-R BT.799.

NOTE: 1080i/60 to VGA/60 is not a valid locking option.