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Key Features

- SMPTE ST 2081, ST 424, ST 292, and ST 259-C compliant

- Supports retiming data at rates of 125Mb/s, 270Mb/s, 1.485 and 1.485/1.001Gb/s, 2.97 and 2.97/1.001Gb/s, 5.94 and 5.94/1.001Gb/s

- Supports retiming of DVB-ASI signals

- Automatic or Manual Rate Selection

  - Detected rate indication in Auto Mode

- 4:1 input selector patented technology

- Option of two reclocked data outputs

- Four configurable GPIO pins with ability to output device status, including:

  - Lock Detect
  - Loss of Signal (LOS)
  - Low/High bit-rate indication for slew-rate control of SDI cable drivers

- On-chip 100Ω differential input and output termination

- Bypass support for rates up to 5940Mb/s

  - Manual Bypass function
  - Configurable automatic Bypass when not locked

- Option to use external reference or operate referenceless

- Cascading reference buffer supports multiple CDRs using a single reference source

- Input signal equalization and output signal de-emphasis to compensate for trace dielectric losses

- Single power supply operation at 1.8V

- 130mW typical power consumption (150mW with second output enabled)

- Pb-free and RoHS compliant

- Operating temperature range: -40°C to 85°C

Applications

- SMPTE ST 2081, SMPTE ST 424, SMPTE ST 292, SMPTE ST 259-C coaxial cable serial digital interfaces

- EN50083-9 DVB-ASI interfaces

- MADI standard

Description

The GS6152 is a low-power, multi-rate serial digital CDR designed to automatically recover the embedded clock from a digital video signal and re-time the incoming video data.

The GS6152 will recover the embedded clock signal and re-time the data from 6G UHD-SDI signals compliant with SMPTE ST 2081. In addition, it can also re-time SMPTE ST 259-C, SMPTE ST 292, SMPTE ST 424 or DVB-ASI compliant digital video signals as well as MADI audio streams.

The GS6152 features four high-speed differential signal inputs feeding a 4:1 input selector. Input termination is on-chip for seamless matching to 100Ω differential transmission lines. The input selector is a component of a video switching system with tightly constrained timing requirements.

The GS6152 includes programmable trace equalization to compensate for high-frequency losses associated with board-level interconnect.

Two CML outputs interface seamlessly to devices with a CML input reference between 1.2V and 2.5V.

Programmable output swing and de-emphasis provide flexibility in managing signal integrity of the output signals.
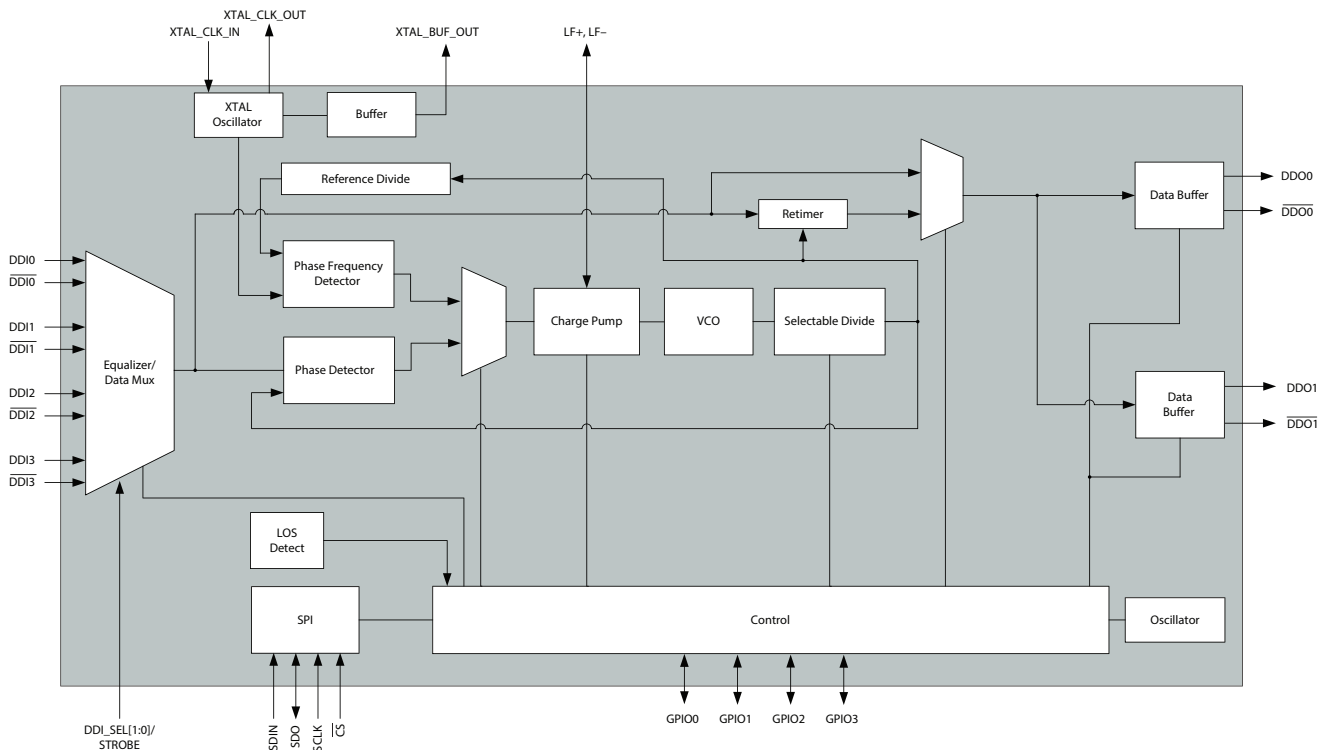
The GS6152 can operate in either automatic rate detection or manual rate selection mode. In auto mode the device will automatically detect and lock onto incoming data signals at any supported rate.

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The device can operate without an external 27MHz frequency reference. For applications which require rapid signal lock, an external 27MHz reference may be used to set the VCO frequency when not locked to the input signal. The presence of an external reference crystal is automatically detected by the device.

In systems that require passing of non-supported data rates, the GS6152 can be configured to either automatically or manually enter a bypass mode in order to pass the signal without reclocking.

A four-wire serial Gennum Serial Peripheral Interface (GSPI) facilitates configuration and status monitoring of the device. Multiple GS6152 devices can be daisy-chained together with a single 4-pin connection to the host system.

This device is Pb-free, and the encapsulation compound does not contain halogenated flame retardant. This component and all homogenous sub-components are RoHS compliant.

GS6152 Functional Block Diagram

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Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
2	027036	—	July 2015	Updated Table 2-2, Table 2-3, and Table 5-1. Updated to Final Data Sheet.
1	026419	—	July 2015	Updated Table 2-2, Table 2-3, Section 4.12 and Table 5-1.
0	024886	—	May 2015	New Document

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1. Pin Out

1.1 Pin Assignment
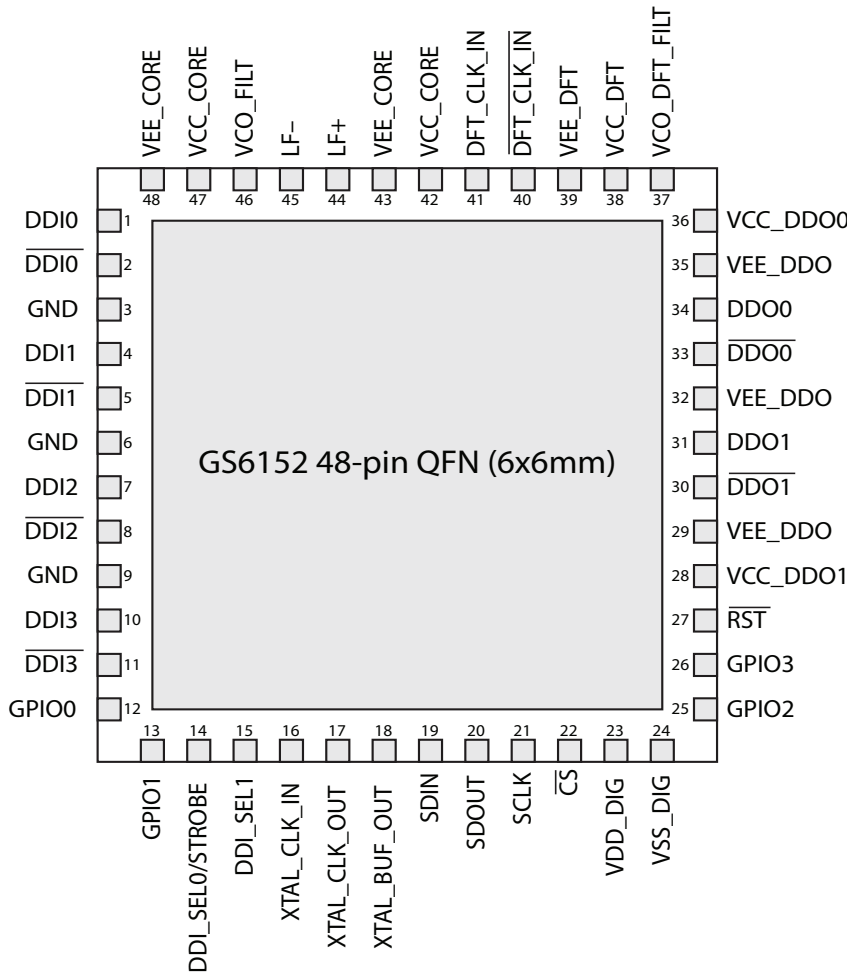
Figure 1-1: GS6152 Pin Out

1.2 Pin Descriptions

Table 1-1: GS6152 Pin Descriptions

Pin Number	Name	Type	Description
1, 2	DDI0, $\overline{\text{DDI0}}$	Input	Serial Digital Differential Input 0.
3, 6, 9	GND	Power	Input channel isolation. Connect to ground or leave unconnected.
4, 5	DDI1, $\overline{\text{DDI1}}$	Input	Serial Digital Differential Input 1.
7, 8	DDI2, $\overline{\text{DDI2}}$	Input	Serial Digital Differential Input 2.

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Table 1-1: GS6152 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
10, 11	DDI3, $\overline{DDI3}$	Input	Serial Digital Differential Input 3.
12	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Signal options are: LOS (output; default) LOCKED LBR_HBR RATE_DET0 RATE_DET1 RATE_DET2 LOCKED_125M LOCKED_270M LOCKED_1G485 LOCKED_2G97 LOCKED_5G94 RATE_CHANGE DDO0_DISABLE DDO1_DISABLE This pin is configured using the GPIO0_SELECT and GPIO0_IO_SELECT bits in the GPIO_CONTROL_REG_0 register.
13	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Signal options are: LOS LOCKED (output; default) LBR_HBR RATE_DET0 RATE_DET1 RATE_DET2 LOCKED_125M LOCKED_270M LOCKED_1G485 LOCKED_2G97 LOCKED_5G94 RATE_CHANGE DDO0_DISABLE DDO1_DISABLE This pin is configured using the GPIO1_SELECT and GPIO1_IO_SELECT bits in the GPIO_CONTROL_REG_0 register.
14, 15	DDI_SEL0/STROBE, DDI_SEL1	Logic Input	Input selection control. Used to select the high-speed input for processing through the device. Refer to Table 4-2 for details on input selection.
16	XTAL_CLK_IN	Input	Reference Crystal Pin/27MHz clock input. Connect to an external circuit as shown in Figure 6-1: GS6152 Typical Application Circuit or to a digital clock source (XTAL_BUF_OUT of another GS6152 or GS6151). Connect to ground if operating referenceless.
17	XTAL_CLK_OUT	Output	Reference Crystal Pin. Connect to a external circuit as shown in Figure 6-1: GS6152 Typical Application Circuit, or leave unconnected if XTAL_CLK_IN is driven by an external clock source or if XTAL_CLK_IN is connected to ground (referenceless).

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Table 1-1: GS6152 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
18	XTAL_BUF_OUT	Output	Buffered clock reference output. Leave unconnected if not used to drive 27MHz clock input of another device.
19	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Refer to 4.11 GSPI Host Interface for more details.
20	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Refer to 4.11 GSPI Host Interface for more details.
21	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Refer to 4.11 GSPI Host Interface for more details.
22	$\overline{CS}$	Digital Input	Chip select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Active-low input. Refer to 4.11 GSPI Host Interface for more details.
23	VDD_DIG	Power	Most positive power supply for the internal logic Connect to 1.8V.
24	VSS_DIG	Power	Most negative power supply for the internal logic Connect to ground.
25	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. Signal options are: LOS LOCKED LBR_HBR (output; default) RATE_DET0 RATE_DET1 RATE_DET2 LOCKED_125M LOCKED_270M LOCKED_1G485 LOCKED_2G97 LOCKED_5G94 RATE_CHANGE DDO0_DISABLE DDO1_DISABLE This pin is configured using the GPIO2_SELECT and GPIO2_IO_SELECT bits in the GPIO_CONTROL_REG_1 register.

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Table 1-1: GS6152 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
26	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Signal options are: LOS LOCKED LBR_HBR RATE_DET0 RATE_DET1 RATE_DET2 LOCKED_125M LOCKED_270M LOCKED_1G485 LOCKED_2G97 LOCKED_5G94 RATE_CHANGE DDO0_DISABLE DDO1_DISABLE (input; default) This pin is configured using the GPIO3_SELECT and GPIO3_IO_SELECT bits in the GPIO_CONTROL_REG_1 register.
27	$\overline{RST}$	Digital Input	Reset pin. If set LOW, all blocks set to default conditions and inputs/outputs set to high impedance. If HIGH, normal operation of the device resumes. By default, internally pulled HIGH.
28	VCC_DDO1	Power	Most positive power supply connection for the DDO1/$\overline{DDO1}$ output driver. Connect to any voltage between 1.2V and 2.5V.
29, 32, 35	VEE_DDO	Power	Most negative power supply connections for the output drivers. Connect to ground.
30, 31	$\overline{DDO1}$, DDO1	Output	Differential serial data output 1.
33, 34	$\overline{DDO0}$, DDO0	Output	Differential serial data output 0.
36	VCC_DDO0	Power	Most positive power supply connection for the DDO0/$\overline{DDO0}$ output driver. Connect to any voltage between 1.2V and 2.5V.
37	VCO_DFT_FILT	Power Decoupling	Connect through decoupling capacitor to ground.
38	VCC_DFT	Power	Connect to 1.8V.
39	VEE_DFT	Power	Connect to ground.
40, 41	$\overline{DFT\_CLK\_IN}$, DFT_CLK_IN	Input	Connect to high-speed differential clock (AC coupled internally). Leave unconnected if not using external DFT clock input feature.
42	VCC_CORE	Power	Most positive power supply connection to the analog core Connect to 1.8V.
43	VEE_CORE	Power	Most negative power supply connection to the analog core Connect to ground.
44	LF+	Passive	Connect to LF– through C_{LF} Refer to Figure 6-1: GS6152 Typical Application Circuit.
45	LF–	Passive	Connect to LF+ through C_{LF} Refer to Figure 6-1: GS6152 Typical Application Circuit.

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Table 1-1: GS6152 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
46	VCO_FILT	Power	External decoupling for the VCO. Refer to Figure 6-1: GS6152 Typical Application Circuit.
47	VCC_CORE	Power	Most positive power supply connection for the analog core Connect to 1.8V.
48	VEE_CORE	Power	Most negative power supply connection to the analog core Connect to ground.
—	Center Pad	Power	Ground pad on bottom of package. Connect to ground.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage – Core (VCC_CORE, VDD_DIG)	-0.5 to $+2.1V_{DC}$
Supply Voltage – Output Driver (VCC_DDO0, VCC_DDO1)	-0.5 to $+2.8V_{DC}$
Input ESD Voltage	4kV
Storage Temperature Range (T_S)	-50^oC to $+125^oC$
Operating Temperature Range (T_A)	-40^oC to $+85^oC$
Input Voltage Range (any input pin)	-0.3 to $(V_{CC\_CORE} + 0.3)V_{DC}$
Solder Reflow Temperature	$+260^oC$

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

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2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= −40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage – Core (VCC_CORE, VDD_DIG)	V_{CC_CORE}, V_{DD_DIG}	—	1.710	1.8	1.890	V	
Supply Voltage – Output Driver (VCC_DDO0, VCC_DDO1)	V_{CC_DDO0}, V_{CC_DDO1}	—	1.140	—	2.625	V	
Power	P_D	Data Rate 6G, DDO1/$\overline{DDO1}$ disabled	—	140	185	mW	1, 2
		Data Rate <6G, DDO1/$\overline{DDO1}$ disabled	—	130	170	mW	1, 2
		Data Rate 6G, Default Settings, DDO1/$\overline{DDO1}$ enabled	—	210	280	mW	3, 4
		Data Rate <6G, Default Settings, DDO1/$\overline{DDO1}$ enabled	—	190	255	mW	3, 4
		Maximum Supply and Power Settings with Diagnostic Features Off	—	280	360	mW	5
		Maximum Supply and Power Settings with Diagnostic Features On	—	575	630	mW	5
Power (Sleep operation)	P_{SLEEP}	—	—	20	35	mW	
Power (Standby operation)	$P_{STANDBY}$	—	—	80	110	mW	
Supply Current - Output Driver	I_{CC_DDO0}, I_{CC_DDO1}	Output Swing Register Setting = 0000$_b$	—	4.8	7	mA	6, 7
		Output Swing Register Setting= 0100$_b$	—	7.5	12	mA	6, 7
		Output Swing Register Setting = 1100$_b$	—	15	22	mA	6, 7

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Table 2-2: DC Electrical Characteristics (Continued)

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= −40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Current - Core	I_{CC_CORE}	Output De-emphasis Disabled Data Rate 6G	—	82	—	mA	8
		Output De-emphasis Disabled Data Rate 3G	—	74	—	mA	8
		Output De-emphasis Enabled Data Rate 6G	—	90	—	mA	8
		Output De-emphasis Enabled Data Rate 3G	—	81	—	mA	8
Supply Current - Digital	I_{CC_DIG}	External Crystal Referenced	—	7	12	mA	
Serial Input Termination		Differential	75	100	125	Ω	
Serial Output Termination		Differential	75	100	125	Ω	
Serial Input Common Mode Voltage	V_{CMIN}	—	0.9	—	V_{CC_CORE} - 50mV	V	9, 10
Input Voltage - Digital Pins ($\overline{CS}$, SDIN, CLK, GPIO[0:3])	V_{IH}	—	0.65* VDD_DIG	—	VDD_DIG	V	
	V_{IL}	—	0	—	0.35* VDD_DIG	V	
Output Voltage - Digital Pins (SDOUT, GPIO[0:3])	V_{OH}	I_{OH} = -2mA	VDD_DIG – 0.45	—	—	V	
	V_{OL}	I_{OL} = 2mA	—	—	0.45	V	

Notes:

1. Normal operation in referenceless mode, minimum output swing with de-emphasis disabled
2. VCC_DDO0/1 = 1.2V
3. The swing is default and de-emphasis is on
4. VCC_DDO0/1 = 1.8V
5. DDO0/$\overline{DDO0}$ and DDO1/$\overline{DDO1}$ set to maximum swing setting, external crystal reference used
6. Consumption per enabled DDO output
7. Refer to Table 4-4 for the exact register settings for each ΔV_{DDO} output swing listed
8. For two enabled outputs
9. Maximum input voltage level = 1.8V ± 5%
10. Up to a maximum swing of 800mV

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2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= −40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Data Rate (Bypass)	DR_{BYPASS}	Bypass mode enabled	3	—	5940	Mb/s	1
Input Sensitivity	ΔV_{SDI}	Differential	200	—	800	mV_{ppd}	
Output Voltage Swing	ΔV_{DDO}	Output Swing Register Setting = 0100$_b$	310	410	510	mV_{ppd}	2
		Output Swing Register Setting = 1100$_b$	600	800	1000	mV_{ppd}	2
Serial Input Jitter Tolerance	IJT	Square wave modulation	0.8	—	—	UI	
PLL Lock Time — Asynchronous	t_{ALOCK}	Referenceless	—	—	50	ms	3
		With External Reference (MADI enabled)	—	—	30	ms	3
		With External Reference (MADI disabled)	—	—	20	ms	3
PLL Lock Time — Synchronous	t_{SLOCK}	Referenceless	—	—	10	µs	3
		With External Reference	—	—	10	µs	3
Serial Data (DDO0 and DDO1) Output Rise And Fall Time	$t_{riseDDO}$	20% ~ 80% rising edge into 50Ω load	—	—	70	ps	4
	$t_{fallDDO}$	20% ~ 80% falling edge into 50Ω load	—	—	70	ps	4
Rise And Fall Time Mismatch (DDO0 and DDO1)	—	—	—	—	15	ps	4
Duty Cycle Distortion (DDO0 and DDO1)	—	—	—	—	5	%	
Serial Data Output Jitter Intrinsic	$t_{OJ(125Mb/s)}$	BW = Nominal PRN 2^{23} – 1 test pattern	—	0.02	0.03	UI_{P-P}	5, 6
	$t_{OJ(270Mb/s)}$		—	0.02	0.03	UI_{P-P}	5, 6
	$t_{OJ(1485Mb/s)}$		—	0.03	0.06	UI_{P-P}	5, 6
	$t_{OJ(2970Mb/s)}$		—	0.04	0.09	UI_{P-P}	5, 6
	$t_{OJ(5940Mb/s)}$		—	0.07	0.13	UI_{P-P}	5, 6
	$t_{OJ(BYPASS)}$		—	—	37	ps	5, 6

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Table 2-3: AC Electrical Characteristics (Continued)

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= −40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Loop Bandwidth	BW$_{LOOP(125Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	37	—	kHz	7
		PLL_LOOP_BANDWIDTH = 00010	—	74	—	kHz	7
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	148	—	kHz	7
		PLL_LOOP_BANDWIDTH = 01000	—	296	—	kHz	7
		PLL_LOOP_BANDWIDTH = 10000	—	590	—	kHz	7
	BW$_{LOOP(270Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	80	—	kHz	7
		PLL_LOOP_BANDWIDTH = 00010	—	160	—	kHz	7
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	320	—	kHz	7
		PLL_LOOP_BANDWIDTH = 01000	—	640	—	kHz	7
		PLL_LOOP_BANDWIDTH = 10000	—	1.28	—	MHz	7
	BW$_{LOOP(1485Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	438	—	kHz	7
		PLL_LOOP_BANDWIDTH = 00010	—	875	—	kHz	7
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	1.75	—	MHz	7
		PLL_LOOP_BANDWIDTH = 01000	—	3.5	—	MHz	7
		PLL_LOOP_BANDWIDTH = 10000	—	7	—	MHz	7
	BW$_{LOOP(2970Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	875	—	kHz	7
		PLL_LOOP_BANDWIDTH = 00010	—	1.75	—	MHz	7
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	3.5	—	MHz	7
		PLL_LOOP_BANDWIDTH = 01000	—	7.0	—	MHz	7
		PLL_LOOP_BANDWIDTH = 10000	—	14.0	—	MHz	7

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Table 2-3: AC Electrical Characteristics (Continued)

VCC_CORE, VDD_DIG = +1.8V ± 5%, T_A= −40ºC to +85ºC unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Loop Bandwidth	$BW_{LOOP(5940Mb/s)}$	PLL_LOOP_BANDWIDTH = 00001	—	1.75	—	MHz	7
		PLL_LOOP_BANDWIDTH = 00010	—	3.5	—	MHz	7
		PLL_LOOP_BANDWIDTH = 00100 (default)	—	7.0	—	MHz	7
		PLL_LOOP_BANDWIDTH = 01000	—	14.0	—	MHz	7
		PLL_LOOP_BANDWIDTH = 10000	—	28.0	—	MHz	7

Note:

1. Edge detection method for LOS detection should be used for data rates below 20Mb/s
2. Refer to Table 4-4 for the exact register settings for each ΔV_{DDO} output swing listed
3. PRBS23 pattern used for supported video rates
4. At HD, 3G, and 6G rates
5. Jitter measured using an oscilloscope according to SMPTE RP-184
6. Accumulated jitter measured peak to peak differential over 2000 hits
7. Test pattern used is clock pattern with 100% toggle rate

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3. Input/Output Circuits
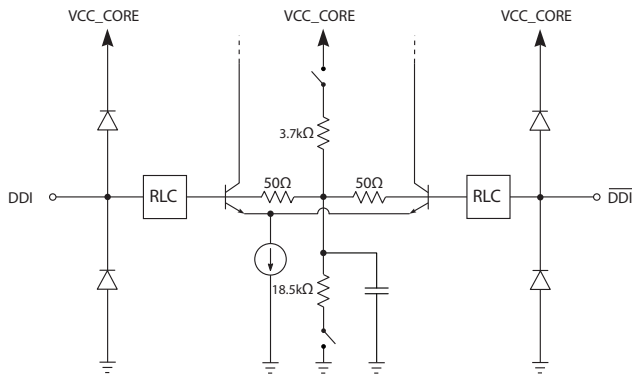
Figure 3-1: DDI0, $\overline{\text{DDI0}}$, DDI1, $\overline{\text{DDI1}}$, DDI2, $\overline{\text{DDI2}}$, DDI3, $\overline{\text{DDI3}}$ Serial Digital Differential Inputs
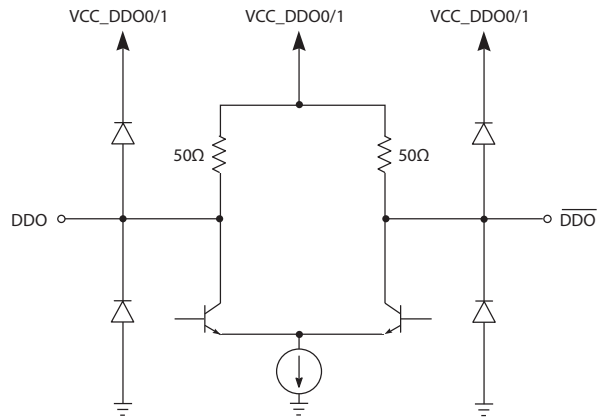
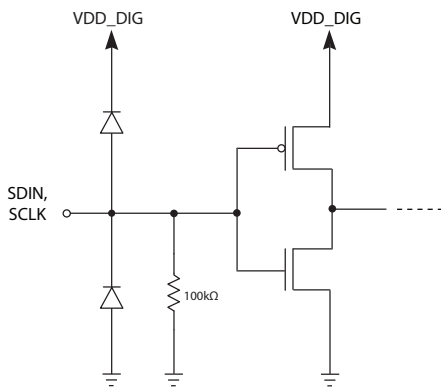**Figure 3-2: DDO0, $\overline{\text{DDO0}}$, DDO1, $\overline{\text{DDO1}}$ Serial Digital Differential Output**

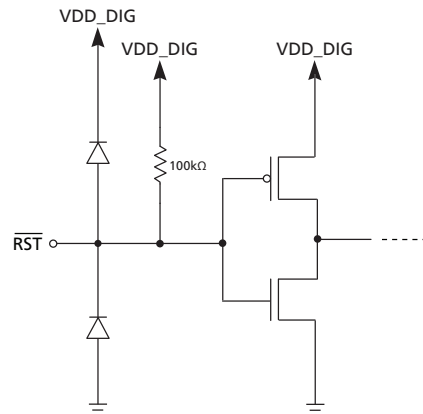
Figure 3-3: SDIN and SCLK
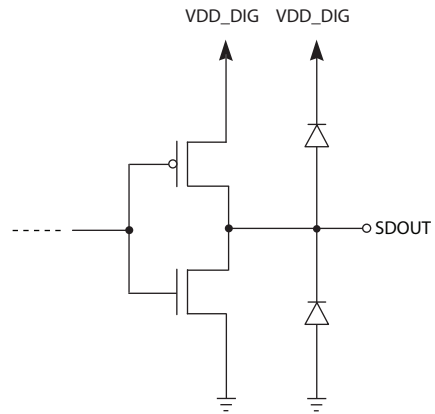
Figure 3-4: SDOUT

Table 3-1: $\overline{\text{CS}}$

Table 3-2: $\overline{\text{RST}}$

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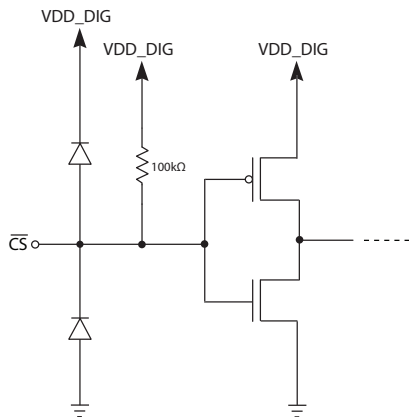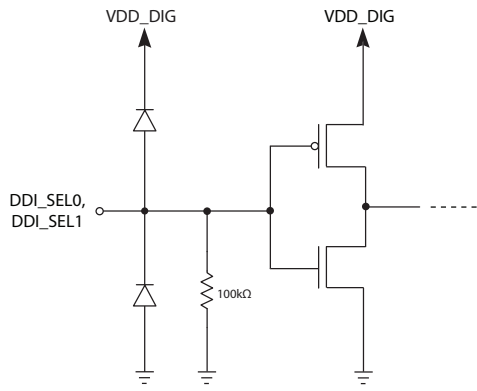
Figure 3-5: DDI_SEL0/STROBE and DDI_SEL1

Figure 3-6: XTAL_BUF_OUT

Note: GPIO Interface includes pins
GPIO0, GPIO1, GPIO2, and GPIO3
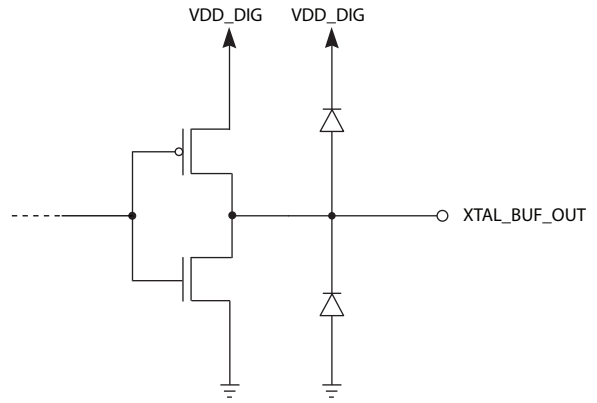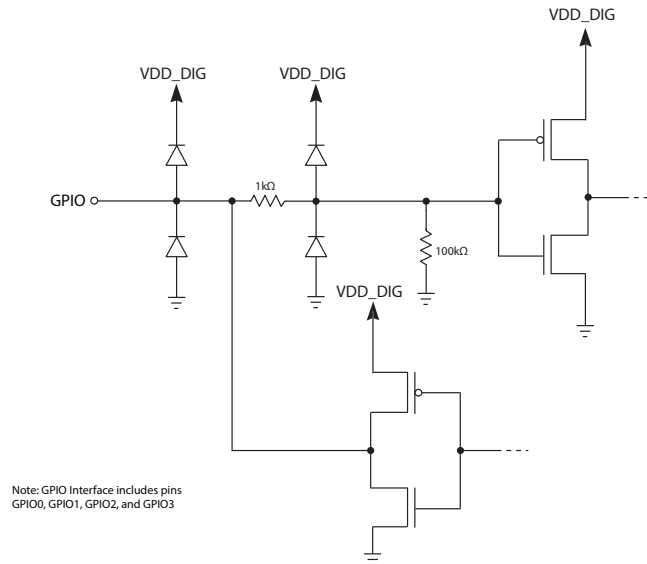
Figure 3-7: General Purpose Inputs/Outputs (GPIO)

Figure 3-8: XTAL_CLK_IN and XTAL_CLK_OUT

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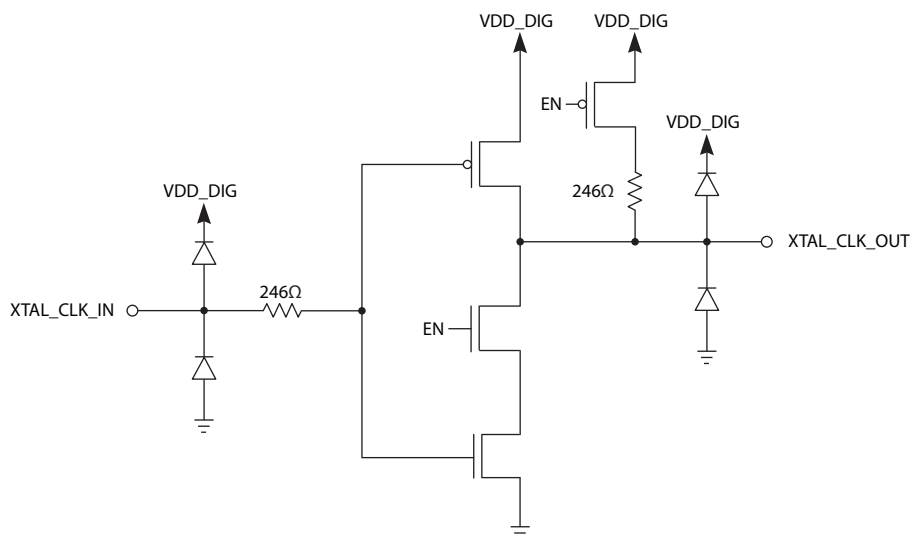
4. Detailed Description

The GS6152 is a multi-standard CDR for signals operating at the following data rates: 125Mb/s, 270Mb/s, 1.485Gb/s, 1.485/1.001Gb/s, 2.97Gb/s, 2.97/1.001Gb/s, 5.94Gb/s, and 5.94/1.001Gb/s.

4.1 Serial Data Inputs

The GS6152 features four 100Ω terminated differential input buffers.

A serial data input signal may be connected to any of the following input pin pairs of the device: DDI0/$\overline{\text{DDI0}}$, DDI1/$\overline{\text{DDI1}}$, DDI2/$\overline{\text{DDI2}}$, and DDI3/$\overline{\text{DDI3}}$.

By default, the self-biasing circuit at the input is enabled to allow AC coupling to upstream devices. To enable DC coupling of the inputs, the user must disable the self-biasing network by setting bits 4:4 through 7:7 to 0 in the register 7_h: DDI[0:3]_TRACE_EQ_DC_TERM_ENABLE.

In order to select DC coupling, please ensure that the output common mode of the upstream device is in range of the input common mode voltage range shown in Table 2-2.

The serial digital input buffer is capable of operating with any binary coded signal that meets the input signal level requirements defined below, with any data rate between 3Mb/s and 5.94Gb/s.

4.1.1 Input Trace Equalization

The GS6152 features adjustable trace equalization to compensate for PCB trace dielectric losses up to half the maximum supported data rate, or 3GHz.

Table 4-1: Equalization Settings

Data Rate	Trace Loss	Settings
2.97Gb/s and below	0-7dB of trace loss at 1.5GHz	LOW (default)
5.94Gb/s	0-10dB of trace loss at 3GHz	
2.97Gb/s and below	7-12dB of trace loss at 1.5GHz	HIGH
—	negligible trace loss	0dB or EQ_BYPASS

These settings are selected using the DDI0_TRACE_EQ_CONTROL, DDI1_TRACE_EQ_CONTROL, DDI2_TRACE_EQ_CONTROL and DDI3_TRACE_EQ_CONTROL bits in the INPUT_CONTROL_REG_0 register at address 5_h.

The default state of the device is input trace equalization on all inputs set to LOW.

If system jitter profile allows, it is recommended that the loop bandwidth is reduced to the minimum setting to maximize performance.

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4.1.2 Input Selection

The GS6152 incorporates a 4:1 input selector which allows the connection of four independent streams of video/data.

The selector is controllable in three separate ways:

1. The DDI_SEL0 and DDI_SEL1 pins can be used to select the input.

2. A GSPI accessible register can be used to select the input, with the state change occurring as soon as the register value changes.

3. A GSPI accessible register can be used to select the input, with a rising edge on the STROBE pin triggering a change to the next state.

Since these states are mutually exclusive, the DDI_SEL0 pin is shared with the STROBE function.

In the case of using the DDI_SEL0/STROBE and DDI_SEL1 pins (#1 above) or the STROBE pre-select method (#3 above), the input selector will switch within 1µs of the change of state on the corresponding pin(s). This strict timing requirement is not maintained when using GSPI register selection (#2 above).

Each of the device's four inputs is selected as shown in Table 4-2.

Table 4-2: Pin and Register Settings for Input Selection

Register Settings			Pin Settings		Differential High-speed Input Selected
INPUT_SELECTION_CONTROL 7_h[9:8]	DDI_SELECT 7_h[11]	DDI_SELECT 7_h[10]	DDI_SEL1	DDI_SEL0/ STROBE	
X0 (default)	X	X	LOW	LOW	DDI0, $\overline{DDI0}$
X0 (default)	X	X	LOW	HIGH	DDI1, $\overline{DDI1}$
X0 (default)	X	X	HIGH	LOW	DDI2, $\overline{DDI2}$
X0 (default)	X	X	HIGH	HIGH	DDI3, $\overline{DDI3}$
01	0	0	X	X	DDI0, $\overline{DDI0}$
01	0	1	X	X	DDI1, $\overline{DDI1}$
01	1	0	X	X	DDI2, $\overline{DDI2}$
01	1	1	X	X	DDI3, $\overline{DDI3}$
11	0	0	X	on LOW-to-HIGH transition	DDI0, $\overline{DDI0}$
11	0	1	X	on LOW-to-HIGH transition	DDI1, $\overline{DDI1}$
11	1	0	X	on LOW-to-HIGH transition	DDI2, $\overline{DDI2}$

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Table 4-2: Pin and Register Settings for Input Selection (Continued)

Register Settings			Pin Settings		Differential High-speed Input Selected
INPUT_SELECTION_CONTROL 7$_h$[9:8]	DDI_SELECT 7$_h$[11]	DDI_SELECT 7$_h$[10]	DDI_SEL1	DDI_SEL0/ STROBE	
11	1	1	X	on LOW-to-HIGH transition	DDI3, $\overline{DDI3}$

Note: 'X' indicates 'Do Not Care'

The DDI_SEL0/STROBE and DDI_SEL1 pins include internal pull-downs, which pulls the input voltage LOW if either pin is unconnected.

When using the STROBE pre-select method (#3 above), the pre-selected input buffer and trace EQ is powered up in advance of the STROBE pulse.

4.2 Reference Clock

The GS6152 can operate with or without an external frequency reference. For applications requiring rapid asynchronous locking, a 27MHz reference or crystal is required.

The PLL lock times for both referenceless and external crystal reference operation are given in Table 2-3: AC Electrical Characteristics.

If a reference is connected to the XTAL_CLK_IN pin or a crystal is connected to the XTAL_CLK_IN and XTAL_CLK_OUT pins of the device, it will automatically be used as the reference frequency for rapid asynchronous lock. If XTAL_CLK_IN is not connected to a crystal, XTAL_CLK_OUT must be left unconnected.

The XTAL_CLK_IN pin operates correctly when connected directly to the XTAL_BUF_OUT from another GS6152, or a 27MHz output of a different device.

4.3 Signal Monitoring

The GS6152 measures and reports the following signal status and quality monitoring parameters:

* Loss of Signal
* Lock Detection
* Rate Detection
* Low/High Bit Rate Detection

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4.3.1 Loss of Signal Detection

LOS (Loss of Signal) detection is an active HIGH output available to the application on any of the GPIO[3:0] multi-function status and control pins. It is selected for output using the GPIO[3:0]_IO_SELECT and GPIO[3:0]_SELECT bits accessible in the GPIO_CONTROL_REG_0 and GPIO_CONTROL_REG_1 registers. It is the default output of the GPIO0 pin.

LOS indicates when the serial digital signal selected by the input selector is invalid. This function is always active.

Two methods can be used to detect loss of signal: strength (default) and edge. Either method can be selected with LOS_DETECTION_METHOD bits of register PLL_CONTROL.

When strength detection is used as the method of LOS detection the corresponding GPIO pin will be HIGH (signal lost) when the input signal amplitude within a predefined window falls below the threshold set by the bits DDI[0:3]_LOS_THRESHOLD_CONTROL in the LOS_CONTROL_REG_1 and LOS_CONTROL_REG_2 registers. The LOS threshold hysteresis can be set by the LOS_HYSTERESIS bits in the LOS_CONTROL_REG_0 register at address F_h.

The corresponding GPIO pin will be LOW (signal present) when the input signal amplitude within a predefined window is above the defined threshold.

The method of strength detection is measurement of the average rectified differential voltage on the input pins. The strength detection method is therefore inherently dependent on the input signal's eye shape, particularly the rise/fall times of the input signal relative to the data rate. Additionally, the circuit has a lower bandwidth limit of operation (20Mb/s) below which it is recommended that the edge detection method is used. The absolute value of the threshold can be determined for any input swings according to Equation 4-1 below:

$$\mathrm{Threshold} = \frac{1.9\mathrm{mV} \times (\mathrm{DDI[0..3]\_LOS\_THRESHOLD\_CONTROL}) \times 53}{(\mathrm{DEVICE\_SPECIFIC\_LOS\_THRESHOLD})}$$

Equation 4-1

where DEVICE_SPECIFIC_LOS_THRESHOLD specifies the LOS threshold value for a 100mV input swing at SD-rate specific to each device. The other rates scale according to the fractional relationship given in Figure 4-1 and Figure 4-2 below.
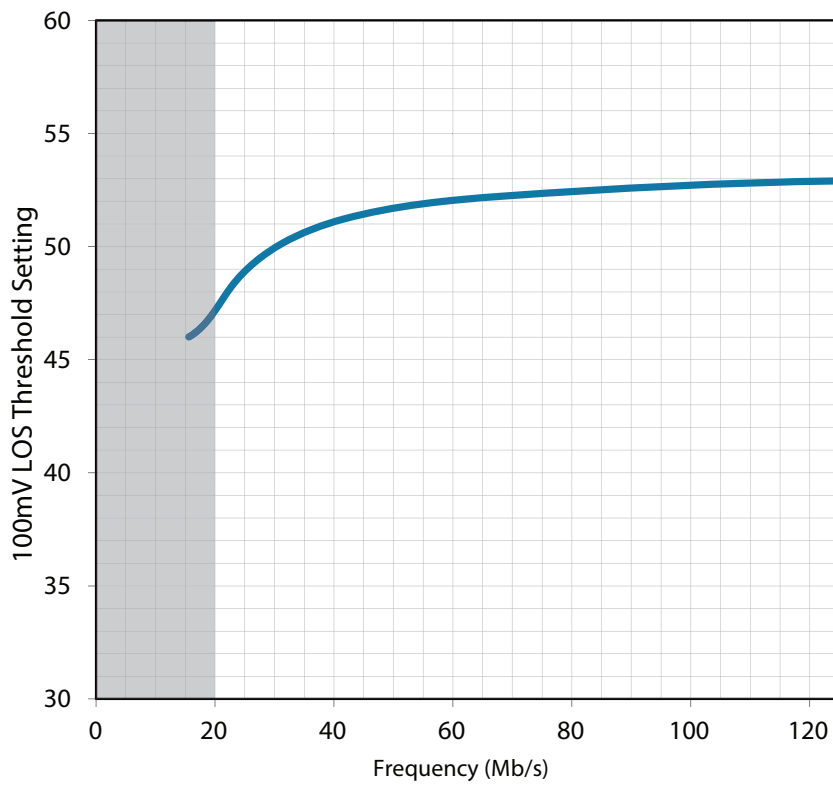
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Figure 4-1: LOS Threshold at 100mV Input Swing vs. Low Frequency Rates for a Nominal DEVICE_SPECIFIC_LOS_THRESHOLD of 53

Note: Edge detection method is recommended for signals in shaded areas.

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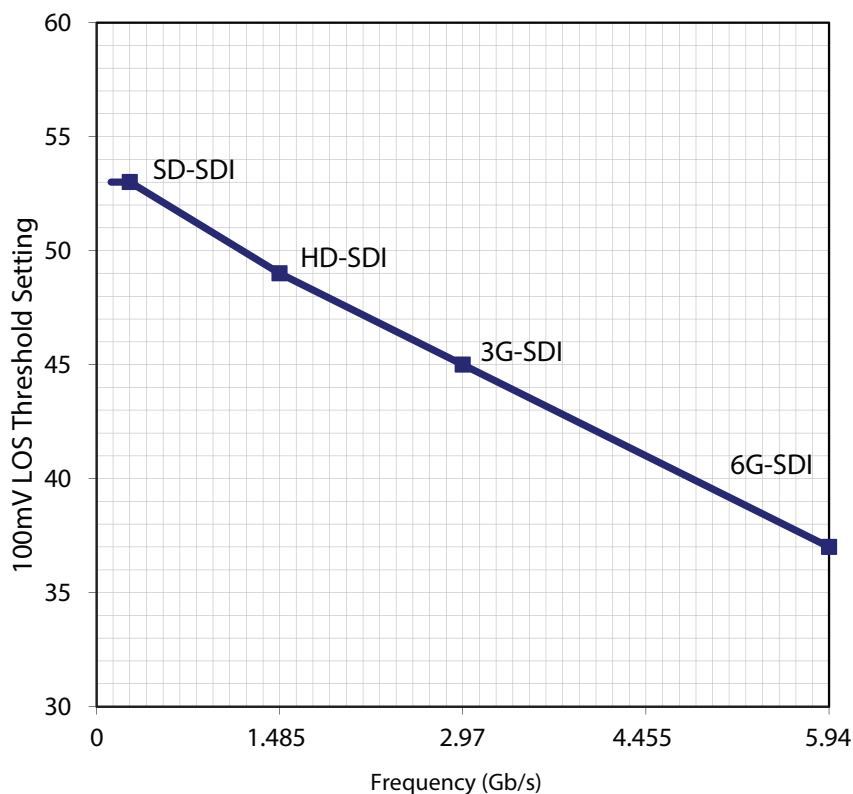Proprietary & Confidential

Figure 4-2: LOS Threshold at 100mV Input Swing vs. SDI Data Rates for a Nominal DEVICE_SPECIFIC_LOS_THRESHOLD of 53

Strength detection is unaffected by the Trace EQ settings in INPUT_CONTROL_REG_0.

When edge detection is used as the method of LOS detection the corresponding GPIO pin will be HIGH (signal lost) when no transitions are detected on the selected input. The corresponding GPIO pin will be LOW (signal present) when transitions are detected on the input. The LOS status is also available through the LOS bit in the PLL_STATUS register, and as a sticky status through the LOS_STICKY bit in the STICKY_STATUS register at address 50_h.

4.3.2 Lock Detection

The GS6152 lock detection circuitry outputs a LOCKED status signal which indicates that the CDR has achieved phase lock to the incoming data stream. The LOCKED signal is an active HIGH output available to the application on any of the GPIO[3:0] multi-function status and control pins. It is selected for output using the GPIO[3:0]_IO_SELECT and GPIO[3:0]_SELECT bits accessible in the GPIO_CONTROL_REG_0 and GPIO_CONTROL_REG_1 registers. By default, LOCKED is output on GPIO1.

The LOCKED status is available from the LOCKED bit in the PLL_STATUS register, and the LOCK_LOST_STICKY bit in the STICKY_STATUS register indicates whether lock has been lost since the bit was last cleared.

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4.3.2.1 Synchronous and Asynchronous Lock Time

Asynchronous lock time is defined as the time it takes the device to lock when a signal is first applied to the serial digital inputs, or when the signal rate changes.

The synchronous lock time is defined as the time it takes the device to lock to a signal which has been momentarily interrupted.

The asynchronous and synchronous lock times are defined in Table 2-3: AC Electrical Characteristics.

To qualify for synchronous lock time, the maximum interruption time of the signal is 10μs for a 270Mb/s signal. 1.485Gb/s, 2.97Gb/s, and 5.94Gb/s signals, as well as their f/1.001 components have a maximum interruption time of 6μs. The new signal, after interruption, must have the same frequency as the original signal but can have arbitrary phase.

4.3.3 Rate Detection

The GS6152 can be manually forced to lock to a specific supported data rate, or automatically search for and lock to supported rates. The selection between manual and automatic rate selection is through the FORCE_PLL_RATE and FORCE_PLL_RATE_ENABLE bits of the PLL_CONTROL register at address $4C_h$. By default the device is set to automatically search for supported SDI rates.

When set to automatically detect supported data rates, the device repeatedly cycles through each supported rate that is enabled through the RATE_ENABLE_5G94, RATE_ENABLE_2G97, RATE_ENABLE_1G485, RATE_ENABLE_270M and RATE_ENABLE_125M bits of the PLL_CONTROL register, until the device phase locks to one of the enabled rates. If lock is lost the rate search resumes, continuously testing for each rate in sequence until lock is regained.

The device reports the current data rate setting of the automatic rate search state machine through the DETECTED_RATE bits in the PLL_STATUS register at address $4F_h$. Each bit of DETECTED_RATE is also available to output through the GPIO pins, selected for output using the GPIO[3:0]_IO_SELECT and GPIO[3:0]_SELECT bits accessible in the GPIO_CONTROL_REG_0 register. The supported rates that the DETECTED_RATE bits can output are shown in Table 4-3 below.

Table 4-3: Automatic Rate Detection - Supported Data Rates

DETECTED_RATE	Data Rate
000	125Mb/s – MADI
001	270Mb/s – SD
010	1.485Gb/s – HD
011	2.97Gb/s – 3G
100	5.94Gb/s – 6G

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4.3.4 Low/High Bit Rate Detection for Slew Rate Control

A status output named LBR_HBR is provided to control the slew rate selection input of a downstream SDI cable driver. It can be connected to the SD_EN input of drivers such as the GS6080 or GS6081 using the Semtech recommended application circuit.

When this signal is HIGH, the data rate is 270Mb/s (SD) or 125Mb/s (MADI). This signal is LOW for all other supported data rates, and when the GS6152 is operating in Bypass Mode or any time the device is not locked.

The LBR_HBR output signal is available to the application on any of the GPIO[3:0] multifunction status and control pins. It is selected for output using the GPIO[3:0]_IO_SELECT and GPIO[3:0]_SELECT bits accessible in the GPIO_CONTROL_REG_0 and GPIO_CONTROL_REG_1 registers. By default, LBR_HBR is output on GPIO2.

4.4 Low Power Modes

The device can be programmed via the GSPI to operate in two different low power modes. SLEEP mode has minimum power consumption at the expense of recovery time upon de-assertion of the FORCE_PWRDN_SLEEP bit. STANDBY mode has higher power consumption relative to SLEEP mode but minimizes time to return to operation on de-assertion of the FORCE_PWRDN_STANDBY bit. The features affected by each mode are outlined below.

SLEEP mode:

- LOS detection remains functional
- The GSPI remains functional
- The reference oscillator remains functional

STANDBY mode:

- LOS detection remains functional
- The GSPI remains functional
- The reference oscillator remains functional
- The VCO and PLL remains functional so as to minimize the lock time when a signal is detected
- The rate detector remains set to the last valid data rate. On detection of a signal, the last valid rate is tested first by the rate detect state machine

The device can be programmed to automatically enter into SLEEP or STANDBY mode when LOS is asserted by programming the AUTO_PWRDN_DISABLE bit in the PWRDN_CONTROL register at address 17_h. The AUTO_PWRDN_MODE bit in the same register selects which mode, SLEEP or STANDBY, is entered into upon assertion of LOS.

The device also features a power-save feature that reduces power when the CDR is locked to HD, 3G or 6G rates. The HS_LOCKED_POWER_SAVE parameter of register PWR_CONTROL at address $D2_h$ can be set to 1 to enable this feature.

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4.5 Serial Data Output

The GS6152 has two current-mode differential output drivers, each capable of driving up to 930mV$_{pp}$ differential into an external 100Ω differential load.

The output drivers operate with any binary coded signal with supported data rates up to 5.94Gb/s. This is applicable to the serial data (DDO, $\overline{DDO}$, DDO1, $\overline{DDO1}$) outputs of the device.

4.5.1 Output Impedance

Each of the GS6152's output buffers include two on-chip, 50Ω termination resistors.

4.5.2 Output Signal Interface Levels

The serial digital outputs operate within specification with an output CML power supply of 1.2V to 2.5V.

4.5.3 Adjustable Output Swing

Through the GSPI, the output swing can be set in the range from approximately 230mV$_{ppd}$ to 930mV$_{ppd}$ in 45mV$_{ppd}$ increments, when the outputs are terminated with 50Ω loads. For the exact values, please see Table 4-4 below.

The output swing for each data rate is controlled using the bits in the DRIVER_CONTROL_REG_3, DRIVER_CONTROL_REG_4, DRIVER_CONTROL_REG_5, and DRIVER_CONTROL_REG_6 registers at addresses 1C$_h$ through 1F$_h$.

The device automatically adjusts the swing setting depending on the state of the device (i.e. detected rate, bypass mode, or mute). There are separate register controls for mute, bypass and each data rate.

Table 4-4: Serial Digital Output Swing Settings

Register Setting (See Note 1)	Min	Typ	Max	Units
0000$_b$	175	230	290	mV
0001$_b$	205	275	345	mV
0010$_b$	245	325	405	mV
0011$_b$ (default)	280	370	460	mV
0100$_b$	310	410	510	mV
0101$_b$	345	460	575	mV
0110$_b$	380	510	640	mV
0111$_b$	420	560	700	mV

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Table 4-4: Serial Digital Output Swing Settings (Continued)

Register Setting (See Note 1)	Min	Typ	Max	Units
1000_b	455	605	760	mV
1001_b	490	655	820	mV
1010_b	530	705	880	mV
1011_b	565	755	945	mV
1100_b	600	800	1000	mV
1101_b	630	840	1050	mV
1110_b	670	890	1110	mV
1111_b	700	930	1160	mV

Note:

1. Applicable registers that can be programmed with the values shown above are DDO0_SWING_1G485, DDO0_SWING_270M, DDO0_SWING_125M, DDO0_SWING_BYPASS, DDO0_SWING_MUTE, DDO0_SWING_5G94, DDO0_SWING_2G97, DDO1_SWING_1G485, DDO1_SWING_270M, DDO1_SWING_125M, DDO1_SWING_BYPASS, DDO1_SWING_MUTE, DDO1_SWING_5G94, and DDO1_SWING_2G97

4.5.4 Output De-emphasis

The GS6152 features adjustable output de-emphasis to compensate for PCB dielectric trace loss. Each output can be independently set to a different de-emphasis setting for each detected rate through controls found in the DRIVER_CONTROL_REG_1 and DRIVER_CONTROL_REG_2 registers.

The effect of de-emphasis, illustrated in Figure 4-3, is to attenuate the swing of bits that do not follow a bit transition (V_{DE}). The swing of bits that do follow a bit transition (V_{nom}) is set by the output swing registers found in Section 4.5.3 and do not depend on the de-emphasis settings.

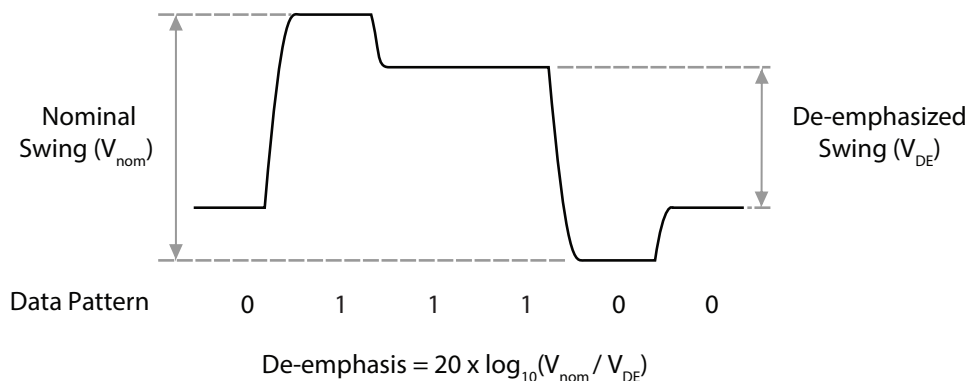$$\text{De-emphasis} = 20 \times \log_{10}(V_{nom} / V_{DE})$$

Figure 4-3: De-emphasis Waveform

The default de-emphasis settings for each rate are given in the register descriptions for DRIVER_CONTROL_REG_1 and DRIVER_CONTROL_REG_2 in Table 5-1. De-emphasis is

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