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GENLINX™ II GS9020A
Serial Digital Video Input Processor

DATA SHEET

FEATURES

- fully compatible with SMPTE 259M
- drop-in replacement for the GS9020
- auto-standard operation to 540MHz
- embedded EDH and data processing core
- selectable loop through or re-serialized EDH-processed serial output
- noise immune HVF timing signal outputs
- configurable FIFO reset pulse for clearing downstream FIFOs
- ANC header and TRS-ID correction for all standards
- user controlled output blanking
- ITU-R-601 output clipping for active picture area
- ancillary data indication
- low system power
- selectable I²C interface or 8-bit parallel port for access to EDH flags and device configuration bits
- EDH flags also available on dedicated pins
- seamless flag mapping to GS9021 EDH coprocessor
- 80 pin LQFP
- Pb-free and Green

APPLICATIONS

SMPTE 259M serial digital receiver for composite and component standards including 4:4:4:4 at 540Mb/s with EDH processing; Noise immune digital sync and timing generation; Cost effective EDH insertion and checking for serial routing and distribution applications.

DESCRIPTION

The GS9020A is specifically designed to deserialize SMPTE 259M serial digital signals. The inclusion of Error Detection and Handling (EDH) ensures the integrity of the data being received from the serial digital interface (SDI). Internal 75Ω termination resistors allow INTERLINX™ seamless connection with the GS9035A Reclocker or the GS9025A Receiver, thus providing a complete high performance, digital video input processor with EDH, digital sync signal generation, and other system features.

The GS9020A also includes a parallel to serial converter and NRZI scrambler to provide re-serialized, EDH compliant data output. The EDH core implements EDH insertion and extraction according to SMPTE RP-165. This core also generates noise immune timing signals such as horizontal sync, vertical blanking, field ID and ancillary data identification. It also provides many system features such as a FIFO reset pulse (which can be programmed to coincide with either EAV or SAV), TRS-ID and ANC header correction, user controlled output blanking and ITU-R-601 output clipping. The GS9020A has an I²C (Inter-Integrated Circuit, I²C is a registered Trademark of Philips) serial interface bus and an 8-bit parallel port for external access to all error flags and device configuration bits.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	Pb-FREE AND GREEN
GS9020ACFV	80 pin LQFP Tray	0°C to 70°C	No
GS9020ACTV	80 pin LQFP Tape	0°C to 70°C	No
GS9020ACFVE3	80 pin LQFP Tray	0°C to 70°C	Yes
GS9020ACTVE3	80 pin LQFP Tape	0°C to 70°C	Yes

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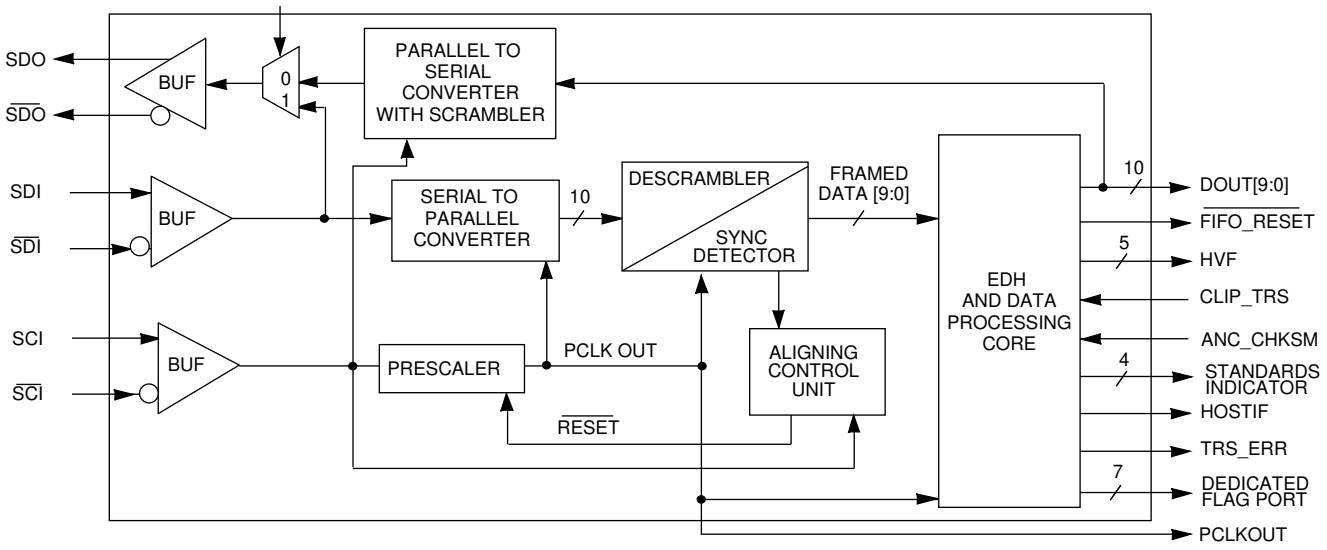


BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.3V to 6.0V
Input Voltage Range (any input)	-0.3 to V_{DD} +0.3V
Operating Temperature Range	0°C to 70°C
Storage Temperature	-55°C to 150°C
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARCTERISTICS

V_{DD} = 5.0 V, T_A = 0 - 70°C unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}		4.75	5.0	5.25	V	
Supply Current Unloaded	I_{DD}	270Mb/s	-	110	-	mA	
		540Mb/s	-	190	-	mA	
High Speed Serial Data and Clock Inputs	V_{CM}		3.14	3.65	3.95	V	
	V_{DIFFIN}		450	800	1250	mV	
	R_{PULLUP}		-	75	-	Ω	1
Serial Data Outputs	V_{CM}		-	2.7	-	V	
	$V_{DIFFOUT}$		-	800	-	mV	2
TTL Compatible CMOS Inputs	V_{ILMAX}		-	-	0.8	V	
	V_{IHMIN}		2.0	-	-	V	
	I_{IN}	V_{IN} = V_{DD} or GND	-	-	150	µA	3
			-	-	1	µA	4
	C_{IN}		-	10	-	pF	
TTL Compatible CMOS Outputs	V_{OLMAX}	at I_{OUT}	-	-	0.4	V	
	V_{OHMIN}	at I_{OUT}	2.4	-	-	V	
	I_{OUT}		-	8	-	mA	5
			-	4	-	mA	6
			-	2	-	mA	7

NOTES

1. R_{PULLUP} refers to the internal pullup resistor associated with the serial data and clock inputs (see Figure 4).
2. Assuming 100Ω differential termination resistor as shown in figure 7. Given $V_{DIFFOUT}$ = 800mV and a 100Ω termination, I_{SDO} = 8mA.
3. The following inputs have internal pull-up resistors: SDOMODE. The following inputs have internal pull-down resistors: ANC_CHKSM, FLYWDIS, FLAG_MAP, $\overline{\text{RESET}}$, CRC_MODE, FIFOE/$\overline{\text{S}}$ AND HOSTIF_MODE. To ensure reliable operation these pins should be externally connected to GND or V_{cc}.
4. All other inputs.
5. The following outputs have 8mA drivers (typical): PCLKOUT
6. The following outputs have 4mA drivers (typical): S[1:0], FL[4:0], ANC_DATA, DOUT[9:0], V, F[2:0], H, $\overline{\text{FIFO\_RESET}}$, TRS_ERR, NO_EDH
7. The following outputs have 2mA drivers (typical): P[7:0], STD[3:0], $\overline{\text{INTERRUPT}}$

AC ELECTRICAL CHARCTERISTICS

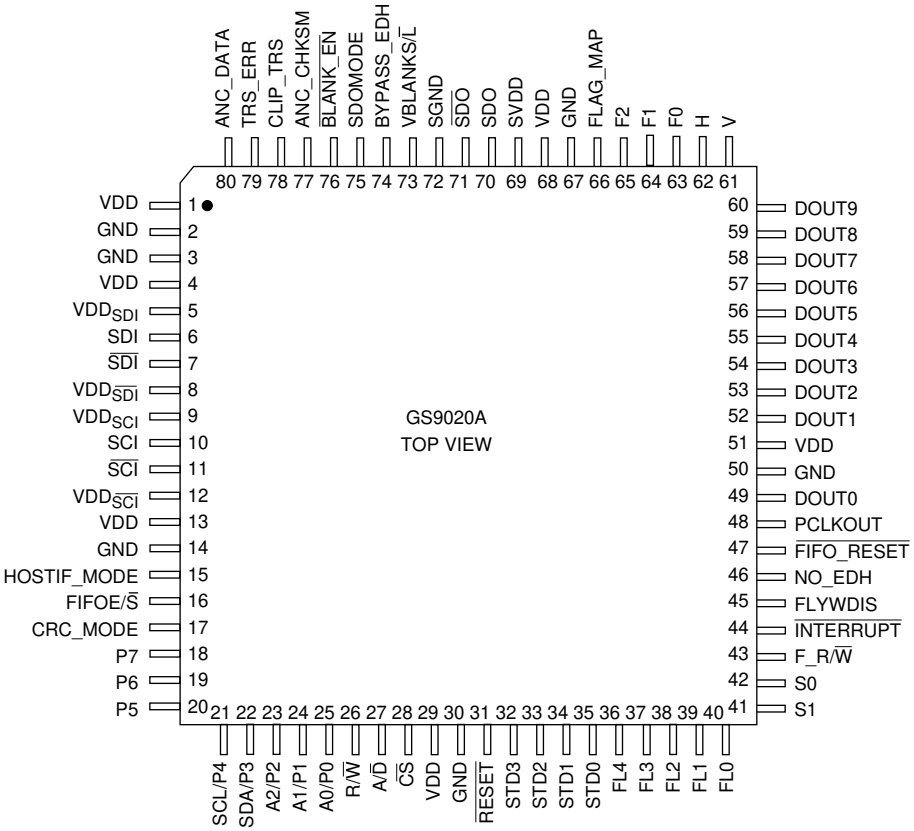
V_{DD} = 5.0 V, T_A = 0 - 70°C unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Serial Input Clock Frequency	f_{SCI}		-	-	540	MHz	
Serial Data Input Setup Time	t_{SS}		600	-	-	ps	1
Serial Data Input Hold Time	t_{SH}		600	-	-	ps	1
Serial Data Output Duty Cycle Distortion			-	5	-	%	
Serial Output Jitter		540Mb/s at eye crossing	-	360	-	ps p-p	
Serial Data Output Rise Time			-	600	-	ps	
Parallel Clock Output Jitter		27MHz at 50% voltage level	-	700	-	ps p-p	
Input Timing	t_1		20	-	-	ns	2
	t_2		-	-	9	ns	2
Output Delay Time	t_{OD}	with 25pF loading	T/2	-	T/2+7	ns	3
Output Hold Time	t_{OH}	with 25pF loading	T/2-3	-	-	ns	3
Output Setup Time	t_{OS}	with 25pF loading	T/2-7	-	-	ns	3
Flag Port Disable Time	t_{FDIS}	with 25pF loading	-	-	T/2+0.5	ns	
Flag Port Enable Time	t_{FEN}	with 25pF loading	-	-	T/2+1	ns	
I²C Clock Frequency	f_{SCL}		-	-	400	kHz	
Host Interface Setup Time	t_{HS}		6	-	-	ns	4
Host Interface Hold Time	t_{HH}		6	-	-	ns	4
Host Interface Output Enable Time	t_{HEN}	with 25pF loading	-	-	21	ns	4
Host Interface Output Disable Time	t_{HDIS}	with 25pF loading	-	-	10	ns	4
Reset Time Pulse Width	t_{RESET}		100	-	-	ns	

NOTES

1. The serial clock rising edge should occur at the centre of the data period for optimum performance. (See Figure 1)
2. Since the GS9020A does not have a parallel clock input, it is not possible to define timing details relative to it. Instead the GS9020A has a parallel clock output and all timing information is relative to PCLKOUT. The flag port pins (FL[4:0], F_R/$\overline{W}$, S[1:0]) are the only inputs where the timing details are important. The timing requirements are shown in Figure 2.
3. These times are relative to the rising edge of PCLKOUT as shown in Figure 3. Note that the data transitions at the falling edge of PCLKOUT. T is the parallel clock period in ns.
4. The Host Interface signals, P[7:0], R/$\overline{W}$, A/$\overline{D}$ and $\overline{CS}$ are asynchronous to the parallel clock.

PIN CONNECTIONS



PIN DESCRIPTIONS

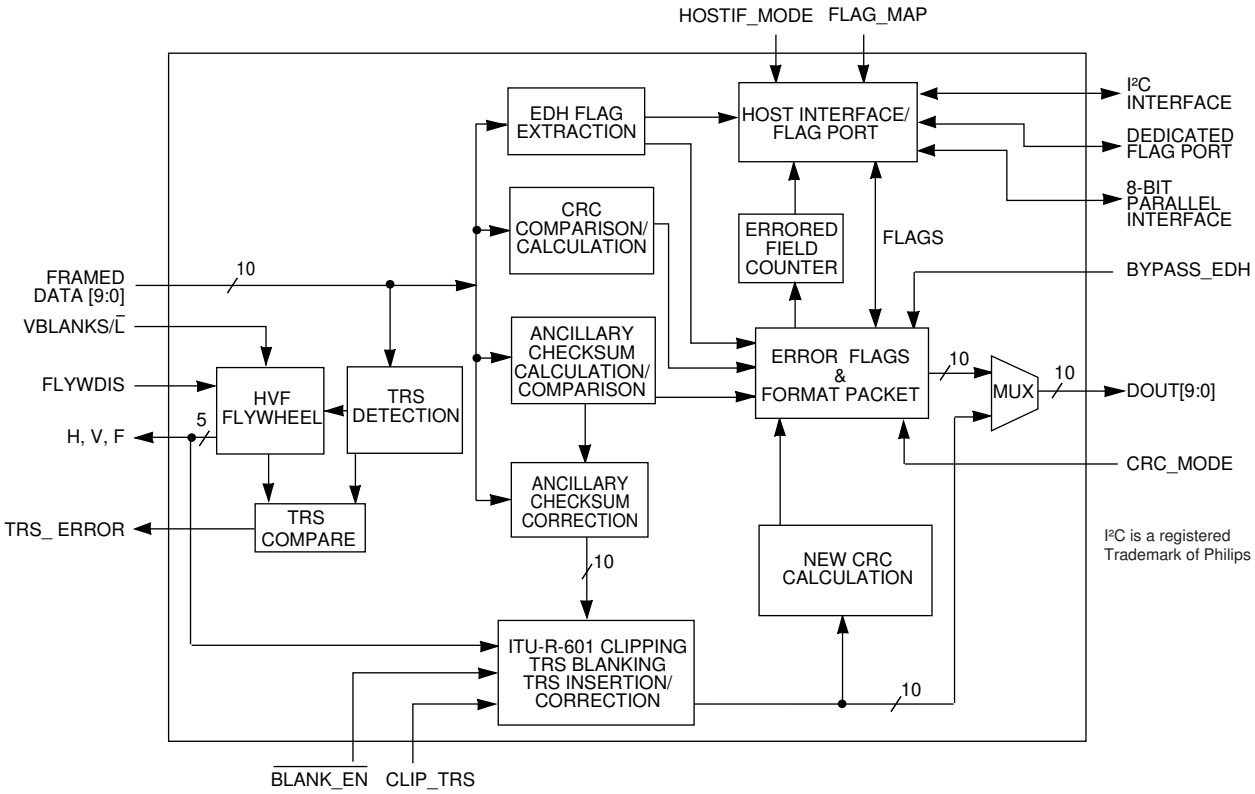
NUMBER	SYMBOL	TYPE	DESCRIPTION
6, 7	SDI, $\overline{SDI}$	I	Differential serial data inputs.
10, 11	SCI, $\overline{SCI}$	I	Differential serial clock inputs.
15	HOSTIF_MODE	I	Host interface mode select. When HIGH, the host interface is configured for I²C mode. When LOW, the host interface is configured for parallel port mode.
16	FIFOE/$\overline{S}$	I	$\overline{FIFO\_RESET}$ pulse control. When HIGH, the output $\overline{FIFO\_RESET}$ pulse occurs on the EAV word. When LOW, the output $\overline{FIFO\_RESET}$ pulse occurs on the SAV word.
17	CRC_MODE	I	CRC_MODE enable. When HIGH, CRC_MODE is enabled. When LOW, CRC_MODE is disabled.
18 - 20	P[7:5]	I/O	In parallel port mode, these are bits 7:5 of the host interface address/data bus. In I²C mode, these pins must be set LOW.
21	SCL/P4	I/O	In parallel port mode, this is bit 4 of the host interface address/data bus. In I²C mode, this is the serial clock input for the I²C port.
22	SDA/P3	I/O	In parallel port mode, this is bit 3 of the host interface address/data bus. In I²C mode, this is the serial data pin for the I²C port.
23 - 25	A[2:0]/P[2:0]	I/O	In parallel port mode, these are bits 2:0 of the host interface address/data bus. In I²C mode, these are input bits which define the I²C slave address for the device.
26	R/$\overline{W}$	I	Parallel port read/write control. When HIGH, the parallel port is configured as an output (read mode). When LOW, the parallel port is configured as an input (write mode). In I²C mode, this pin must be set HIGH.

PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
27	A/$\overline{D}$	I	Parallel port address/data bus control. When HIGH, the parallel port is used for address input. When LOW, the parallel port is used for data input or output. In I²C mode, this pin must be set LOW.
28	$\overline{CS}$	I	Parallel port chip select. When $\overline{CS}$ is LOW and R/$\overline{W}$ is HIGH, the GS9020A drives the address/data bus. When $\overline{CS}$ is LOW and R/$\overline{W}$ is LOW, the user should drive the address/data bus. When $\overline{CS}$ is HIGH, the address/data bus is in a high impedance state (Hi - Z). In I²C mode, this pin must be set HIGH.
31	$\overline{RESET}$	I	Reset. When LOW, the internal control circuitry is reset.
32 - 35	STD[3:0]	O	Video standards indication as described in section 1.4
36 - 40	FL[4:0]	I/O	EDH flag data port to allow access to the EDH flags.
41, 42	S[1:0]	I/O	Control bits which select whether FF, AP, or ANC EDH flags are active on the EDH flag data port (FL[4:0]). In FLAG_MAP mode, the S[1:0] pins become outputs (see device description).
43	F_R/$\overline{W}$	I	Flag port read/write control. When HIGH, FL[4:0] are configured as outputs allowing EDH flags to be read from the device. When LOW, FL[4:0] are configured as inputs allowing EDH flags to be overwritten in the outgoing EDH packet. In FLAG_MAP mode this pin must be set HIGH.
44	$\overline{INTERRUPT}$	O	Interrupt output. This output goes low when EDH errors occur. This pin is an open drain output and requires an external pullup resistor. If this output is not used, a pullup resistor is not required.
45	FLYWDIS	I	Flywheel disable. When HIGH, the internal flywheel is disabled. When LOW, the internal flywheel is enabled.
46	NO_EDH	O	No EDH present indication. When HIGH, indicates EDH packets are not present in the incoming data stream.
47	$\overline{FIFO\_RESET}$	O	FIFO Reset output. Asserted LOW during the TRSID word for composite standards and the EAV or SAV word for component standards.
48	PCLKOUT	O	Parallel clock output.
52-60,49	DOUT[9:0]	O	Parallel digital video data outputs.
61	V	O	Vertical sync indication.
62	H	O	Horizontal sync indication.
63 - 65	F[2:0]	O	Field indication. F2 is the MSB.
66	FLAG_MAP	I	FLAG_MAP mode enable. When HIGH, FLAG_MAP mode is enabled. When LOW, FLAG_MAP mode is disabled.
70, 71	SDO/$\overline{SDO}$	O	Differential serial data outputs.
73	VBLANKS/$\overline{L}$	I	Vertical blanking interval control. For NTSC signals, when VBLANKS/$\overline{L}$ is set LOW the 19 line blanking interval is selected and when set HIGH the 9 line blanking interval is selected. For PAL D2 signals, when VBLANKS/$\overline{L}$ is set LOW the 17 line blanking interval is selected and when set HIGH the 7 line blanking interval is selected. For PAL component signals VBLANKS/$\overline{L}$ should be set LOW.
74	BYPASS_EDH	I	Bypass EDH control. When HIGH, the device allows the EDH packet to pass through unaltered.
75	SDOMODE	I	Serial data output control. When LOW, the serial data output is re-serialized processed data. When HIGH, the serial data output is the looped through serial input. After changing SDOMODE, the GS9020A must be reset for proper operation.
76	$\overline{BLANK\_EN}$	I	Blanking enable. When LOW, incoming data words are set to appropriate blanking levels.
77	ANC_CHKSM	I	Ancillary checksum updating enable. When HIGH, ancillary checksum updating is enabled.

PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
78	CLIP_TRS	I	Clip and TRS correction control. When HIGH, the TRS Blanking, ITU-R-601 clipping and TRS insertion features are enabled.
79	TRS_ERR	O	TRS error indication. When HIGH, indicates a TRS error in the data stream such as a missing TRS, an improperly placed TRS, or an incorrect TRS ID word.
80	ANC_DATA	O	Ancillary data indication. When HIGH, indicates that an ANC packet is coming out of the device. The output is high from the beginning of the first header word to the end of the checksum word of the ANC packet.
1, 4, 13	VDD		Power supply connection for the serial processing circuitry (nominally +5V).
2, 3, 14	GND		Ground connection for the serial processing circuitry.
69	SVDD		Power supply connection for the serial data outputs. To save power when not using the SDO/$\overline{\text{SDO}}$ outputs, set this pin to ground.
72	SGND		Ground connection for the serial data outputs.
5, 8	VDD_SDI, $\overline{\text{SDI}}$		Power supply connection for the internal 75 ohm pullup resistor (nominally +5V) on the serial data input lines.
9, 12	VDD_SCI, $\overline{\text{SCI}}$		Power supply connection for the internal 75 ohm pullup resistor (nominally +5V) on the serial clock input lines.
29,51,68	VDD		Power supply connection for the parallel processing circuitry (nominally +5V).
30,50,67	GND		Ground for the parallel processing circuitry.



BLOCK DIAGRAM - EDH AND DATA CORE PROCESSING

DETAILED DESCRIPTION

The GS9020A EDH coprocessor consists of five major blocks:

1. Data Input/Output Block (with automatic standard detect)
2. Flywheel Block
3. EDH Block
4. Data Processing Block
5. Host Interface (HOSTIF) Block

The following convention is used to differentiate device pins from HOST interface table bits.

PIN	LOGIC OPR	HOSTIF
XX		YY

LOGIC OPR (logic operator) gives the combinational relationship (if one exists), between pins which also have a corresponding HOST bit. This operator governs the signal the GS9020A receives. The following is the list of possible logic operators and their meaning.

LOGIC OPR	MEANING
AND	XX AND YY
OR	XX OR YY
>	XX takes precedence over YY
<	YY takes precedence over XX

1. DATA INPUT/OUTPUT BLOCK

1.1 Serial Video Data Inputs

PIN	LOGIC OPR	HOST BIT
SDI, $\overline{\text{SDI}}$ SCI, $\overline{\text{SCI}}$		

Serial data and clock signals are supplied to the GS9020A chip via the SDI/$\overline{\text{SDI}}$ and SCI/$\overline{\text{SCI}}$ pins, respectively. Eight standards are supported: Composite, 4:2:2 Component with 13.5MHz Y sampling, 4:2:2 16 x 9 wide screen with 18MHz Y sampling, and 4:4:4:4 Component Single Link with 13.5MHz Y sampling, all in both NTSC and PAL formats. See Table 1.

SDI/$\overline{\text{SDI}}$ and SCI/$\overline{\text{SCI}}$ are high speed Pseudo-ECL (PECL) compatible differential inputs with internal pullup resistors (75Ω nominally) as shown in Figure 4. Note that each pullup resistor has a dedicated power pin allowing the use of other interfacing topologies.

The internal pullup resistors allow the GS9020A to be easily interfaced to the GS9025A as shown in Figure 5 and Figure 17. An external diode is required to offset the input signals to the input range of the GS9020A. For maximum signal integrity the GS9025A and GS9020A should be placed as close together as possible.

The PECL serial input signals are first converted to CMOS levels and then deserialized to 10 bit parallel format (based on the TRS headers), descrambled, and then passed to the processing core.

1.2 Parallel Digital Video Data Outputs

PIN	LOGIC OPR	HOST BIT
DOUT[9:0]		

The output of the device is 10-bit digital video data and is present on the DOUT[9:0] output pins.

1.3 Reserialized Data Output

PIN	LOGIC OPR	HOST BIT
SDO, $\overline{\text{SDO}}$ SDOMODE		

The GS9020A also provides PECL differential serial data outputs (SDO/$\overline{\text{SDO}}$). The serial data outputs can operate in one of two modes as controlled by the SDOMODE pin. When SDOMODE is set LOW, re-serialized processed data is output at the SDO/$\overline{\text{SDO}}$ output pins. In this mode it is recommended that the lock output of the GS9025A or GS9035A connected to the $\overline{\text{RESET}}$ input of the GS9020A, and to a pull up resistor. This will effectively reset the GS9020A whenever the signal lock is lost. Note that any GS9020A programming through the host interface will be lost after this reset. It will be necessary to reprogram the GS9020A after each reset.

When SDOMODE is set HIGH, the serial input data is supplied directly to the SDO/$\overline{\text{SDO}}$ output pins, bypassing the processing core. After changing SDOMODE, the GS9020A must be reset for proper operation.

The serial data output circuits are shown in Figure 6. The serial data outputs are designed to drive 50-75Ω controlled impedance traces and can be easily connected to the GS9028 cable driver as shown in Figure 7 and Figure 18. Note that to output proper PECL signal levels, a resistor must be connected between the two serial data outputs.

1.4 Automatic Standard Detection

PIN	LOGIC OPR	HOST BIT
STD[3:0]		STD_SEL STD[3:0] S

The device automatically detects the incoming video standard. The detected standard is encoded on the STD[3:0] pins and the HOSTIF read table bits as shown in Table 1 and Table 3.

TABLE 1

STANDARD NAME	STD[3:0]
NTSC 4:2:2 Component with 13.5MHz Y sampling	0000
NTSC Composite	0001
NTSC 4:2:2 16x9 Widescreen with 18MHz Y sampling	0010
NTSC 4:4:4:4 Single Link with 13.5MHz Y sampling	0011
PAL 4:2:2 Component with 13.5MHz Y sampling	0100
PAL Composite	0101
PAL 4:2:2 16x9 Widescreen with 18MHz Y sampling	0110
PAL 4:4:4:4 Single Link with 13.5MHz Y sampling	0111

Noise immunity is included to ensure that momentary signal corruption does not affect the automatic standards detection function. This built in noise immunity results in delayed detection time during power up and when switching between standards. Delays range from as little as eight lines when switching between component standards to as much as four frames when switching between PAL and NTSC standards. If this delay is intolerable, the user can manually set the standard through the HOSTIF write table. To set the standard manually, the STD_SEL bit must be set HIGH and the S bit and STD[3:0] pins/HOSTIF bits set accordingly. The default standard upon reset of the chip is NTSC 4:2:2 component (13.5MHz Y sampling).

The S bit, used for single link data standards only, is encoded in the TRSID word and indicates if the data is in RGB or YC_RC_B format as per SMPTE RP174. In automatic standard detection mode, the S bit can be read from the HOSTIF read table. In manual mode, the S bit must be set in the HOSTIF write table.

1.5 Parallel Clock Output

PIN	LOGIC OPR	HOST BIT
PCLKOUT		

The PCLKOUT pin provides the output parallel clock. All synchronous I/O are timed relative to PCLKOUT. The following listing shows which I/O's are synchronous and which are not. Timing for synchronous outputs is shown in Figure 3. Timing for synchronous inputs is shown in Figure 2.

SYNCHRONOUS	ASYNCHRONOUS
FL[4:0]	P[7:5]
S[1:0]	SCL/P4
$\overline{\text{FIFO\_RESET}}$	$\overline{\text{INTERRUPT}}$
DOUT[9:0]	SDA/P3
F[2:0]	A[2:0]/P[2:0]
V	R/$\overline{W}$
H	A/$\overline{D}$
ANC_DATA	$\overline{CS}$
$\overline{\text{BLANK\_EN}}$	FLAG_MAP
F_R/$\overline{W}$	$\overline{\text{RESET}}$
NO_EDH	CRC_MODE
STD[3:0]	VBLANKS/$\overline{L}$
TRS_ERROR	HOSTIF_MODE
	FIFOE/$\overline{S}$
	FLYWDIS
	BYPASS_EDH
	SDO_MODE
	ANC_CHKSM
	CLIP_TRS

2. FLYWHEEL BLOCK

2.1 FVH Flywheel

PIN	LOGIC OPR	HOST BIT
FLYWDIS	OR	FLYWDIS SWITCHFLYW

The flywheel's primary function is to provide accurate field, vertical, and horizontal output signals in the presence of noisy or error prone input data. Flywheel synchronization is based on the TRS words in the incoming data stream. The FVH flywheel synchronizes to the incoming data stream in less than two fields once the incoming standard has been detected. Once synchronized, the TRS words in the incoming data stream and those generated by the flywheel are constantly compared to ensure that the flywheel remains synchronized.

Noise insensitivity is accomplished by re-synchronizing the flywheel to the data stream only if it is not aligned for long periods of time. For component signals, four mismatches between the EAV signal in the incoming and flywheel generated signals over a window of eight lines will trigger the flywheel to begin re-synchronization. For composite signals, re-synchronization is triggered by mismatches in the TRS encoded line numbers or field bits for 7 consecutive lines.

The flywheel can be disabled by asserting the FLYWDIS control signal HIGH. Disabling the flywheel will remove the effective noise immunity. In this mode, FVH values will be decoded directly from the incoming data stream rather than being decoded from the flywheel. Note that when the flywheel is disabled, TRS_BLANK and TRS_INSERT will not function correctly if enabled. Therefore if the flywheel is disabled then so should TRS_BLANK and TRS_INSERT. FLYWDIS is available as an input pin and as a bit in the HOSTIF write table.

The SWITCHFLYW control signal is used in applications where the data input to the GS9020A is switched between two synchronous signals. In this case, the two signals may be slightly misaligned and would normally require the flywheel to completely re-synchronize. In this scenario, the re-synchronization time would be undesirable. Asserting the SWITCHFLYW bit of the HOSTIF write table HIGH allows the flywheel to re-synchronize to the new incoming signal at the end of the switching line.

For this functionality to operate properly, the two signals must both be in the active picture portion of the switching line at the time of the switch.

2.2 Accurate FVH Timing Signals

PIN	LOGIC OPR	HOST BIT
F[2:0] V H VBLANKS/$\overline{L}$	 AND	F[2:0] VBLANKS/$\overline{L}$

The F[2:0] signals indicate the current field of the video data. Three F bits are necessary to accommodate the composite PAL standard which has 8 fields. The F[2:0] bits are available on dedicated output pins and via the HOSTIF read table. Figure 8a and 8b illustrate the position of the F[2:0] transition within a line for component and composite signals, respectively. For component standards only, F0 is used to indicate fields 0 and 1. The lines on which the transitions occur conform to the SMPTE standards.

For component signals, the horizontal (H) signal is HIGH during the horizontal blanking region of the output signal, from EAV to SAV inclusive. For composite signals, the H signal remains HIGH only for the 3FF, 000, 000, 000, and TRSID words. Figure 8a and 8b illustrate the H output signal timing for component and composite signals, respectively.

The vertical (V) signal timing is dependent on the incoming video standard and the VBLANKS/$\overline{L}$ control signal. The VBLANKS/$\overline{L}$ signal is available as an input pin and via the HOSTIF write table and should be set to indicate the form of the incoming data stream. This allows the flywheel to correctly structure the V bit for flywheel synchronization, TRS insertion, and TRS error indication.

For component based standards, the transition of the V output signal within a line is shown in Figure 8a. The line on which the V output signal transitions from HIGH to LOW is summarized in the table below. The lines on which the LOW to HIGH transition occurs conform to the SMPTE standards.

STANDARD	VBLANKS/$\overline{L}$=1	VBLANKS/$\overline{L}$=0
NTSC 4:2:2 Component (13.5MHz Y sampling)	9/272	19/282
NTSC 4:2:2 16x9 Widescreen (18MHz Y sampling)	9/272	19/282
NTSC 4:4:4:4 Single Link (13.5MHz Y sampling)	9/272	19/282
PAL 4:2:2 Component (13.5MHz Y sampling)	22/335	22/335
PAL 4:2:2 16x9 Widescreen (18MHz Y sampling)	22/335	22/335
PAL 4:4:4:4 Single Link (13.5MHz Y sampling)	22/335	22/335

For composite based standards, the V output signal is asserted HIGH as described in the following table:

	VBLANKS/$\overline{L}$=1	VBLANKS/$\overline{L}$=0
NTSC Composite	from Line 525/ Sample 768 to Line 9/ Sample 767 inclusive AND from Line 263/ Sample 313 to Line 272/ Sample 767 inclusive	from Line 525/ Sample 768 to Line 19/ Sample 767 inclusive AND from Line 263/ Sample 313 to Line 282/ Sample 767 inclusive
	VBLANKS/$\overline{L}$=1	VBLANKS/$\overline{L}$=0
PAL Composite	from Line 623/ Sample 382 to Line 5/ Sample 947 inclusive AND from Line 310/ Sample 948 to Line 317/ Sample 947 inclusive	from Line 623/ Sample 382 to Line 15/ Sample 947 inclusive AND from Line 310/ Sample 948 to Line 327/ Sample 947 inclusive

2.3 TRS Errors

PIN	LOGIC OPR	HOST BIT
TRS_ERR		TRS_ERR

The flywheel is used to indicate TRS errors. These errors are detected by comparing the TRS in the incoming data stream with the expected TRS based on the internal flywheel. If a mismatch occurs, the TRS_ERR signal is immediately set HIGH and maintained HIGH until a correct TRS occurs. The types of TRS errors detected are:

- TRS missing
- TRS in wrong location
- TRS-ID is different from the one generated by the flywheel

The TRS_ERR signal is available as an output pin and via the HOSTIF read table. The TRS_ERR signal should only be considered valid if the flywheel is enabled.

2.4 FIFO Reset Pulse

PIN	LOGIC OPR	HOST BIT
FIFOE/$\overline{S}$ $\overline{FIFO\_RESET}$		

The GS9020A also provides a $\overline{FIFO\_RESET}$ pulse on the $\overline{FIFO\_RESET}$ output pin. This pin is always HIGH except when the TRSID word is exiting the device as shown in Figure 9. For component standards, a FIFOE/$\overline{S}$ input pin is used to determine if the $\overline{FIFO\_RESET}$ pulse occurs during the EAV or SAV word of the outgoing data.

If FIFOE/$\overline{S}$ is HIGH, the active low pulse of the $\overline{FIFO\_RESET}$ output pin occurs during the EAV word. If FIFOE/$\overline{S}$ is LOW, the active low output pulse occurs during the SAV word. For composite signals the FIFOE/$\overline{S}$ pin has no effect since there is only one TRS-ID word per line. This feature is useful for synchronizing line store FIFOs that follow the GS9020A.

3. EDH PROCESSING BLOCK

This section describes the GS9020A's EDH features and functionality.

3.1 Error Flags

PIN	LOGIC OPR	HOST BIT
		INCOMING ERROR FLAGS OUTGOING ERROR FLAGS STICKY IN STICKY OUT OVERWRITE VALUES OVERWRITE CONTROL RO_CTRL RESERVED WORDS (INCOMING) RESERVED WORDS (OUTGOING)

All 15 EDH error flags can be read from the HOSTIF read table. The INCOMING ERROR FLAGS represent the EDH error flags present in the incoming EDH packet. The OUTGOING ERROR FLAGS represent the EDH error flags present in the outgoing EDH packet (after modification by the GS9020A). Please note that the EDH flags can also be accessed using the flag port as described later.

The INCOMING and OUTGOING ERROR FLAGS, the incoming Validity bits (FFV and APV), and the EDH_CHKSM bit can be made "sticky".

Sticky error flags that detect an error for a field remain asserted until a HOSTIF read is performed on those error flags. Sticky mode allows the user to perform HOSTIF reads on the error flags to detect if any errors have occurred since the last read, and are particularly useful when a read cannot be performed after every field. When STICKY IN is asserted HIGH, the incoming flags and validity bits are in sticky mode. When STICKY OUT is asserted HIGH, the outgoing flags and the EDH_CHKSM bit are in sticky mode. Note that the $\overline{\text{INTERRUPT}}$ signal is derived from these signals so that it too becomes sticky. STICKY IN and STICKY OUT are available in the HOSTIF write table. The ERROR FLAGS and the EDH_CHKSM bit are sticky HIGH. That is, once they are set HIGH, they remain HIGH until a read operation. The Validity bits are sticky LOW. That is, once they are set LOW, they remain LOW until a read operation.

In some applications, the user may wish to insert user defined EDH error flags into the outgoing EDH packet. The desired outgoing error flags are written into the OVERWRITE VALUES words of the HOSTIF write table and are placed in the outgoing EDH packet when the corresponding OVERWRITE CONTROL bit is asserted HIGH. See Table 2 for the HOSTIF Write Table.

The GS9020A also allows the user to overwrite the seven reserved words of the OUTGOING EDH packet. When RO_CTRL (Reserved Word Overwrite Control) is asserted HIGH, the GS9020A overwrites the reserved words in the OUTGOING EDH packet with those specified in the HOSTIF write table. If RO_CTRL is LOW, the GS9020A does not alter the reserved words. RO_CTRL is a control bit in the HOSTIF write table. The reserved words of the INCOMING EDH packet are also available via the HOSTIF read table.

3.2 CRC Calculation And Updating

PIN	LOGIC OPR	HOST BIT
		INCOMING FF CRC OUTGOING FF CRC INCOMING AP CRC OUTGOING AP CRC

Since the device has the potential of modifying the full-field and active picture data with features like ITU-R-601 clipping and TRS insertion, the full field and active picture CRC values must be calculated for both the incoming and outgoing data streams. The calculated CRC values based on the incoming data stream are used for comparison with the embedded CRC values. However, the calculated CRC values based on the outgoing data stream are the ones inserted into the data stream. As a result, the CRC values in the outgoing data stream correctly reflect the contents of the outgoing data stream.

The INCOMING FF and AP CRC values for the Full Field (FF) and Active Picture (AP) regions can be read from the HOSTIF read table. Similarly, the OUTGOING (calculated) FF and AP CRC values for the Full Field and Active Picture regions can be read from the HOSTIF read table.

3.3 Validity Bit

PIN	LOGIC OPR	HOST BIT
		FFV APV

The VALIDITY (V) bits (as per SMPTE 165) present in the incoming EDH packet are used to indicate whether the CRC values are valid or invalid. If the V bit is HIGH, the CRC value is considered valid. In this case, the incoming CRC value is compared with the calculated CRC value to identify errors. If the V bit is LOW, the incoming CRC is invalid and a CRC comparison is not performed. If the device receives an EDH packet with the V bit set LOW it behaves as follows:

1. EDH = 0 (Not asserted for an invalid CRC)
2. EDA = EDAin "OR" EDHin (EDA calculated as usual)
3. A new calculated CRC value replaces the invalid one in the output EDH packet
4. The V bit will be set HIGH in the output EDH packet
5. Depending on whether one or both or FFV or APV is low, the Unknown Error Status (UES) flag corresponding to either FF or AP or both, is set HIGH in the output data. (No CRC check could be performed, so the data may or may not contain errors).

The incoming V bits for the Full Field and Active Picture regions are available in the HOSTIF read table as FFV and APV, respectively. Outgoing full field (FFV) and active picture (APV) validity bits are set HIGH unless explicitly over-written through the HOSTIF write table or the flag port.

3.4 Ancillary Checksum Verification

PIN	LOGIC OPR	HOST BIT
ANC_CHKSM	OR	ANC_CHKSM EDH_CHKSM

For each received ANC packet in the incoming data, the device compares the calculated checksum value to the embedded checksum for that ANC packet. If the checksum values do not match for any ANC packets within a field, an error is reported via the ancillary EDH flag in the EDH packet. In addition, if the ANC_CHKSM input pin or HOSTIF write table bit is asserted HIGH, the ancillary checksum correction block is enabled and the checksum in the ANC packet is replaced with the calculated one. This update is required to prevent the ANC data error from being flagged at every downstream EDH chip.

When implementing applications which use the EDH core (ie. BYPASS_EDH set LOW), ANC_CHKSM will indicate a downstream FF/AP EDH error when an illegal/non-allowed ($3FC_H$-$3FF_H$) ANC_CHKSM input value is detected. As such, these values should not be present in the incoming data and the corresponding FF/AP EDH errors should not occur. However, if the user wishes to disable the ANC_CHKSM function, it can be deactivated by setting both the ANC_CHSKM pin and the ANC_CHKSM host interface bit LOW.

If the chip is receiving ANC EDH flag information through the flag port or the HOSTIF, then the ANC EDH flag generated by the ancillary checksum verification block will be overwritten. However, the additional FF/AP EDH flag will still appear at the next downstream chip if an illegal checksum of $3FC_H$-$3FF_H$ was detected and the ANC_CHKSM function was enabled.

If a checksum error is detected in the EDH packet itself, an additional separate error flag, EDH_CHKSM is set HIGH in the HOSTIF read table.

3.5 UES Error Flag Updating

In receive mode, a UES flag is set HIGH in the outgoing EDH packet if the corresponding UES flag was HIGH in the incoming packet or if the corresponding V bit was LOW. (For example, if the incoming Active Picture V bit is LOW, the outgoing Active Picture UES bit will be HIGH). If there is no EDH packet in the incoming data, all three UES flags (ANC, AP, FF) are set HIGH.

3.6 ANC_DATA

PIN	LOGIC OPR	HOST BIT
ANC_DATA		

The ANC_DATA signal is set HIGH when an ancillary data packet is exiting the GS9020A. This pin is asserted from the start of the first header word through to the end of the checksum word of the ANC packet, inclusive, as shown in Figure 10.

3.7 NO_EDH

PIN	LOGIC OPR	HOST BIT
NO_EDH		NO_EDH

Some input data streams may lack the EDH packet. In such cases, the NO_EDH output pin or HOSTIF read table bit is asserted HIGH. If only a few fields lack the EDH packet, the NO_EDH pin/bit will be asserted only for those fields.

In determining if the input data stream contains an EDH packet, the GS9020A looks for two things. First the presence of an ANC packet with the header 000 3FF 3FF 1F4 and second that the ANC header is in the right spot for the video standard detected. The NO_EDH signal is a logical NAND of these two cases. If either one is false, the NO_EDH flag is set.

3.8 ERRORED FIELD COUNTER

PIN	LOGIC OPR	HOST BIT
		ERRORED FIELD COUNTER CLR[1:0] ERROR SENSITIVITY BITS

The device has a 24 bit ERRORED FIELD COUNTER. The counter increments by one on the occurrence of one or more error flags in an OUTGOING EDH packet. The error flags that can increment the counter are user-selectable through the 16 ERROR SENSITIVITY bits in the HOSTIF write table. The error flag SENSITIVITY bits are active LOW, so that if a particular sensitivity bit is set LOW, the counter is sensitive to errors of that type in the OUTGOING EDH packet. The EDH_CHKSM sensitivity bit is active HIGH.

There are four modes of counter operation. The mode is set through 2 bits in the HOSTIF write table, denoted CLR1 and CLR0.

CLR1	CLR0	MODE OF OPERATION
0	0	Normal
0	1	Reset Counter to Zero
1	0	Auto Reset
1	1	Hold Counter at Zero

In "Normal" mode the counter operates as previously discussed, such that the counter increments on detection of any error for which the sensitivity flags are set HIGH. If “Reset Counter to Zero” mode is selected, the counter is reset to zero and begins counting again. The mode of operation will immediately return to 00 (normal mode) once the counter resets. In "Auto Reset" mode, the counter behaves in the normal fashion, except that it resets to zero every time a HOSTIF read of the lowest 8 bits of the error counter (address 17) is performed. This functionality allows the chip to count the number of errors since the last read. The “Hold Counter at Zero” mode instantly freezes the counter at zero until it is moved into one of the other modes.

3. 9 INTERRUPT Signal

PIN	LOGIC OPR	HOST BIT
$\overline{\text{INTERRUPT}}$		

An interrupt output pin ($\overline{\text{INTERRUPT}}$) is also available on the GS9020A. The $\overline{\text{INTERRUPT}}$ output is asserted LOW for each field that contains errors in the outgoing EDH packet. The sensitivity flags used for the 24 bit errored field counter also apply to the interrupt signal. As a result, the interrupt can be made sensitive to any particular flags. The $\overline{\text{INTERRUPT}}$ signal is stable after an EDH packet exits the device and before the subsequent EDH packet enters the device as shown in Figure 11.

If the STICKY OUT control bit is asserted HIGH, the interrupt remains asserted LOW until a HOSTIF read is performed on the flag that caused the interrupt.

The $\overline{\text{INTERRUPT}}$ output is an open drain output and as a result requires an external pull-up resistor. A 10k resistor value is recommended. If this output is not used, a pullup resistor is not required.

3.10 Flag Port

PIN	LOGIC OPR	HOST BIT
F_R/$\overline{\text{W}}$		
S[1:0]		
FL[4:0]	>	OVERWRITE VALUES

In addition to the HOSTIF tables, the EDH error flags can also be read and written via the synchronous flag port. The five flag port pins, FL[4:0], allow access to all 15 error flags. The select pins S[1:0] control which flags are read/written as outlined below. If the flag port is not going to be used, it is best to set F_R/$\overline{\text{W}}$ high, leave FL[4:0] unconnected, and set S[1:0] to any value desired (but not floating).

3.10.1 Write Mode

When the F_R/$\overline{\text{W}}$ pin is LOW, the flag port is in write mode and the FL[4:0] pins are configured as inputs. After writing to the flag port, the GS9020A inserts the written flags into the next outgoing EDH packet. Note that external flag overwriting via the flag port takes precedence over HOSTIF overwriting but the flag port writing only affects the next outgoing EDH packet. Following this, if the flag port is not written to again, flag operation is returned to normal EDH functionality (unless it is being overwritten through the HOSTIF).

The data present on the FL[4:0] output pins, as controlled by the S[1:0] pins, is summarized below.

Write Mode, F_R/$\overline{\text{W}}$ = 0

S[1:0]	FL4	FL3	FL2	FL1	FL0
00	FF UES	FF IDA	FF IDH	FF EDA	FF EDH
01	AP UES	AP IDA	AP IDH	AP EDA	AP EDH
10	ANC UES	ANC IDA	ANC IDH	ANC EDA	ANC EDH
11	IN/$\overline{\text{OUT}}$	APV	FFV	0	0

In addition to overwriting the 15 error flags, the outgoing validity bits for the active picture (APV) and full field (FFV) can be overwritten via the flag port.

The IN/$\overline{\text{OUT}}$ bit has no effect on writes to the error flags. IN/$\overline{\text{OUT}}$ is a control bit used to determine if the flags read from the flag port during flag port read cycles represent incoming or outgoing EDH flags. If this bit is set HIGH, all subsequent reads are from the incoming EDH packet. If this bit is set LOW, then all subsequent reads are from the updated outgoing packet. When the IN/$\overline{\text{OUT}}$ bit is written to, the value remains latched until it is re-programmed. The IN/$\overline{\text{OUT}}$ bit is set LOW upon reset of the chip.

3.10.2 Read Mode

When the F_R/$\overline{W}$ pin is HIGH, the flag port is in read mode and the FL[4:0] pins are configured as outputs. The data present on the FL[4:0] output pins, as controlled by the S[1:0] pins, is summarized below.

Read Mode, F_R/$\overline{W}$ = 1

S[1:0]	FL4	FL3	FL2	FL1	FL0
00	FF UES	FF IDA	FF IDH	FF EDA	FF EDH
01	AP UES	AP IDA	AP IDH	AP EDA	AP EDH
10	ANC UES	ANC IDA	ANC IDH	ANC EDA	ANC EDH
11	EDH_ CHKSUM	APV	FFV	S	

Note that the 15 error flags can be read from the incoming or outgoing EDH packet (see IN/$\overline{OUT}$ control bit above). However, the EDH_CHKSM flag available on pin FL4 when S[1:0] = 11 is only valid if IN/$\overline{OUT}$ is LOW. Also, the APV and FFV bits available on pins FL[3:2] when S[1:0] = 11 are only valid when IN/$\overline{OUT}$ is HIGH (that is, the validity bits are always read from the incoming EDH packet). The S bit is available regardless of the state of the IN/$\overline{OUT}$ bit.

3.10.3 FLAG PORT Read/Write Timing

Figure 12a shows a FLAG PORT write cycle followed by a FLAG PORT read cycle and illustrates the read/write timing requirements. Note that the signals are not latched in exactly on the rising edge of PLCKOUT (as described in Note 2 of the AC electrical table), but are shown as being latched in on the rising edge for simplicity only.

A write cycle is initiated by changing the F_R/$\overline{W}$ signal from HIGH to LOW. The first time the device samples the F_R/$\overline{W}$ LOW (at t_0) it is instructed to stop driving the FL[4:0] pins. On each subsequent clock cycle (and F_R/$\overline{W}$ LOW) the device latches in the data present on S[1:0] and FL[4:0] (at t_1, t_2, t_3 and t_4). In this example, the S[1:0] pins begin at "00" and are incremented each clock cycle to update all the error flags, validity bits, and the IN/$\overline{OUT}$ control bit. Note that if a write cycle is performed to update, say the FF error flags (S[1:0] = 00), only the FF flags are updated, and the others are unaffected.

A delay time, t_{FDIS}, is necessary to change the FL[4:0] pins from output mode to input mode as defined in the AC timing table and shown in Figure 12b.

The external controller can begin to drive the FL[4:0] bus after this delay time. A simple way to allow for this is to wait one clock cycle before starting to drive the FL[4:0] port and thus prevent bus contention (but set the S[1:0] inputs when F_R/$\overline{W}$ goes LOW so that flags are not unintentionally affected).

At t_5, the F_R/$\overline{W}$ pin is sampled HIGH, indicating a read operation. Also at this time, the device reads in the information on the S[1:0] pins. Upon sampling a read operation, the device will begin driving the FLAG PORT after a delay, t_{FEN} (see Figure 12c), with invalid data. The requested information is output on the FL[4:0] pins on the subsequent clock, t_6, (plus an output delay time, see AC timing table and Figure 3). That is, there is a one clock latency between sampling of the S[1:0] pins and when the corresponding output information is presented on the FL[4:0] pins. In this example, the S[1:0] pins begin at "00" and are incremented each clock cycle to read all the error flags, EDH_CHKSM, validity, and S bits.

The FLAG PORT is synchronous to the internal parallel clock and hence adequate timing for writing must be provided as indicated in the AC timing information and Figure 2. FLAG PORT read/write cycles, relative to the data stream, should take place as outlined in section 5.3 (HOST INTERFACE READ/WRITE TIMING).

3.11 CRC_MODE and FLAG_MAP Mode

PIN	LOGIC OPR	HOST BIT
CRC_MODE FLAG_MAP	OR	FLAG_MAP

A common configuration is to have an input EDH chip that checks for errors at the input of a piece of equipment, followed by a processing block that manipulates the data, followed by an output EDH chip that updates the CRC values in the EDH packet before the data exits the equipment. Because the processing block changes the data values, the CRC values in the EDH packet no longer represent the data stream. The output EDH chip updates the CRC values to correctly reflect the newly modified data. To prevent the output EDH chip from indicating erroneous CRC errors on each field, the GS9020A has two special modes of operation, CRC_MODE and FLAG_MAP mode.

3.11.1 CRC_MODE

In CRC_MODE, the CRC values in the EDH packet are updated by the chip but the error flags are preserved and unaltered, unless they are overwritten via the HOSTIF or the FLAG PORT. This mode should be used by the output EDH chip to prevent the newly processed data from creating misleading EDH errors due to CRC mismatches. The device is placed in CRC_MODE by asserting the CRC_MODE pin HIGH.

CRC_MODE is applicable when the processing circuitry does not corrupt the EDH packet, as illustrated in Figure 13a. In this configuration, the input EDH chip operates in normal mode while the output EDH chip is in CRC_MODE. In this scenario, the input IC receives the EDH packet and does normal EDH processing.

The output IC updates the EDH packet with new CRC values but passes the EDH flags through unaltered. Because of this, erroneous EDH flag handling by the second EDH chip is not performed.

3.11.2 FLAG_MAP Mode

In FLAG_MAP mode, the FLAG PORT is used to read EDH flags from the GS9020A and write them to another EDH chip. To enable FLAG_MAP mode, the FLAG_MAP mode pin and the F_R/$\overline{W}$ pin must be asserted HIGH (set F_R/$\overline{W}$ at least one cycle ahead of FLAG_MAP). After a delay of t_{FEN}, the FL[4:0] and S[1:0] pins of the FLAG PORT become outputs and can be connected to the chip which you wish the GS9020A to write the FLAG data to. In this mode the GS9020A automatically increments the value of S[1:0] and subsequently displays the appropriate flags on the FL[4:0] port, synchronous to the rising edge of PCLKOUT. This is illustrated in Figure 12d.

Figure 12d displays three properties of the FLAG PORT in FLAG_MAP mode.

First, each data is present on the FLAG PORT for two clock cycles to eliminate any setup time violations that might occur due to clock data skew between chips placed far apart. However, the designer must still ensure that the hold time is satisfied. Second, the S[1:0] pins never cycle to the value of "11" in FLAG_MAP mode since the values contained in the FL[4:0] register when S[1:0] ="11" are not considered EDH flags. Also, the chip cycles S[1:0] in the sequence "01", "00", "10" since this is the order in which the flags are stored and subsequently decoded from the EDH packet. Finally the S[1:0] pins only change value after receipt of an EDH packet and are thus static between packets. During this inter-packet time, the S[1:0] pins display a value of "01" and the FL[4:0] pins display the ANC EDH flags from the preceding EDH packet.

For reliable data output on the FLAG PORT, switching the FLAG_MAP pin when an EDH packet is exiting the device is not advised. Also, if the EDH core is bypassed by asserting the BYPASS_EDH pin HIGH, the flag port will always display zeros. This is because the incoming flags (which will be decoded and written to the HOSTIF table) will not be updated to reflect the condition of the input data, and as a result no outgoing flags will be generated (the FLAG PORT only displays the outgoing EDH flags).

FLAG_MAP mode can be used to write EDH flags to any chip, the most common use being applicable when the processing circuitry following the EDH chip corrupts the EDH packet. In this case, the FLAG_MAP mode can be used to route the EDH flags from an input EDH chip around the processing core and write them to an output EDH chip. In this configuration, the input IC is in FLAG_MAP mode. It receives the EDH packet, does normal EDH processing and transfers the new EDH flags to the output IC. The output IC, which is not in FLAG_MAP mode but is in write mode (FLAG_MAP and F_R/$\overline{W}$ stay LOW) receives these flags as they are written to it by the EDH chip. The output EDH chip then updates the EDH packet with the new CRC values and inserts the preserved EDH flags that have been transferred from the input IC. A diagram of this can be found in Figure 13b.

Because the flags are output as soon as they are decoded, the maximum processing latency supported between the two EDH chips is the number of clock cycles in the shortest field of the standard minus 15 clock cycles.

For example, D1 has one field of 262 x 1716 = 449592 clock cycles, and one field of 263 x 1716 = 451308 clock cycles. Thus the maximum latency for D1 is 449592 - 15 = 449577 clock cycles.

Any additional latency requires that the flags be delayed before they can be piped to the output chip. Since writing to the flag port takes precedence over the HOSTIF writing, if any of the flags need to be forced at the output EDH chip, external logic in the routing path must be added. Alternately, the HOSTIF of the EDH chip can be used to perform any additional flag masking.

3.12 BYPASS_EDH Processing

PIN	LOGIC OPR	HOST BIT
BYPASS_EDH	OR	BYPASS_EDH

EDH processing can be bypassed by asserting the BYPASS_EDH pin or HOSTIF write table bit HIGH. When bypassed, EDH packets pass through the chip unaltered. Overwriting information in the EDH packet via the HOSTIF write table or the FLAG PORT has no effect. Data processing in the chip (as described below) can still occur even if BYPASS_EDH is asserted. In this case, valid incoming error flags can be read via the I^2C or parallel port interface. However, reading outgoing error flags via the host port or the flag port returns values of 0.

4. DATA PROCESSING BLOCK

The GS9020A contains advanced data processing features that can simplify system design requirements. These include:

- TRS Blanking,
- ITU-R-601 Clipping
- Data Blanking,
- TRS Insertion, and
- ANC Header updating

It is important to note that these processing functions occur in the GS9020A in the order listed above.

When implementing applications which use the EDH core (ie. BYPASS_EDH set LOW), TRS blanking, data blanking, and TRS insertion will indicate a downstream FF/AP EDH error when a $3FC_H$-$3FF_H$ input data value is blanked out or overwritten to a value less than $3FB_H$. As such, users may wish to disable data blanking, TRS blanking and TRS insertion by setting the $\overline{\text{BLANK\_EN}}$ pin HIGH, the CLIP_TRS pin LOW, and leaving the corresponding host interface bits at their power-on default values when implementing applications which use the EDH core.

4.1 TRS Blanking

PIN	LOGIC OPR	HOST BIT
		TRS_BLANK

When asserted HIGH, TRS_BLANK (HOSTIF write table) will blank out any incorrectly positioned TRS words with respect to the flywheel. The blanking values used will be appropriate for the detected video standard as described below in the Data Blanking section. When TRS_INSERT is enabled and TRS_BLANK is not, there may be 4 TRSs per line in the outgoing data stream during a standard switch. Similarly, if TRS_BLANK is enabled and TRS_INSERT is not, then there may be 0 TRS per line during a switch. In most applications, these features should be either both enabled or both disabled to maintain only two TRSs per line. TRS blanking will function incorrectly if the flywheel is disabled. Thus if the flywheel is disabled the TRS_BLANK function should be disabled as well.

4.2 ITU-R-601 Clipping

PIN	LOGIC OPR	HOST BIT
		601_CLIP

This feature operates on the active picture portion (as defined in RP165) of the data stream only. When the 601_CLIP bit of the HOSTIF write table is asserted HIGH, the device remaps all reserved data words in the active picture to values compliant with ITU-R-601. That is, 000-003 is clipped to 004 and $3FC_H$-$3FF_H$ is clipped to $3FB_H$.

4.3 Data Blanking

PIN	LOGIC OPR	HOST BIT
$\overline{\text{BLANK\_EN}}$	AND	$\overline{\text{BLANK\_EN}}$

Asserting the $\overline{\text{BLANK\_EN}}$ pin or the corresponding HOSTIF write table bit LOW causes the corresponding input data to be forced to blanking levels. This is a dynamic control allowing the user to individually select which data words are to be blanked. TRS and EDH insertion occurs after data blanking so if all these features are being used, the output data stream continues to have TRS words and EDH packets present, even if the $\overline{\text{BLANK\_EN}}$ is constantly held LOW.

The outgoing EDH packet will contain the correct CRC values for the blanked fields since the CRC values are calculated and inserted just prior to the data exiting the device.

The blanking values in hexi-decimal notation for each standard are as follows:

NTSC/PAL 4:2:2	200 040 200 040 (CB:Y:CR:Y)
NTSC 4fsc	0F0
PAL 4fsc	100
NTSC/PAL 4:4:4:4	040 040 040 040 (B:G:R:A) 200 040 200 040 (CB:Y:CR:A)

Note that the device must first detect the incoming standard in order for the proper blanking values to be inserted.

4.4 TRS Insertion

TRS words, based on the internal flywheel, can be inserted into the outgoing data stream by asserting HIGH the TRS_INSERT bit of the HOSTIF write table. Note that for proper TRS insertion, the incoming standard must be detected and the flywheel synchronized. That is, the GS9020A does NOT provide proper TRS insertion for unformatted video data (video without TRS words).

PIN	LOGIC OPR	HOST BIT
		TRS_INSERT

In the case where the input signal disappears, TRSs will continue to be inserted based on the last detected standard. Further, if a TRS is already in the correct location, it will be overwritten which may have the effect of correcting the TRS-ID word.

TRS insertion will function incorrectly if the flywheel is disabled. Thus if the flywheel is disabled the TRS_INSERT function should be disabled as well.

4.5 Clipping And TRS Blanking/Insertion

PIN	LOGIC OPR	HOST BIT
CLIP_TRS	OR	601_CLIP
		TRS_BLANK
		TRS_INSERT

Asserting the CLIP_TRS pin HIGH turns on three features described above:

ITU-R-601 Clipping,

TRS Blanking, and

TRS Insertion

These three functions can also be turned on individually through the HOSTIF as described above. THE CLIP_TRS pin is logically ORed with each of the three bits from the HOSTIF table. As a result, as long as the CLIP_TRS pin is asserted, these functions cannot be turned off via the HOSTIF.

4.6 Ancillary Header

PIN	LOGIC OPR	HOST BIT
		ANC_HEADER

Updating of the ANC headers can occur to facilitate 8-bit to 10-bit conversion. If the ANC_HEADER bit of the HOSTIF write table is set HIGH, all 3FC-3FF data values corresponding to component ANC headers are remapped to 3FF in the output data stream.

For example, if 8 bit data is input to the device, the ANC header of 00, FF, FF will appear as 000, 3FC, 3FC and will be remapped to 000, 3FF, 3FF by the GS9020A.

5.0 HOST INTERFACE TABLES

PIN	LOGIC OPR	HOST BIT
HOSTIF_MODE		

The HOST INTERFACE TABLES (HOSTIF) refer to memory locations within the GS9020A which store functional information about the device. There are two tables, a write table and read table.

The write table is organized into 15 word locations (each 8 bits wide) as shown in Table 2 and is used to set various configuration/flag bits. The read table is organized into 23 word locations (each 8 bits wide) as shown in Table 3 and is used to read status information from the device.

The HOSTIF tables can be accessed via an I²C (Inter-Integrated Circuit) serial interface or an 8-bit parallel interface. The HOSTIF_MODE pin selects which interface is used. If the HOSTIF_MODE pin is HIGH, the HOSTIF operates in I²C mode. If the HOSTIF_MODE pin is LOW, the HOSTIF operates in parallel mode.

Note that many bits stored in the tables are also available as device pins. Bits in the write table that have a default value of 0 are logically ORed with the corresponding pin. Write table control bits VBLANKS/$\overline{L}$ and $\overline{BLANK\_EN}$, which have a default value of 1, are logically ANDed with the corresponding pin. However, write table control bit ANC_CHKSM, which has a default value of 1, is logically ORed with the corresponding pin. Therefore, to use the ANC_CHKSM pin, the ANC_CHKSM control bit must first be set to 0.

If the HOST interface is not going to be used, the best way to set the related pins is as follows:

HOSTIF_MODE = LOW

$\overline{CS}$ = HIGH

R/$\overline{W}$ = HIGH

A/$\overline{D}$ = DON'T CARE (BUT NOT FLOATING)

P[7:0] = N/C

5.1 I²C Serial Interface

PIN	LOGIC OPR	HOST BIT
SCL		
SDA		
A[2:0]		

The I²C interface consists of a bi-directional serial data pin (SDA) and a serial clock input pin (SCL). In addition, 3 input pins, A[2:0] are provided to assign the chip one of eight possible I²C addresses ($0001A_2A_1A_0$).

During an I²C write operation, the first byte written to the chip (after the device has been addressed) is interpreted as the starting HOSTIF write table address for the communication. The next byte is interpreted as data to be written to this address. The address then automatically increments so that the following bytes are written to subsequent addresses.

When executing a read operation, a write must be performed first to load the starting address. After this, bytes read from the chip will begin at this address and will auto-increment. If the read operation is halted and communication with the chip is later established for another read, the chip will resume reading at the next HOSTIF memory address.

In I²C mode, P[7:5] and A/D must be set LOW while R/W and CS must be set HIGH.

5.2 Parallel Interface

PIN	LOGIC OPR	HOST BIT
P[7:0]		
A/$\overline{D}$		
R/$\overline{W}$		
$\overline{CS}$		

The asynchronous parallel interface consists of an 8-bit multiplexed address/data bus (P[7:0]), a chip select pin ($\overline{CS}$), a read/write pin (R/$\overline{W}$), and an address/data pin (A/$\overline{D}$).

The following should be noted when interfacing to the parallel port:

A) Read/Write cycles via the parallel interface are completely independent and asynchronous to the parallel clock PCLKOUT.

B) Signals are "strobed" into/out of the parallel port on the falling edge of the $\overline{CS}$ signal. Setup and hold times, as defined in the AC timing tables, are relative to this edge and must be met (see Figure 14a)

C) The GS9020A drives the P[7:0] bus when the R/$\overline{W}$ pin is HIGH and the $\overline{CS}$ pin is LOW. At all other times, the P[7:0] port is in a high impedance state. The host interface enable and disable times are shown in Figure 14b and are specified in the AC timing information. In this figure, the rising/falling edges of R/$\overline{W}$ and $\overline{CS}$ are not aligned to illustrate that the state of the P[7:0] I/Os is only a combinatorial function of the R/$\overline{W}$ and $\overline{CS}$ pins.

A write cycle to the parallel interface is shown in Figure 14c. The starting address of the operation is written to the chip by putting the R/$\overline{W}$ pin LOW (indicating write) and the A/D pin high (indicating ADDRESS). At t_0, the falling edge of $\overline{CS}$ strobes in the information. Following this, the A/$\overline{D}$ line should be asserted LOW indicating data. The R/$\overline{W}$ line remains LOW indicating a write operation and at t_1 the data is strobed into the device.

A read example follows the write cycle. Note that the read cycle begins with a write operation to indicate the starting address. At t_2, R/$\overline{W}$ is LOW (indicating write), A/$\overline{D}$ is HIGH (indicating address) and P[7:0] represent the starting address for the read cycle. After sufficient hold time, the microcontroller releases the P[7:0] bus and the R/$\overline{W}$ is asserted HIGH to indicate a read operation. At t_3, the $\overline{CS}$ is asserted low causing the GS9020A to present the required data on the P[7:0] bus.

If two consecutive data read or write operations are performed, the device will automatically increment the address. However, for a completely random-access operation, the address can be specified prior to every data read or write operation.

5.3 Host Interface Read/Write Timing

Figure 15 illustrates valid times for reading/writing information from the HOSTIF tables. It represents two fields of video data entering and exiting the GS9020A. The relative position of the EDH packet in the data stream is also shown. (Note that the EDH packet entering the device at t_0, EDH F0, represents the EDH information from the previous field, FIELD 0).

It is safe to read or write EDH information at least two lines after an EDH packet exits the chip but before the subsequent EDH packet enters the chip. Reading during the time interval shown will show values from EDH F0. Writing during the time interval shown will affect EDH F1.

Note that the above read/write timing should also be observed when reading/writing flag information via the FLAG PORT.

6.0 RESET

PIN	LOGIC OPR	HOST BIT
$\overline{\text{RESET}}$		

Setting the RESET input pin LOW re-initializes the internal control circuitry including returning all HOST interface programming values to their original default values. An internal power-on-reset cell is also present in the device so that device initialization occurs on power-up. Figure 16a illustrates the reset circuitry. The internal power-on reset circuit of the GS9020A is sensitive to the rise time of the power supply, hence an external power on reset chip or board level reset line is strongly recommended. When using this technique, the user must ensure that a minimum pulse width of 100ns is present on the reset line.

In applications where a board-level reset is not available, a circuit similar to figure 16b can be used to ensure correct reset on power-up. The $\overline{\text{RESET}}$ pin will typically take 1.4ms to reach 2.5V on power up, but can take longer for power supplies with slower rise times. A bleed resistor such as the one shown (20k) will assist the capacitor to discharge once power is removed. The user should allow the capacitor to discharge to at least 0.5V before power is reapplied, to permit a full internal reset. The time taken by the $\overline{\text{RESET}}$ pin to reach 0.5V on power down, is dependent upon the fall time of the power supply.

TABLE 2: GS9020A Host Interface Write Table

WRITE Table	ADDRESS	7	6	5	4	3	2	1	0
CONFIGURATION	1	^{0}STICKY IN	^{0}STICKY OUT	^{0}CLR1	^{0}CLR0	^{0}SWITCH FLYW	^{0}FLYWDIS	0	0
	2	0	^{1}VBLANKS/$\overline{\text{L}}$	^{0}STD SEL	^{0}S	^{0}STD3	^{0}STD2	^{0}STD1	^{0}STD0
	3	^{0}601_CLIP	$^{1}\overline{\text{BLANK\_EN}}$	^{0}ANC_HEADER	^{0}BYPASS_EDH	^{0}FLAG_MAP	^{1}ANC_CHKSM	^{0}TRS_INSERT	^{0}TRS_BLANK
OVERWRITE VALUES	4	^{0}FF UES	^{0}FF IDA	1	^{0}FF EDA	^{0}FF EDH	^{0}ANC UES	^{0}ANC IDA	1
	5	^{0}AP UES	^{0}AP IDA	1	^{0}AP EDA	^{0}AP EDH	^{0}AND EDA	^{0}ANC EDH	0
OVERWRITE CONTROL	6	^{0}FF UES	^{0}FF IDA	^{0}FF IDH	^{0}FF EDA	^{0}FF EDH	^{0}ANC UES	^{0}ANC IDA	^{0}ANC IDH
	7	^{0}AP UES	^{0}AP IDA	^{0}AP IDH	^{0}AP EDA	^{0}AP EDH	^{0}ANC EDA	^{0}ANC EDH	0
ERROR SENSITIVITY BITS	8	$^{0}\overline{\text{FF UES}}$	$^{0}\overline{\text{FF IDA}}$	$^{0}\overline{\text{FF IDH}}$	$^{0}\overline{\text{FF EDA}}$	$^{0}\overline{\text{FF EDH}}$	$^{0}\overline{\text{ANC UES}}$	$^{0}\overline{\text{ANC IDA}}$	$^{0}\overline{\text{ANC IDH}}$
	9	$^{0}\overline{\text{AP UES}}$	$^{0}\overline{\text{AP IDA}}$	$^{0}\overline{\text{AP IDH}}$	$^{0}\overline{\text{AP EDA}}$	$^{0}\overline{\text{AP EDH}}$	$^{0}\overline{\text{ANC EDA}}$	$^{0}\overline{\text{ANC EDH}}$	^{1}EDH_CHKSM
RESERVED (OUTGOING)	10	^{0}RW1 B7	^{0}RW1 B6	^{0}RW1 B5	^{0}RW1 B4	^{0}RW1 B3	^{0}RW1 B2	^{0}RW2 B7	^{0}RW2 B6
	11	^{0}RW2 B5	^{0}RW2 B4	^{0}RW2 B3	^{0}RW2 B2	^{0}RW3 B7	^{0}RW3 B6	^{0}RW3 B5	^{0}RW3 B4
	12	^{0}RW3 B3	^{0}RW3 B2	^{0}RW4 B7	^{0}RW4 B6	^{0}RW4 B5	^{0}RW4 B4	^{0}RW4 B3	^{0}RW4 B2
	13	^{0}RW5 B7	^{0}RW5 B6	^{0}RW5 B5	^{0}RW5 B4	^{0}RW5 B3	^{0}RW5 B2	^{0}RW6 B7	^{0}RW6 B6
	14	^{0}RW6 B5	^{0}RW6 B4	^{0}RW6 B3	^{0}RW6 B2	^{0}RW7 B7	^{0}RW7 B6	^{0}RW7 B5	^{0}RW7 B4
	15	^{0}RW7 B3	^{0}RW7 B2	^{0}RO_CTRL	^{1}FFV	^{1}APV	0	0	0

NOTE: 1. Superscripts denote default settings upon reset.

TABLE 3: GS9020A Host Interface Read Table

READ Table	ADDRESS	7	6	5	4	3	2	1	0
CONFIGURATION	1	F2	F1	F0	S	STD3	STD2	STD1	STD0
	2	NO_EDH	EDH_CHKSM	TRS_ERR	FFV	APV	0	0	0
INCOMING ERROR FLAGS	3	FF UES	FF IDA	FF IDH	FF EDA	FF EDH	ANC UES	ANC IDA	ANC IDH
	4	AP UES	AP IDA	AP IDH	AP EDA	AP EDH	ANC EDA	ANC EDH	0
OUTGOING ERROR FLAGS	5	FF UES	FF IDA	FF IDH	FF EDA	FF EDH	ANC UES	ANC IDA	ANC IDH
	6	AP UES	AP IDA	AP IDH	AP EDA	AP EDH	ANC EDA	ANC EDH	0
INCOMING FF CRC	7	b15	b14	b13	b12	b11	b10	b9	b8
	8	b7	b6	b5	b4	b3	b2	b1	b0
OUTGOING FF CRC	9	b15	b14	b13	b12	b11	b10	b9	b8
	10	b7	b6	b5	b4	b3	b2	b1	b0
INCOMING AP CRC	11	b15	b14	b13	b12	b11	b10	b9	b8
	12	b7	b6	b5	b4	b3	b2	b1	b0
OUTGOING AP CRC	13	b15	b14	b13	b12	b11	b10	b9	b8
	14	b7	b6	b5	b4	b3	b2	b1	b0
ERRORED FIELD COUNTER	15	b23	b22	b21	b20	b19	b18	b17	b16
	16	b15	b14	b13	b12	b11	b10	b9	b8
	17	b7	b6	b5	b4	b3	b2	b1	b0
RESERVED WORDS (INCOMING)	18	RW1 B7	RW1 B6	RW1 B5	RW1 B4	RW1 B3	RW1 B2	RW2 B7	RW2 B6
	19	RW2 B5	RW2 B4	RW2 B3	RW2 B2	RW3 B7	RW3 B6	RW3 B5	RW3 B4
	20	RW3 B3	RW3 B2	RW4 B7	RW4 B6	RW4 B5	RW4 B4	RW4 B3	RW4 B2
	21	RW5 B7	RW5 B6	RW5 B5	RW5 B4	RW5 B3	RW5 B2	RW6 B7	RW6 B6
	22	RW6 B5	RW6 B4	RW6 B3	RW6 B2	RW7 B7	RW7 B6	RW7 B5	RW7 B4
	23	RW7 B3	RW7 B2	0	0	0	0	0	0

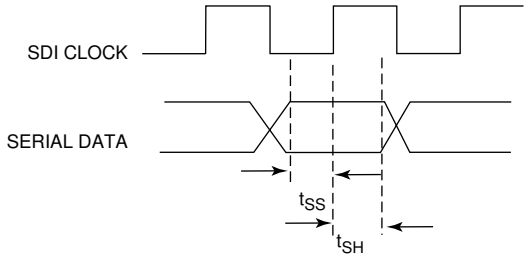


Fig. 1 Serial Data Input Setup & Hold Times

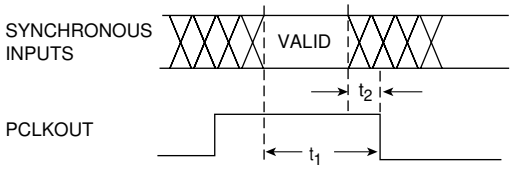


Fig. 2 Input Setup & Hold Times (Synchronous Inputs)

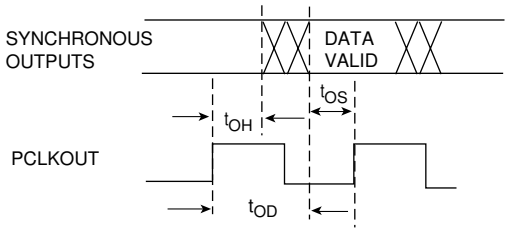


Fig. 3 Output Delay & Hold Times (Synchronous Outputs)

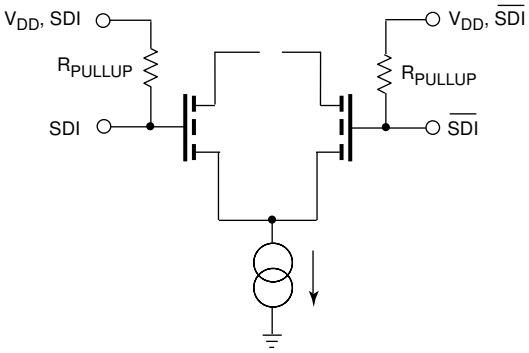


Fig. 4 Serial Data & Clock Input Circuit

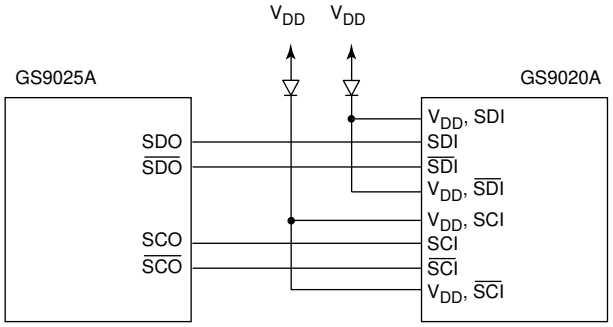


Fig. 5 Interfacing the GS9020A to the GS9025A

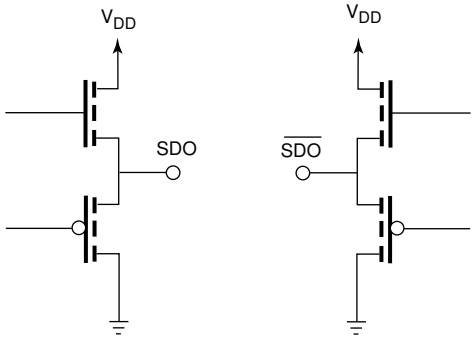


Fig. 6 Serial Data Output Circuit

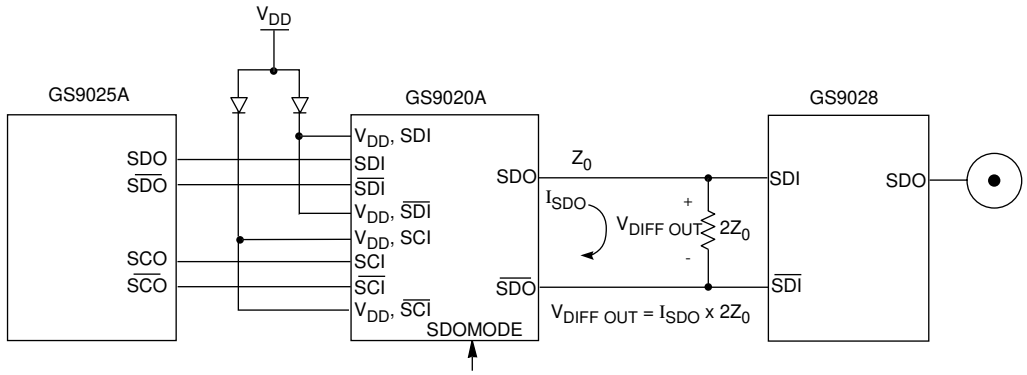


Fig. 7 Interfacing the GS9020A to the GS9028

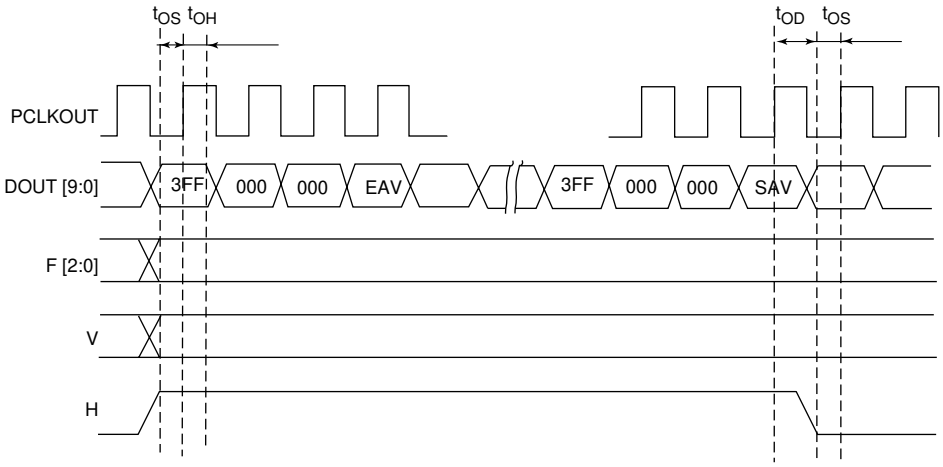


Fig. 8a FVH Timing for Component Video

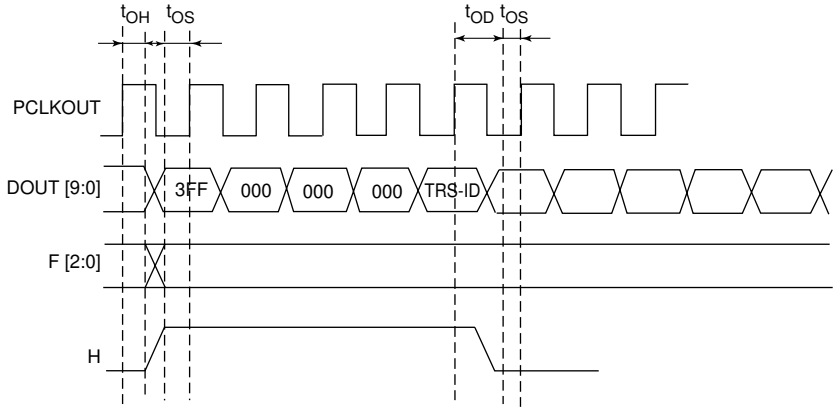


Fig. 8b F and H Timing for Composite Video

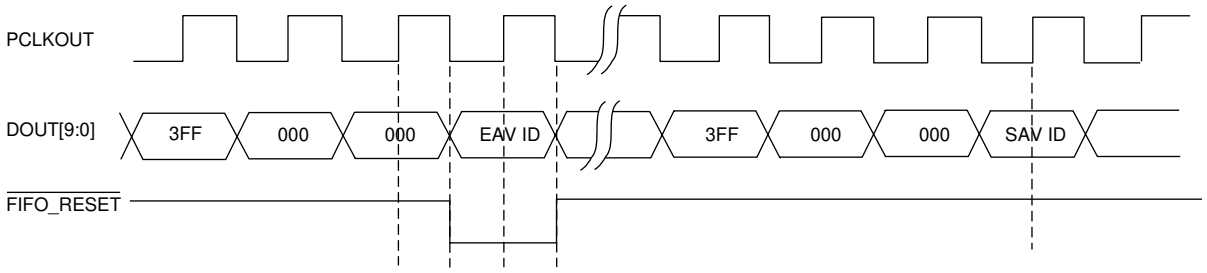


Fig. 9a $\overline{\text{FIFO\_RESET}}$ Pulse Timing for Component Signals (FIFOE/$\overline{\text{S}}$ = 1)

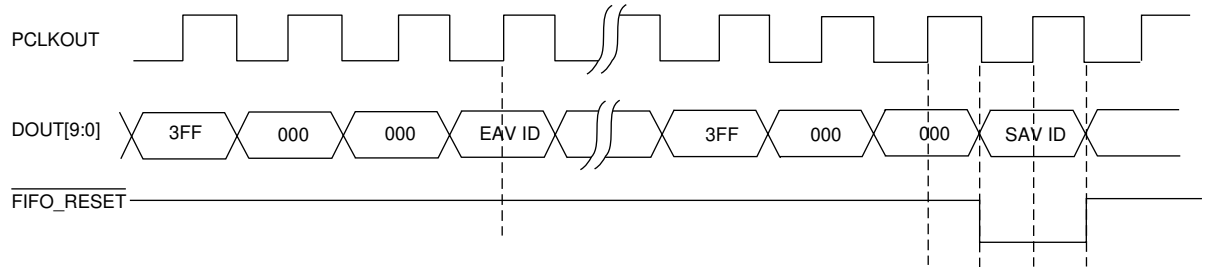


Fig. 9b $\overline{\text{FIFO\_RESET}}$ Pulse Timing for Component Signals (FIFOE/$\overline{\text{S}}$ = 0)

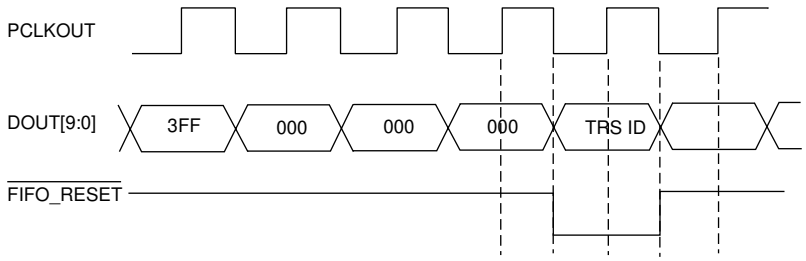


Fig. 9c $\overline{\text{FIFO\_RESET}}$ Pulse Timing for Composite Signals (FIFOE/$\overline{\text{S}}$ = 0 or 1)

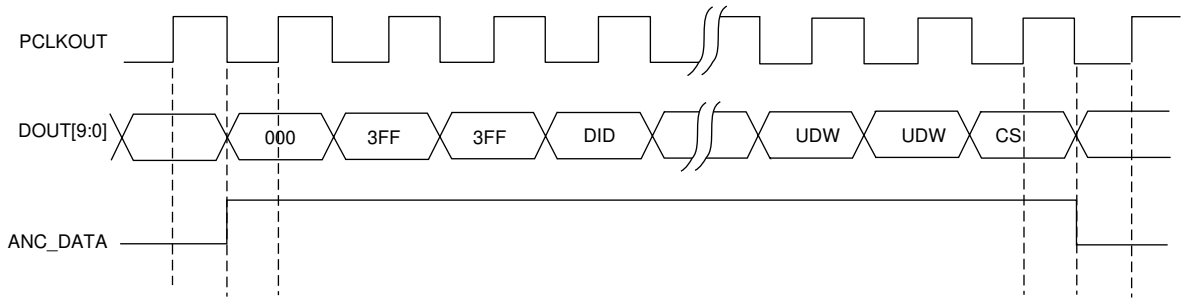


Fig. 10a ANC_DATA Timing for Component Signals

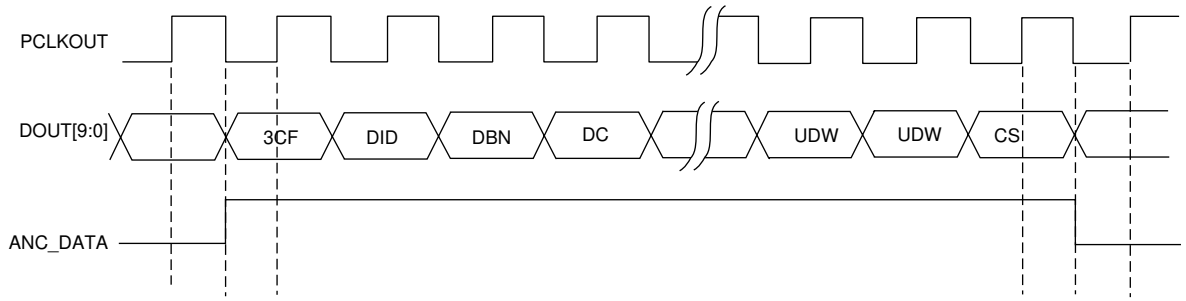


Fig. 10b ANC_DATA Timing for Composite Signals

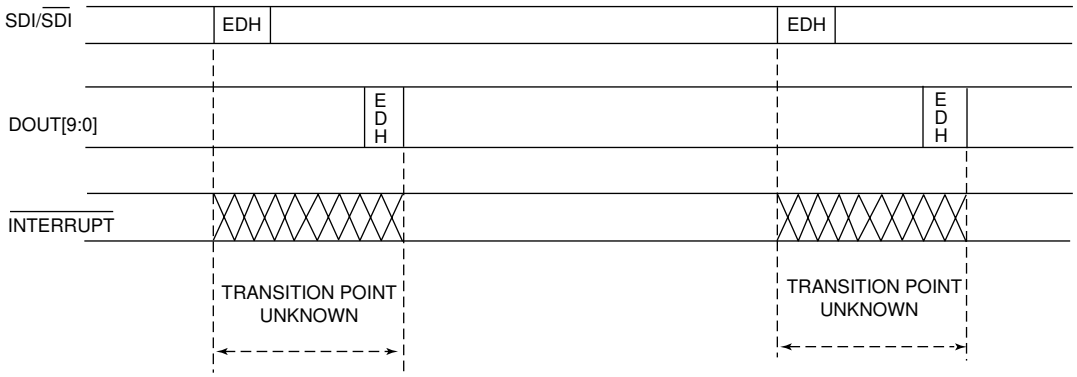


Fig. 11 $\overline{\text{INTERRUPT}}$ Timing