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GENLINX® II GS9023B Embedded Audio CODEC

Key Features

- single chip embedded audio solution
- operates as an embedded audio multiplexer or demultiplexer
- full support for 48kHz synchronous 20/24 bit audio
- 4 channels of audio per GS9023B
- cascadable architecture supports additional audio channels
- multiplexes and demultiplexes arbitrary ANC data packets
- support for 143, 177, 270, 360 and 540 Mb/s video standards
- full processing of audio parity, channel status and user data
- multiplexes and demultiplexes audio control packets
- EDH generation and insertion when in Multiplex Mode
- 3.3V core with 3.3V or 5V I/O (requires 5V supply)
- complies with SMPTE 272M A, B, and C

Applications

SDI Embedded Audio

Brief Description

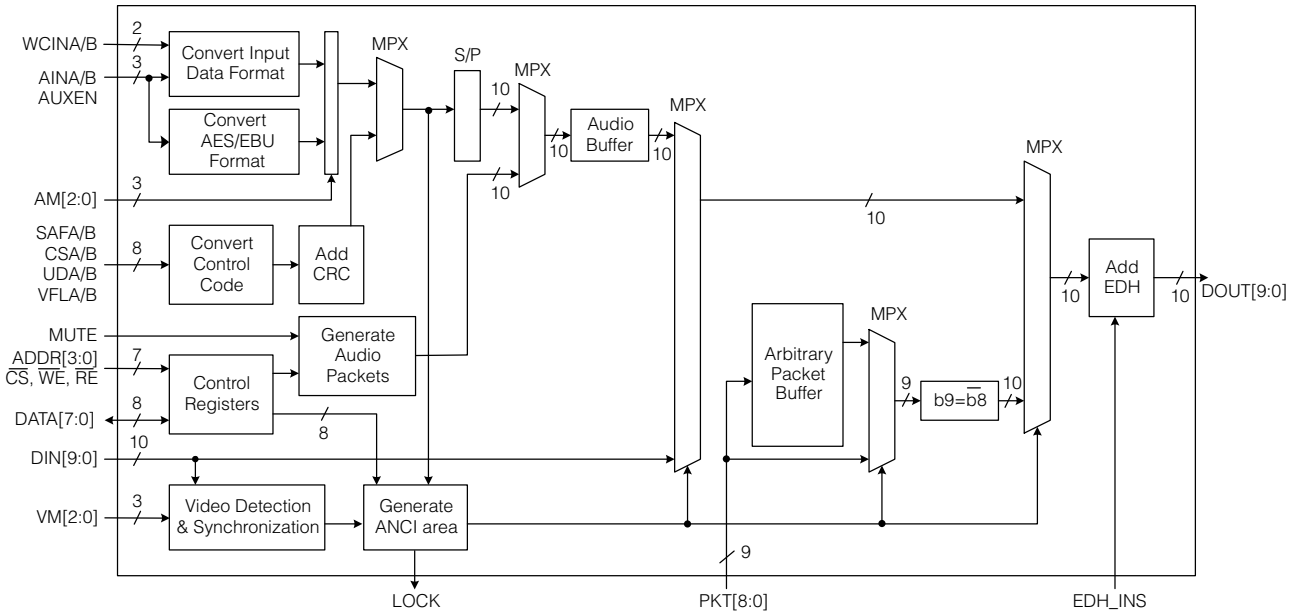
The GS9023B is a highly integrated, single chip solution for the multiplexing/demultiplexing of digital audio channels into and out of digital video signals. The GS9023B supports the multiplexing/demultiplexing of 20 or 24-bit synchronous audio data with a 48kHz sample rate.

Audio signals with different sample rates may be sample rate converted to 48kHz before and after the GS9023B using audio sample rate converters.

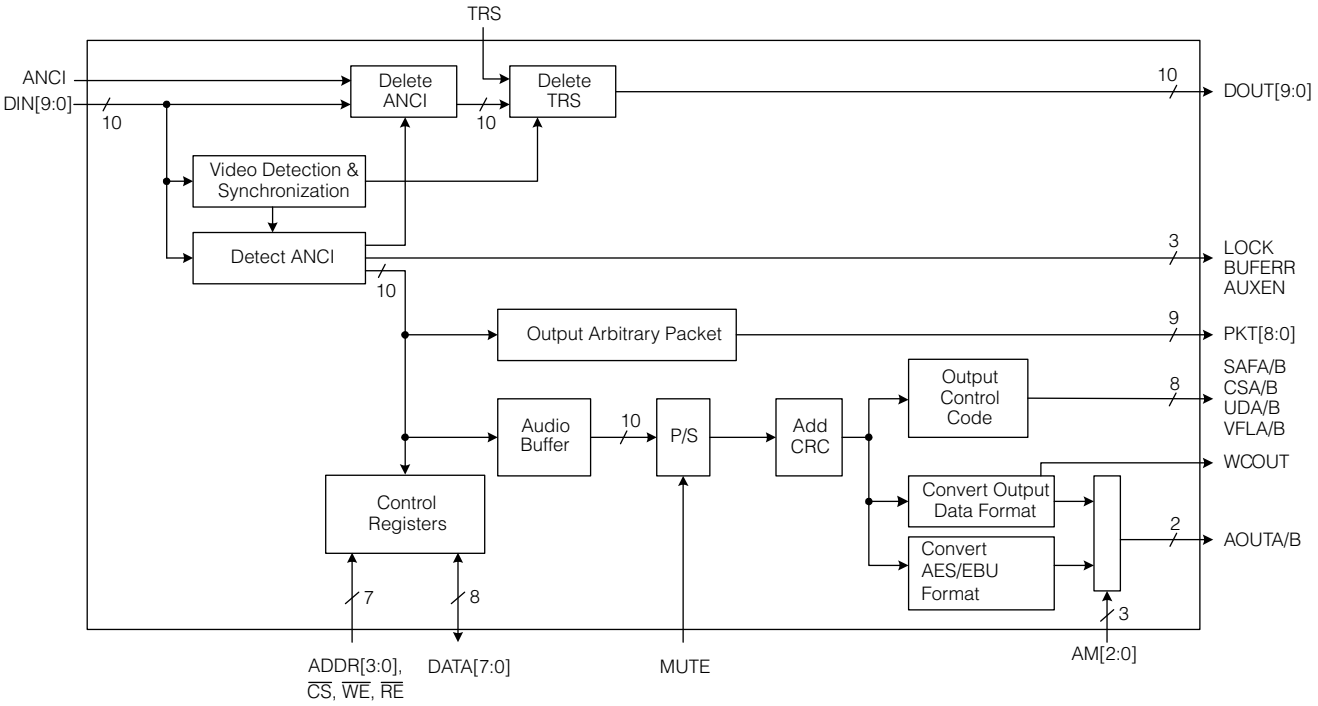
Each GS9023B supports all the processing required to handle the multiplexing/demultiplexing of four digital audio channels. To simplify system design, the GS9023B seamlessly integrates with common AES/EBU digital audio receivers and transmitters. The cascadable architecture allows for the multiplexing/demultiplexing of additional audio channels with no external glue logic.

The GS9023B supports video standards with rates from 143Mb/s to 540Mb/s. When in Multiplex Mode, the GS9023B supports the generation and insertion of EDH information according to SMPTE RP165. In combination with Gennum's GS9032, the GS9023B provides a low power, highly integrated two chip solution for SDI transmit applications. In combination with Gennum's GS7005, the GS9023B provides a low power, highly integrated two chip solution for SDI receive applications.

The GS9023B requires a 3.3V power supply for internal core logic and a 3.3V or 5V power supply for device I/O.



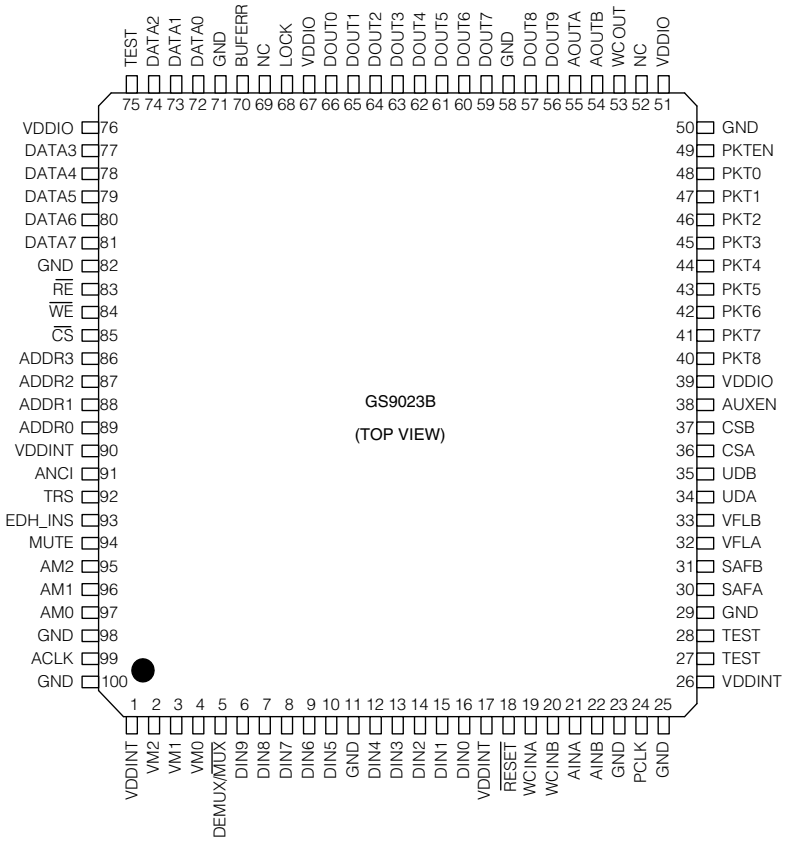
Multiplex Mode Block Diagram



Demultiplex Mode Block Diagram

Contents

1. Pin Connections



NOTE: The GS9023B DOUT[9:0] MSB to LSB convention is compatible with the GS9022 but reversed with the GS9032 or GS7005.
See Interconnection with GS9032 or GS7005 section.

1.1 Pin Descriptions

Table 1-1: Pin Descriptions

Number	Symbol	Type	Description
1, 17, 26, 90	VDDINT		+3.3V power supply pins for core logic.
2-4	VM[2:0]	I	Video standard format. Used in conjunction with the TRS pin. VM[2] is the MSB and VM[0] is the LSB. See Table 3-1.
5	DEMUX/$\overline{\text{MUX}}$	I	Mode of operation. When set HIGH, the GS9023B operates in Demultiplex Mode. When set LOW, the GS9023B operates in Multiplex Mode. NOTE: A device reset must be performed when switching between Multiplex and Demultiplex Modes while the device is powered up.
6-10,12-16	DIN[9:0]	I	Parallel digital video signal input. DIN[9] is the MSB and DIN[0] is the LSB. The digital video input must contain TRS information.

Table 1-1: Pin Descriptions (Continued)

Number	Symbol	Type	Description
11, 23, 25, 29, 50, 58, 71, 82, 98, 100	GND		Device ground.
18	$\overline{\text{RESET}}$	I	Device reset. Active low. NOTE: The video input to output data path will be interrupted during device reset.
19	WCINA	I	48kHz word clock for channels 1 and 2. Used only when operating in Multiplex Mode and when the audio source is not an AES/EBU data stream. This pin should be grounded when inputting AES/EBU digital audio data or when operating in Demultiplex Mode.
20	WCINB	I	48kHz word clock for channels 3 and 4. Used only when operating in Multiplex Mode and when the audio source is not an AES/EBU data stream. This pin should be grounded when inputting AES/EBU digital audio data or when operating in Demultiplex Mode.
21	AINA	I	Audio signal input for channels 1 and 2. AES/EBU digital audio data is bi-phase mark encoded. For all non-AES/EBU input modes, bi-phase mark encoding is not required.
22	AINB	I	Audio signal input for channels 3 and 4. AES/EBU digital audio data is bi-phase mark encoded. For all non-AES/EBU input modes, bi-phase mark encoding is not required.
24	PCLK	I	Video clock signal input.
27, 28, 75	TEST	–	Connect to ground.
30	SAFA	I/O	Start of audio frame indicator for channels 1 and 2. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. SAFA is HIGH for audio frame 0 and LOW for all other audio frames. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023B.
31	SAFB	I/O	Start of audio frame indicator for channels 3 and 4. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. SAFB is set to HIGH for audio frame 0 and LOW for all other audio frames. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023B.
32	VFLA	I/O	Validity flag for channels 1 and 2. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. VFLA is HIGH when audio is invalid and LOW when audio is valid. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023B.
33	VFLB	I/O	Validity flag for channels 3 and 4. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. VFLB is HIGH when audio is invalid and LOW when audio is valid. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023B.
34	UDA	I/O	User data for channels 1 and 2. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023B.

Table 1-1: Pin Descriptions (Continued)

Number	Symbol	Type	Description
35	UDB	I/O	User data for channels 3 and 4. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023B.
36	CSA	I/O	Channel status for channels 1 and 2. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023B.
37	CSB	I/O	Channel status for channels 3 and 4. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023B.
38	AUXEN	I/O	Extended audio enable. When HIGH, the GS9023B processes 24-bit audio samples. When LOW, the GS9023B processes 20-bit samples. In Multiplex Mode, this pin is an input and is supplied by the user. The setting is logical OR with the related A4ON setting in host interface register address 1h. In Demultiplex Mode, this pin is an output and is generated by the GS9023B.
39, 51, 67, 76	VDDIO		+3.3V or +5V power supply pins for device I/Os. In order for device I/O to be +5V tolerant V_{DDIO} must be +5V. Device I/O are not +5V tolerant if V_{DDIO} is +3.3V.
40-48	PKT[8:0]	I/O	Arbitrary data I/O bus. In Multiplex Mode, the user must input the arbitrary data packet words starting from the secondary data identification (SDID) to the last user data word (UDW) according to SMPTE 291M. The GS9023B internally converts the data to 10 bits by generating the inversion bit (bit 9). The checksum (CS) word is also generated internally. In Demultiplex Mode, the GS9023B outputs the arbitrary data packet words starting from the SDID to the last UDW. PKT[8] is the MSB and PKT[0] is the LSB. See Figure 3-11 and Figure 3-16.
49	PKTEN	I/O	Arbitrary data packet enable. In Multiplex Mode, PKTEN must be set HIGH one PCLK cycle before Arbitrary packet data is input to the device. In Demultiplex Mode, the output is set HIGH when outputting Arbitrary packet data. See Figure 3-11 and Figure 3-16.
52, 69	NC	N/A	No Connect. Do not connect these pins.
53	WCOUT	O	48kHz word clock for channels 1, 2, 3 and 4. Valid only when operating in Demultiplex Mode.
54	AOUTB	O	Audio signal output for channels 3 and 4. The AES/EBU digital audio output is bi-phase mark encoded. In all non-AES/EBU modes, the output is not bi-phase mark encoded.
55	AOUTA	O	Audio signal output for channels 1 and 2. The AES/EBU digital audio output is bi-phase mark encoded. In all non-AES/EBU modes, the output is not bi-phase mark encoded.
56, 57, 59-66	DOUT[9:0]	O	Parallel digital video signal output. DOUT[9] is the MSB and DOUT[0] is the LSB.

Table 1-1: Pin Descriptions (Continued)

Number	Symbol	Type	Description
68	LOCK	O	Lock indicator. In Multiplex Mode, when HIGH, the video standard has been identified, the start of a new video frame has been detected and the device is multiplexing audio. NOTE: LOCK will not be set HIGH unless at least one of the audio channel enable bits is HIGH. See "CHACT" description in Table 4-1. In Demultiplex Mode, when HIGH, the video standard has been identified, the 'lock' process selected by "ACTSEL" has been validated and the device is demultiplexing audio. See "ACTSEL" description in Table 4-2. NOTE: LOCK remains active regardless of the number of audio samples in the video stream after 'lock' is achieved.
70	BUFERR	O	Buffer error. Indicates when an internal buffer overflow/underflow error has occurred. Valid only when the device is configured to operate in Demultiplex Mode. NOTE: If an internal buffer overflow/underflow condition occurs, the GS9023B does not mute the audio output.
72-74, 77-81	DATA[0:7]	I/O	Host Interface data bus. DATA[7] is the MSB and DATA[0] is the LSB.
83	$\overline{RE}$	I	Read enable for Host Interface. Active LOW.
84	$\overline{WE}$	I	Write enable for Host Interface. Active LOW.
85	$\overline{CS}$	I	Chip select for Host Interface. Active LOW.
86-89	ADDR[3:0]	I	Host Interface address bus. ADDR[3] is the MSB and ADDR[0] is the LSB.
91	ANCI	I	ANCI Selection. Valid in Demultiplex Mode only. When set HIGH, each ancillary data packet with a DID corresponding to either the audio packet DID, the extended audio packet DID or the arbitrary packet DID is removed from the video signal. The data contained in the packets are output at the corresponding pins. The various DIDs are user programmable in the internal registers and are accessible via the Host Interface. NOTE: When ancillary data packets are deleted, the GS9023B does not recalculate the EDH checkwords. When set LOW, all ancillary data packets remain in the video signal.
92	TRS	I	TRS Selection. Used in conjunction with the VM[2:0] pins to select video standard format. In Multiplex Mode, when the TRS pin is HIGH, TRS is added to a composite video signal. In Demultiplex Mode, when HIGH, TRS is removed from a composite video signal. See Table 3-1.
93	EDH_INS	I	EDH Insert Selection. Valid in Multiplex Mode only. When set HIGH, the GS9023B performs EDH functions according to SMPTE RP165. When set LOW, EDH is not inserted. This setting is logical OR with the related EDHON setting in host interface register address 1h. NOTE: Active picture and full field data words are updated from recalculated values but error flag information is replaced with the values programmed in the internal registers via the Host Interface.
94	MUTE	I	Audio mute. In Multiplex Mode, when set HIGH, the embedded audio packets are forced to '0'. In Demultiplex Mode, when set HIGH, the output data is forced to "0". This setting is logical OR with the related MUTE setting in host interface address 4h.
95-97	AM[2:0]	I	Audio mode format. In Multiplex Mode, AM[2:0] indicates the input audio data format. In Demultiplex Mode, AM[2:0] indicates the output audio data format. AM[2] is the MSB and AM[0] is the LSB. See Table 3-2.

Table 1-1: Pin Descriptions (Continued)

Number	Symbol	Type	Description
99	ACLK	I	Input audio signal clock (128 fs). Synchronous to PCLK. In non-AES/EBU audio modes, the serial audio data is sampled on both edges of ACLK.

NOTE: All unused inputs of the GS9023B should be connected to ground.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
I/O Supply Voltage	-0.3 to 7.0V
Internal Supply Voltage	-0.3 to 4.0V
Input Voltage (any input)	-0.3 to V_{DDIO} + 0.5V
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

T_A = 0°C to 70°C unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
I/O Supply Voltage	V_{DDIO}	5V Operating range	4.75	5.00	5.25	V
I/O Supply Current	I_{DDIO}	V_{DDIO} = 5V; PCLK = 54.0 MHz	–	25	–	mA
I/O Supply Current	I_{DDIO}	V_{DDIO} = 5V; PCLK = 27.0 MHz	–	18	–	mA
I/O Supply Voltage	V_{DDIO}	3.3V Operating range	3.00	3.30	3.60	V
Internal Supply Voltage	V_{DDINT}	–	3.00	3.30	3.60	V
Internal Supply Current	I_{DDINT}	PCLK = 54.0 MHz	–	67	–	mA
Internal Supply Current	I_{DDINT}	PCLK = 27.0 MHz	–	37	–	mA
Input Current	I_{IN}	–	-1	–	1	µA
Hi-Z Output Leakage Current	I_{OZ}	–	-1	–	1	µA
Output Voltage, Logic High	V_{OH}	I_{OH} = -3mA	V_{DDIO} - 0.4	–	–	V
Output Voltage, Logic Low	V_{OL}	I_{OL} = 3mA	–	–	0.4	V
Input Voltage, Logic High	V_{IH}	V_{DDIO} = Max (5.25V or 3.6V)	2.0	–	–	V
Input Voltage, Logic Low	V_{IL}	V_{DDIO} = Min. (4.75V or 3.0V)	–	–	0.8	V
Input Capacitance	C_I	f = 1MHz, V_{DDIO} = 0V	–	–	10	pF

Table 2-1: DC Electrical Characteristics (Continued)

T_A = 0°C to 70°C unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Capacitance	C_O	f = 1MHz, V_{DDIO} = 0V	–	–	10	pF
I/O Capacitance	C_{IO}	f = 1MHz, V_{DDIO} = 0V	–	–	10	pF

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{DDIO} = 5V ± 5%, T_A = 0°C to 70°C unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Video Clock Frequency	–	–	–	–	54	MHz
Video Clock Pulse Width Low	t_{PWL}	–	7.4	–	–	ns
Video Clock Pulse Width High	t_{PWH}	–	7.4	–	–	ns
Video Input Data Setup Time	t_S	–	3	–	–	ns
Video Input Data Hold Time	t_H	–	1	–	–	ns
Video Output Data Delay Time	t_{OD}	with 10 pF loading	–	–	13	ns
Video Output Data Hold Time	t_{OH}	with 10 pF loading	3	–	–	ns
Audio Clock Frequency		–	–	–	6.144	MHz
Audio Input Data Setup Time	t_s	–	3	–	–	ns
Audio Input Data Hold Time	t_H	–	1	–	–	ns
Audio Output Data Hold Time	t_{OH}	with 10pF loading	3	–	–	ns
Audio Output Data Delay Time	t_{OD}	with 10pF loading	–	–	13	ns
Address set up time	t_{AS}	–	3	–	–	ns
Chip select set up time	t_{ACS}	–	3	–	–	ns
Read data access time	t_{GQV}	–	–	–	10	ns
Read data enable time	t_{GQLZ}	–	1	–	–	ns
Read data hold time	t_{RDH}	–	1	–	–	ns
Read pulse width	t_{RD}	–	20	–	–	ns
Read cycle time	t_{RC}	–	30	–	–	ns
Write data set up time	t_{DS}	–	3	–	–	ns
Write data hold time	t_{WDH}	–	1	–	–	ns

Table 2-2: AC Electrical Characteristics (Continued)

V_{DDIO} = 5V ± 5%, T_A = 0°C to 70°C unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Write pulse width	t_{WD}	–	20	–	–	ns
Write cycle time	t_{WC}	–	30	–	–	ns
Reset Pulse Width	t_{RESET}	–	1	–	–	us
Device Latency	–	Multiplexer Mode	13	13	13	PCLKs
	–	Demultiplexer Mode	10	10	10	PCLKs

NOTE: The following signals have the same AC electrical characteristics as the audio inputs and outputs: WCINA, WCINB, SAFA, SAFB, VFLA, VFLB, UDA, UDB, CSA, CSB, WCOUTA, WCOUTB.

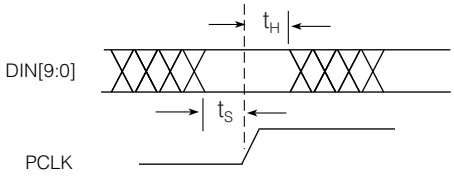


Figure 2-1: Video Data Input Setup & Hold Times

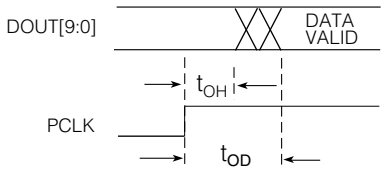


Figure 2-2: Video Data Output Delay & Hold Times

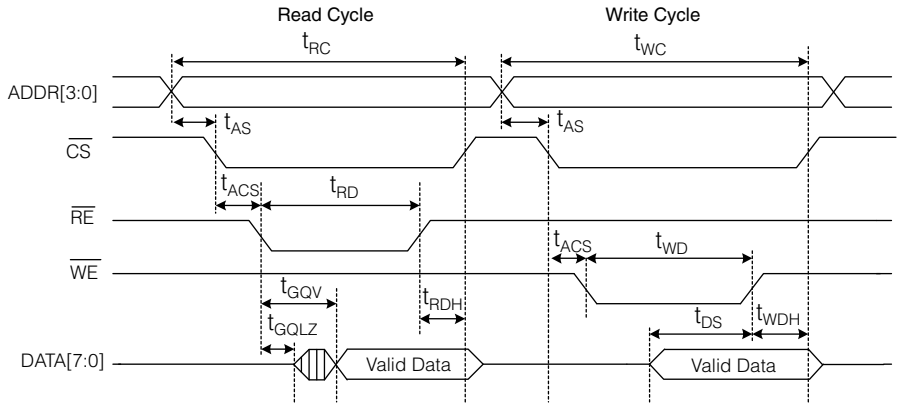


Figure 2-3: Host Interface Timing Diagram

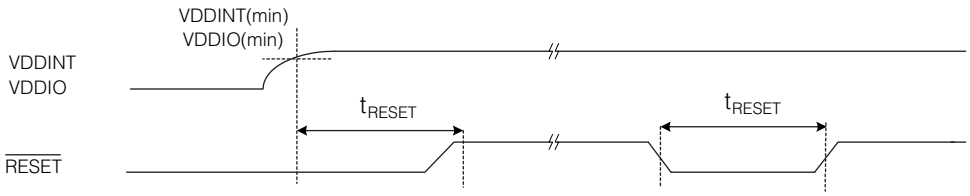


Figure 2-4: Reset Timing Diagram

2.4 Solder Reflow Profiles

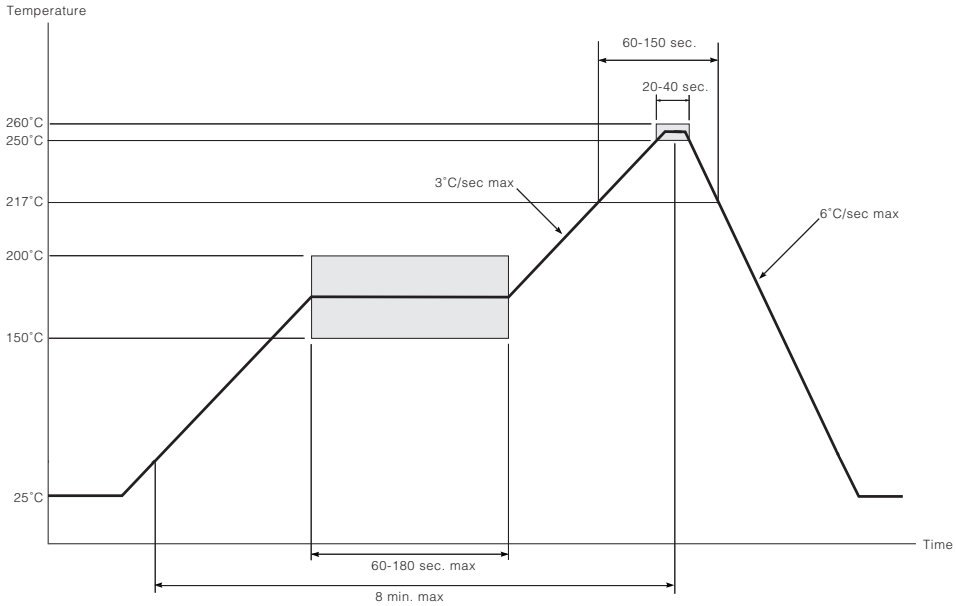


Figure 2-5: Maximum Pb-Free Solder Reflow Profile (Preferred)

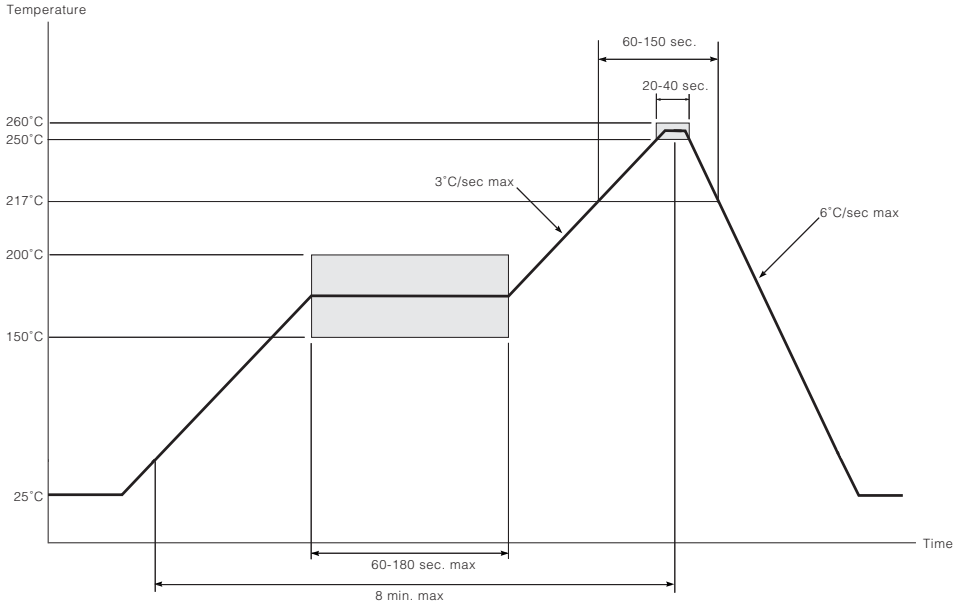


Figure 2-6: Standard Eutectic Solder Reflow Profile

3. Detailed Description

The GS9023B has two main modes of operation: Multiplex Mode and Demultiplex Mode. In Multiplex Mode, which is selected by setting the DEMUX/$\overline{\text{MUX}}$ input pin LOW, digital audio is embedded into a digital video stream. In Demultiplex Mode, which is selected by setting the DEMUX/$\overline{\text{MUX}}$ input pin HIGH, digital audio is extracted from a digital video stream. Table 4-1 and Table 4-2 contain Host Interface Register descriptions for the Multiplex and Demultiplex Modes respectively.

3.1 Multiplex Mode

3.1.1 Video Clock Input

A master video clock must be supplied to the PCLK pin corresponding to the selected video standard. The supported video input standards and corresponding clock frequencies are listed in Table 3-1.

3.1.2 Video Data Input

The video data DIN[9:0] is clocked into the GS9023B on the rising edge of PCLK. The video clock frequency must correspond to the video input standard selected. This is done via the “VSEL” bit of Host Interface Register #0h. When “VSEL” is LOW, the video input standard is selected by the VM[2:0] and TRS input pins. When “VSEL” is HIGH, the video input standard is selected by the “VMOD[2:0]” and “D2_TRS” bits in Host Interface Register #0h. The supported video input standards are listed in Table 3-1.

After the user has specified the video input standard via the VM[2:0] and TRS pins or by setting Host Interface Register #0h, the GS9023B performs video standard detection to verify that the input video stream corresponds to the selected standard. The LOCK output pin and the “LOCK” bit of Host Interface Register #0h are then set HIGH if at least one of the audio channel enable bits “CHACT(4-1)” of Host Interface Register #1h is HIGH and the start of a video frame is detected.

NOTE: The user must ensure that the video input format correctly corresponds to the video format being provided to the GS9023B. For 8-bit video operation, the "8BIT_SEL" bit of the Host Interface Register #2h must be set HIGH.

Table 3-1: Video Input Formats

Video Standard	Serial Digital Data Rate (Mbps)	PCLK Frequency (MHz)	VM[2] or "VMOD[2]"	VM[1] or "VMOD[1]"	VM[0] or "VMOD[0]"	TRS or "D2_TRS"
525/D2 (SMPTE259M)	143	14.3	0	0	0	0
525/D2 (SMPTE244M)	143	14.3	0	0	0	1
525/D1	270	27.0	0	0	1	0
Reserved	–	–	0	0	1	1
525/16:9	360	36.0	0	1	0	0
Reserved	–	–	0	1	0	1
525/4:4:4:4 (System #1)	540	54.0	0	1	1	0
Reserved	–	–	0	1	1	1
625/D2 (with TRS)	177	17.7	1	0	0	0
625/D2 (without TRS)	177	17.7	1	0	0	1
625/D1	270	27.0	1	0	1	0
Reserved	–	–	1	0	1	1
625/16:9	360	36.0	1	1	0	0
Reserved	–	–	1	1	0	1
625/4:4:4:4 (System #2)	540	54.0	1	1	1	0
625/4:2:2P (System #4)	540	54.0	1	1	1	1

3.1.2.1 Synchronous Switch of Video Input

When a 525-line video input to the GS9023B undergoes a synchronous switch between two video sources, the two video sources may have 5-frame sequences which are not aligned. In this case, the GS9023B may not correctly detect the new 5-frame sequence, and the internal FIFO may overflow/underflow continuously. To avoid this problem, it is recommended that the user sets bits 5, 6, and 7 of Host Interface Register #2h HIGH (see bit descriptions in Table 4-1). Setting these bits HIGH will permit the device to reset the internal audio sample buffer when an overflow/underflow condition is detected and mute the embedded audio packets during this reset.

3.1.3 Video Data Output

The video signal is output at the DOUT[9:0] pins. The video signal is synchronized to the rising edge of PCLK. When the GS9023B is properly configured, audio packets, extended audio packets, audio control packets and arbitrary data packets are multiplexed into the output video signal. When the video signal is a 525 line or 625 line D2 format, TRS information is added to the video signal if the TRS input pin or the "D2_TRS" and "VSEL" bits of Host Interface Register #0h are HIGH. EDH packets can also be inserted into the video signal by setting the EDH_INS pin HIGH or by setting the "EDHON" bit HIGH of Host Interface Register #1h. When selected, the GS9023B inserts EDH packets according to SMPTE RP165.

NOTE: Active picture and full field data words are updated from recalculated values but error flag information is replaced with the values programmed in Host Interface Registers #Eh and #Fh.

NOTE: In the 525/4:4:4:4 video standard, EDH packets should not be inserted as this can lead to TRS signal corruption. When EDH packets are not inserted, the "EDHDEL" bit of Host Interface Register #0h controls the deletion of EDH packets. When the "EDHDEL" bit is set LOW, EDH packets are deleted from the incoming video signal. When "EDHDEL" is set HIGH, EDH packets pass through the device unchanged.

NOTE: "EDHDEL" functionality is valid only when the "CASCADE" bit of Host Interface Register #4h is LOW.

3.1.4 Audio Clock Input

A master audio clock (128 fs: 6.144MHz) must be supplied to the ACLK pin. This clock must be synchronized with the video signal input to the GS9023B. An audio word clock must also be supplied (fs: 48kHz) to the WCINA/B pins when using non-AES/EBU audio. The two 48kHz word clocks must also be synchronized to the video signal.

3.1.5 Audio Data Input

The serial audio data for channels 1 and 2 are input to the AINA pin. The serial audio data for channels 3 and 4 are input to the AINB pin. The GS9023B can multiplex 20 or 24 bit audio data samples. When the AUXEN pin or bit "A4ON" of Host Interface Register #1h is HIGH, the device processes 24 bit audio samples. When the AUXEN pin or "A4ON" register bit is LOW, the device processes 20 bit audio samples. On power up, the "A4ON" bit default is LOW.

The GS9023B offers five predefined audio data input formats, selected via the AM[2:0] pins, which are listed in Table 3-2 and illustrated in Figure 3-1. The first four predefined formats relate to non-AES/EBU audio data while the fifth format corresponds to the AES/EBU audio format. The WCINA and WCINB pins should be grounded when inputting AES/EBU audio data as they are not used.

The GS9023B supports muting of the audio data input. Multiplexed audio and extended data packets for all channels are forced to zero when the MUTE pin or "MUTE" bit of Host Interface Register #4h is set HIGH.

When inputting AES/EBU data, the CRC byte and parity bit will be recalculated and inserted automatically.

3.1.6 Control Code Input

When inputting non-AES/EBU audio data, the validity (V), user data (U) and channel status (C) bits of each audio data channel must be input to the corresponding pins (VFLA, VFLB; UDA, UDB; CSA, CSB). The signals must be updated on the rising edge of WCINA/B and remain constant for the entire word clock period (64 ACLK cycles).

When inputting non-AES/EBU audio data, the SAFA and SAFB pins must be high for one frame out of 192 frames received to indicate the start of frame condition.

When inputting AES/EBU audio data, the control code input pins should be grounded as they are not used.

Table 3-2: Audio Input Formats

FORMATS	WCINA/B	AM[2]	AM[1]	AM[0]
AIN-MODE 0	User Supplied	0	0	0
AIN-MODE 1	User Supplied	0	0	1
AIN-MODE 2	User Supplied	0	1	0
AIN-MODE 3	User Supplied	0	1	1
AIN-AES/EBU	Not Used	1	0	0
Not Used	–	1	0	1
Not Used	–	1	1	0
Not Used	–	1	1	1

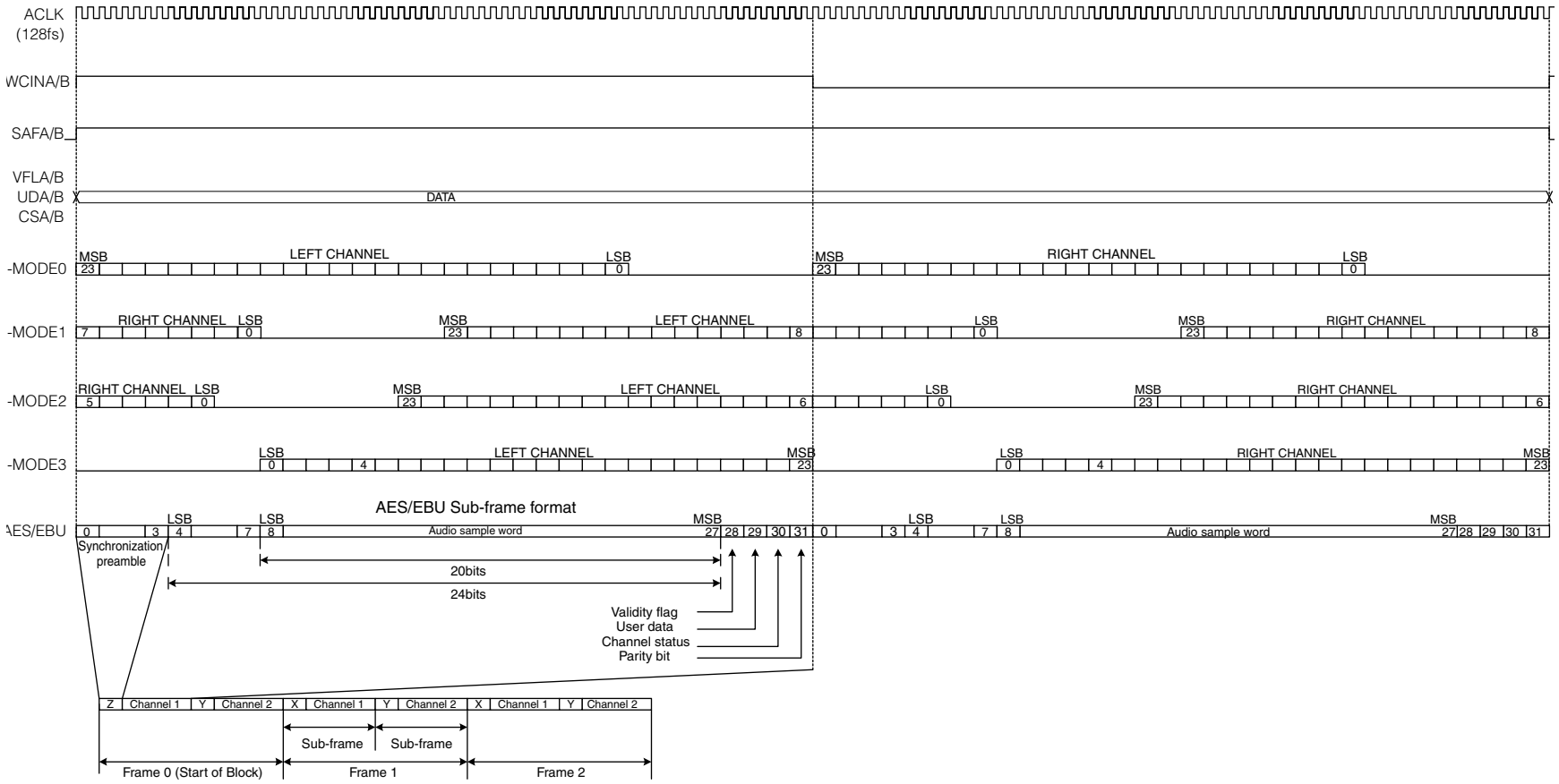


Figure 3-1: Audio Input Format Timing Diagram

3.1.7 Audio Data Packets

The GS9023B can multiplex up to four audio channels. The channels are selectable via the "CHACT(4-1)" bits of Host Interface Register #1h. The audio group (Audio packet data ID) for each device is configured in "AD20ID[3:0]" of Host Interface Register #3h. On power up, the four audio channels and audio group 1 are selected by default.

By setting all the "CHACT(4-1)" bits in Host Interface Register #1h to zero, the GS9023B will be in bypass mode whereby any existing audio data packets, with the same audio group ID or otherwise, will pass through the device unchanged and no new audio data packets will be embedded.

NOTE: Do not rely on default value. Reprogram on power up or reset.

The "CASCADE" bit in Host Interface Register #4h controls the manner in which multiplexing is performed. When "CASCADE" is LOW, the GS9023B deletes all existing ancillary packets. New packets are multiplexed at the first location after the end of active video (EAV) in the horizontal ancillary space (HANC). See Figure 3-2.

When "CASCADE" is HIGH, the GS9023B multiplexes packets at the first free location in the horizontal ancillary (HANC) space after the end of active video (EAV) if there is sufficient space remaining to insert the packet. The GS9023B does not check if existing audio group samples are present in the video signal. Use caution in applications where the video signal contains existing audio packets to avoid adding identical group samples. See Figure 3-3.

The GS9023B assumes that the ancillary space from the first free location is empty to the start of active video (SAV). Existing ancillary data packets (inserted by previous devices) in the video signal must be contiguous from the beginning of the HANC space or the insertion of a new audio data packet may overwrite existing data. See Figure 3-4.

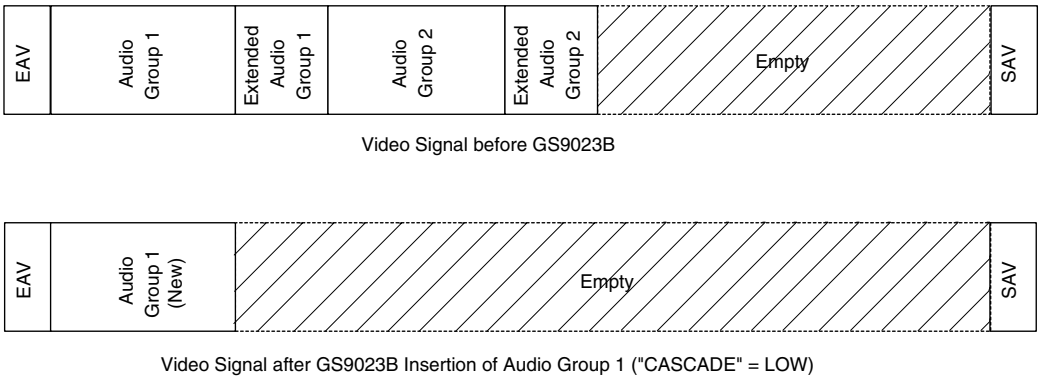


Figure 3-2: Insertion of Audio Group 1, CASCADE=LOW

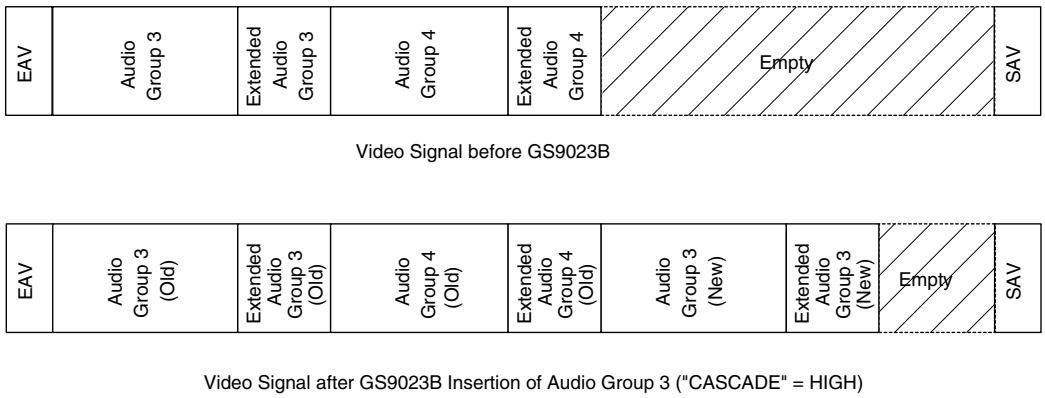


Figure 3-3: Insertion of Audio Group 3, CASCADE=HIGH

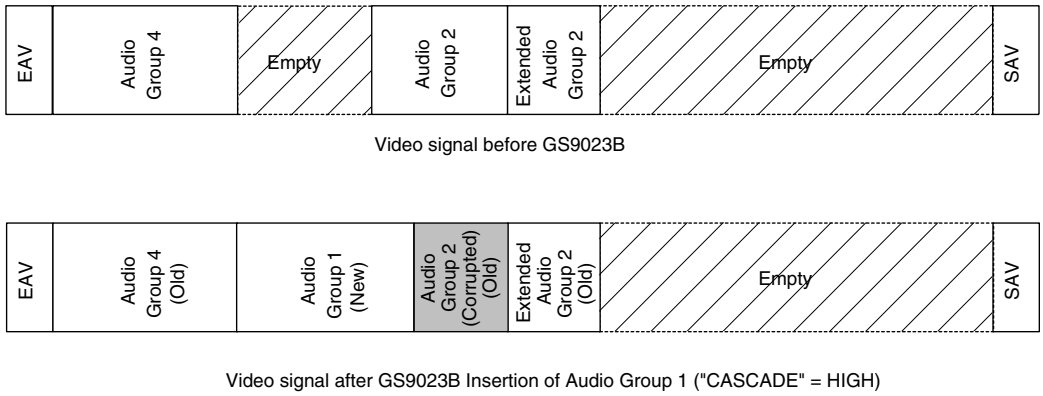


Figure 3-4: Insertion of Audio Group 1, CASCADE=HIGH

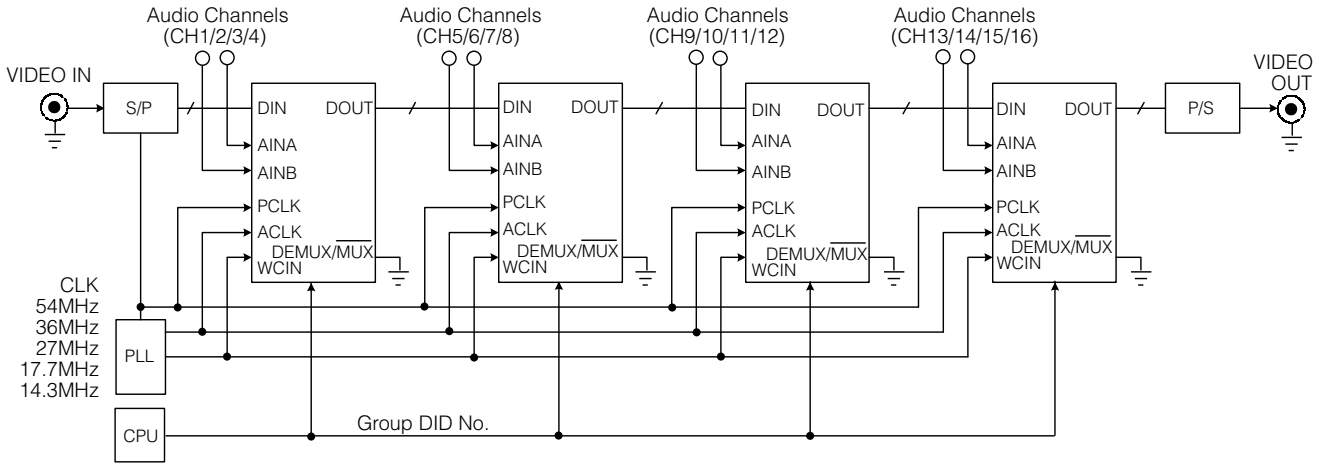


Figure 3-5: Multiplex Mode Cascadable Architecture

In cases where an audio data packet does not fit inside the remaining HANC space, the audio packet is discarded. In this case, the "ADERR" bit of Host Interface Register #7h is HIGH indicating an audio packet multiplexing error. The error bit is cleared once accessed by the Host Interface.

By cascading four GS9023B devices, it is possible to multiplex up to 16 audio channels (according to SMPTE 272) in a component video signal as shown in Figure 3-5.

NOTE 1: In the 525/D1 video format, only 15 channels of 24 bit audio can be multiplexed.

NOTE 2: In cascade mode, audio samples embedded by the first GS9023B may be delayed by up to one audio sample with respect to the audio embedded by cascaded devices.

NOTE 3: When multiplexing audio data into a 525-line video signal at 29.97fps, the GS9023B establishes a 5-frame sequence based on the relationship between the incoming audio and the input video timing. When multiple GS9023Bs are used to multiplex several audio channels, the video signal will undergo a processing delay of 13 video clock cycles through each device. This may affect the timing relationship between the devices such that a different 5-frame sequence may be established in a subsequent GS9023B. For example, Figure 3-6 shows two GS9023Bs cascaded to multiplex eight audio channels. The video signal will be delayed 13 video clock cycles in the first encoder. This timing discrepancy may cause the second GS9023B to establish a different 5-frame sequence from the first.

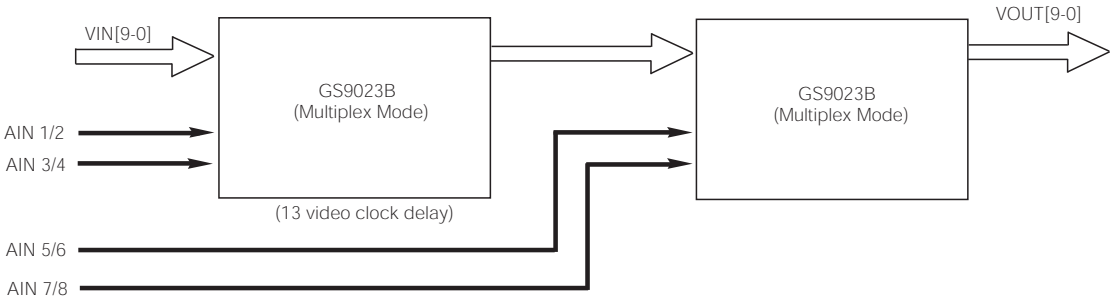
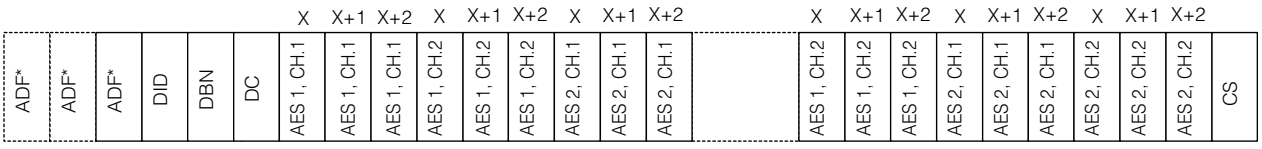


Figure 3-6: Multiplexing 2 Audio Groups using 2 GS9023Bs



* The ancillary data flag, ADF, is one word in composite systems (ANSI/SMPTE 259M) and three words in component systems (ANSI/SMPTE 125M).

Figure 3-7: Audio Data Packet Structure with 4 Audio Channels, 1 Audio Group

Cascade operation is not recommended with a composite video signal, as there is insufficient HANC space for more than four channels of audio. Audio packet insertion is not guaranteed in this case.

The audio data packet structure as described in SMPTE 272M is shown in Figure 3-7.

The audio data packets words are defined as follows:

ADF: Ancillary Data Flag. The ancillary data flag marks the beginning of an ancillary packet and is automatically generated by the GS9023B.

DID: Data ID. Audio data packets corresponding to an audio group are selected by programming "A20ID[3:0]" of Host Interface Register #3h for audio groups 1 to 4 as follows:

Group 1: Fh (2FFh)

Group 2: Dh (1FDh)

Group 3: Bh (1FBh)

Group 4: 9h (2F9h)

NOTE: The six most significant bits of the DID are internally generated by the GS9023B.

DBN: Data Block Number. The data block number is used when data blocks within a common data ID are to be linked or to distinguish consecutive data blocks within a common data ID. The data block number continuously increments from 1 to 255 and is generated automatically by the GS9023B.

DC: Data Count. The data count represents the number of user data words to follow (maximum of 255 words). The data count is automatically generated by the GS9023B.

CS: Checksum. The checksum consists of nine bits. The checksum is used to determine the validity of the words data ID through user data. It is the sum of the nine least significant bits of the words data ID through user data. The checksum is automatically generated by the GS9023B.

The serial audio data samples, are mapped into three contiguous ancillary data words (X, X+1, X+2) as shown in Table 3-3.

Table 3-3: Audio Packet Data Sample Structure

Bit	Word X	Word X+1	Word X+2
b9	not b8	not b8	not b8
b8	aud 5	aud 14	P
b7	aud 4	aud 13	C
b6	aud 3	aud 12	U
b5	aud 2	aud 11	V
b4	aud 1	aud 10	aud 19 (MSB)
b3	aud 0 (LSB)	aud 9	aud 18

Table 3-3: Audio Packet Data Sample Structure (Continued)

Bit	Word X	Word X+1	Word X+2
b2	ch 1 (MSB)	aud 8	aud 17
b1	ch 0 (LSB)	aud 7	aud 16
b0	Z	aud 6	aud 15

Table 3-4: Channel Identification Within The Audio Groups

CH1	CH0	GROUP 1	GROUP 2	GROUP 3	GROUP 4
0	0	Channel 1	Channel 5	Channel 9	Channel 13
0	1	Channel 2	Channel 6	Channel 10	Channel 14
1	0	Channel 3	Channel 7	Channel 11	Channel 15
1	1	Channel 4	Channel 8	Channel 12	Channel 16

The audio packet data sample bits are defined as follows:

Z: The Z flag is set HIGH at the same sample coincident with the beginning of a new AES channel status block (frame 0) and is otherwise set LOW. In non-AES/EBU data input formats this bit is set to the value of the SAFA/B input pins at the rising edge of WCINA/B.

ch[1:0]: Identification of the channels in an audio group as shown in Table 3-4.

aud[19:0]: Twos complement linearly represented audio data. The audio data is input from the AINA and AINB pins.

V: AES/EBU sample validity bit. If the audio sample is valid the bit is set LOW. If the audio sample is invalid, the bit is set HIGH. In non-AES/EBU data input formats, this bit is set to the value of the VFLA/B input pins at the rising edge of WCINA/B.

U: AES/EBU user bit. In non-AES/EBU data input formats, this bit is set to the value of the UDA/B input pins at the rising edge of WCINA/B.

C: AES/EBU audio channel status bit. In non-AES/EBU data input formats this bit is set to the value of the CSA/B input pins at the rising edge of WCINA/B.

P: Even parity for the 26 previous bits in the audio data sample (excludes b9 in the first and second words).

NOTE: The P bit is not the same as the AES/EBU parity bit. This bit is automatically generated by the GS9023B.

3.1.8 Extended Audio Data Packets

The GS9023B can multiplex 20 or 24 bit audio samples. For 24 bit audio samples, the 20 MSBs of a 24 bit audio sample are contained in the audio data packets and the 4 LSBs are contained in an extended audio data packet as defined in SMPTE 272. The extended

audio data packet is multiplexed immediately following the corresponding audio data packet. See Figure 3-8.

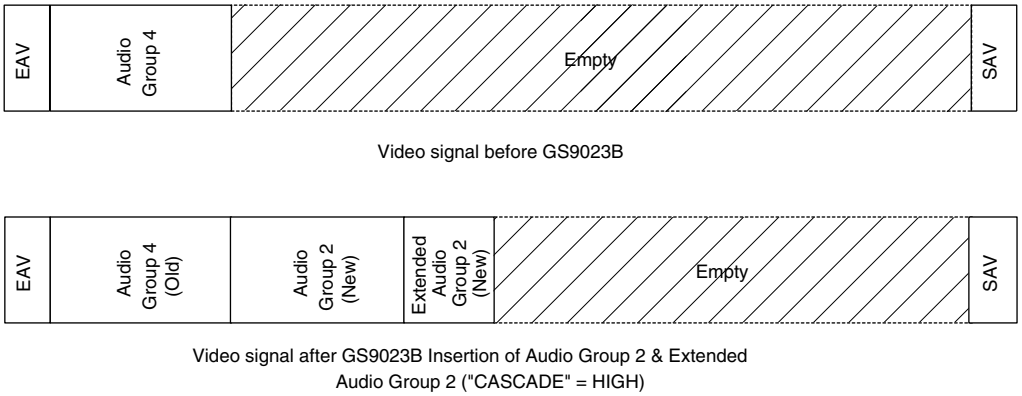


Figure 3-8: Insertion of Audio Group 2 with Extended Audio, CASCADE=HIGH

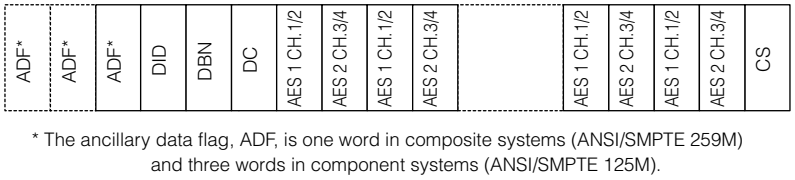


Figure 3-9: Extended Audio Data Packet Structure

To select 24 bit audio operation, the user must set the AUXEN pin or the “A4ON” bit of Host Interface Register #1h HIGH. When the AUXEN pin or “A4ON” bit is HIGH, the GS9023B does not multiplex the audio data packet and the associated extended audio data packet if there is insufficient room for both in the HANC space. In this case, the “ADERR” bit of Host Interface Register #7h is set HIGH, indicating an audio packet multiplexing error. The error bit is cleared when accessed by the Host Interface. The audio group (Extended packet data ID) for each device is configured in “AD4ID[3:0]” of Host Interface Register #3h. On power up, audio group 1 is selected by default.

By cascading four GS9023B devices, it is possible to multiplex up to 16 audio channels (according to SMPTE 272) in a component video signal as shown in Figure 3-5.

NOTE: In the 525/D1 video format, only 15 channels of 24 bit audio can be multiplexed in the cascade configuration.

The extended audio data packet structure as described in SMPTE 272M is shown in Figure 3-9.

The extended audio data packets words are defined as follows:

ADF: Ancillary Data Flag. The ancillary data flag marks the beginning of an ancillary packet and is automatically generated by the GS9023B.