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GENLINX™ II GS9032
Digital Video Serializer

DATA SHEET

GS9032

FEATURES

- **SMPTE 259M and 540Mb/s compliant**
- **serializes 8-bit or 10-bit data**
- **autostandard, adjustment free operation**
- **minimal external components (no loop filter components required)**
- **isolated, quad output, adjustable cable driver**
- **power saving secondary cable driver disable**
- **3.3V and 5.0V CMOS/TTL compatible inputs**
- **lock detect indication**
- **SMPTE scramble and NRZI coding bypass option**
- **EDH support with GS9001, GS9021**
- **Pb-free and RoHS Comliant**

APPLICATION

SMPTE 259M and 540Mb/s parallel to serial interfaces for video cameras, VTRs, and signal generators; generic parallel to serial conversion.

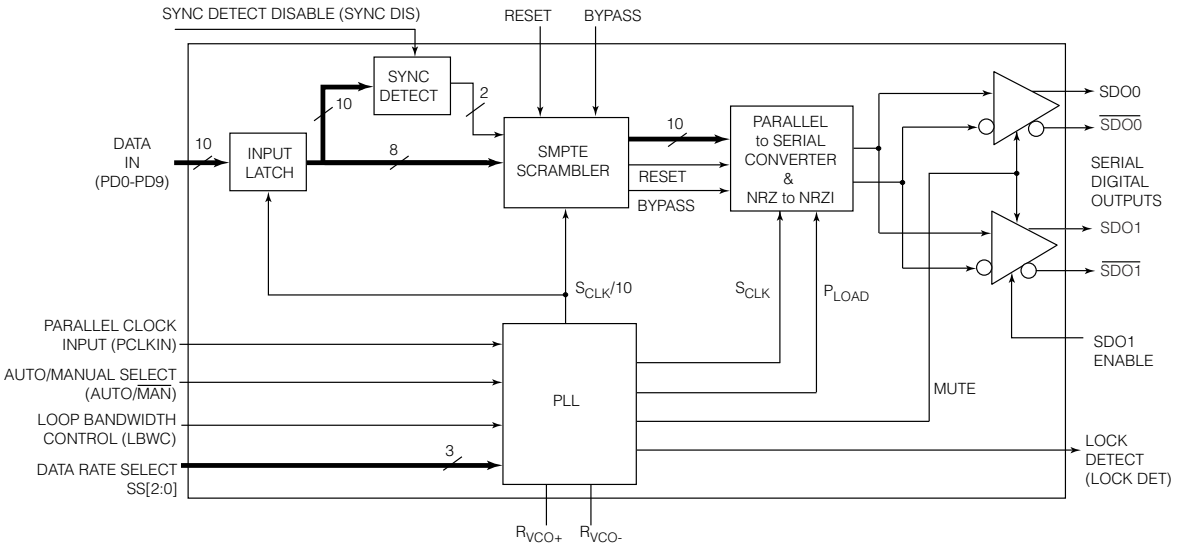
DESCRIPTION

The GS9032 encodes and serializes SMPTE 125M and 244M bit parallel digital video signals, and other 8-bit or 10-bit parallel formats. This device performs sync detection, parallel to serial conversion, data scrambling (using the $X^9 + X^4 + 1$ algorithm), 10x parallel clock multiplication and conversion of NRZ to NRZI serial data. The GS9032 features auto standard and adjustment free operation for data rates to 540Mb/s with a single VCO resistor. Other features include a lock detect output, NRZI encoding, SMPTE scrambler bypass, a sync detect disable, and an isolated quad output cable driver suitable for driving 75Ω loads. The complementary cable driving output swings can be adjusted independently or the secondary differential cable driver can be powered down.

The GS9032 requires a single +5 volt or -5 volt supply and typically consumes 675mW of power while driving four 75Ω loads.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	Pb-FREE AND RoHS COMPLIANT
GS9032 - CVM	44 pin TQFP	0°C to 70°C	No
GS9032 - CTM	44 pin TQFP Tape	0°C to 70°C	No
GS9032 - CVME3	44 pin TQFP	0°C to 70°C	Yes
GS9032 - CTME3	44 pin TQFP Tape	0°C to 70°C	Yes



BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
www.gennum.com

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage ($V_S = V_{CC}$-V_{EE})	5.5V
Input Voltage Range (any input)	$V_{EE}<V_{IN}<V_{CC}$
DC Input Current (any one input)	5mA
Power Dissipation (V_{CC} = 5.25V)	1200mW
$\theta_{j\text{-}a}$	42.5°C/W
$\theta_{j\text{-}c}$	6.4°C/W
Maximum Die Temperature	125°C
Operating Temperature Range	$0°C \le T_A \le 70°C$
Storage Temperature Range	$-65°C \le T_S \le 150°C$
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0° – 70°C unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Positive Supply Voltage	V_{CC}	Operating Range	4.75	5.00	5.25	V		3
Power (System Power)	P	V_{CC} = 5.0V, T = 25°C (4 outputs)	-	675	-	mW		5
Supply Current	I_{CC}	V_{CC} = 5.25V (4 outputs)	-	-	180	mA		1
		V_{CC} = 5.0V, T = 25°C (4 outputs)	-	135	-			3
		V_{CC} = 5.25V (2 outputs)	-	-	160			1
		V_{CC} = 5.0V, T = 25°C (2 outputs)	-	110	-			7
Data & Clock Inputs (PD[9:0] PCLKIN) SYNC DIS	V_{IH}	Logic Input High (wrt V_{EE})	2.4	-	-	V		3
	V_{IL}	Logic Input Low (wrt V_{EE})	-	-	0.8	V		
	I_L	Input Current	-	-	8.0	µA		
Logic Input Levels (Auto/$\overline{\text{Man}}$, SS[2:0] Bypass, RESET)	V_{IH}	Logic Input High (wrt to V_{EE})	2.4	-	-	V		3
	V_{IL}	Logic Input Low (wrt to V_{EE})	-	-	0.8	V		
	I_L	Input Current	-	-	5.0	µA		
Lock Detect Output	V_{OL}	Sinking 500µA	-	-	0.4	V		1

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0° – 70°C unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Serial Data Bit Rate	BR_{SDO}	R_{VCO} = 374Ω	143	-	540	Mb/s	SMPTE 259M	3
Serial Data Outputs Signal Swing	V_{SDO}	R_{LOAD} = 37.5Ω, R_{SET} = 54.9Ω	740	800	860	mVp-p		1
Min. Swing (adjusted)	V_{SDOMIN}	R_{LOAD} = 37.5Ω, R_{SET} = 73.2Ω	-	600	-	mVp-p		7
Max. Swing (adjusted)	V_{SDOMAX}	R_{LOAD} = 37.5Ω, R_{SET} = 43.2Ω	-	1000	-	mVp-p		1
SD Rise/Fall Times	t_r, t_f	20% - 80%	400	-	700	ps		7
SD Overshoot/Undershoot			-	-	7	%	1	7
Output Return Loss	O_{RL}	at 540MHz	15	-	-	dB	1	7
Lock Time	t_{LOCK}	Worst case	-	-	5	ms		6
Min. Loop Bandwidth	BW_{MIN}	270Mb/s LBWC = Grounded : BW_{MIN}	-	220	-	kHz		7
Typical Loop Bandwidth	BW_{TYP}	270Mb/s LBWC = Floating : $\sqrt{10}$ BW_{MIN}	-	500	-	kHz		7
Max. Loop Bandwidth	BW_{MAX}	270Mb/s LBWC = V_{CC} : 10 BW_{MIN}	-	1.7	-	MHz		7
Intrinsic Jitter (6σ)	143Mb/s	LBWC = floating	-	0.07	-	UI		3
	177Mb/s	LBWC = V_{CC}	-	0.07	-			
	270Mb/s		-	0.08	-			
	360Mb/s		-	0.09	-			
	540Mb/s		-	0.11	-			
Data & Clock Inputs (PD[9:0] PCLKIN)	t_{SU}	Setup Time at 25°C	2.5	-	-	ns		3
	t_H	Hold Time at 25°C	2.0	-	-	ns		3

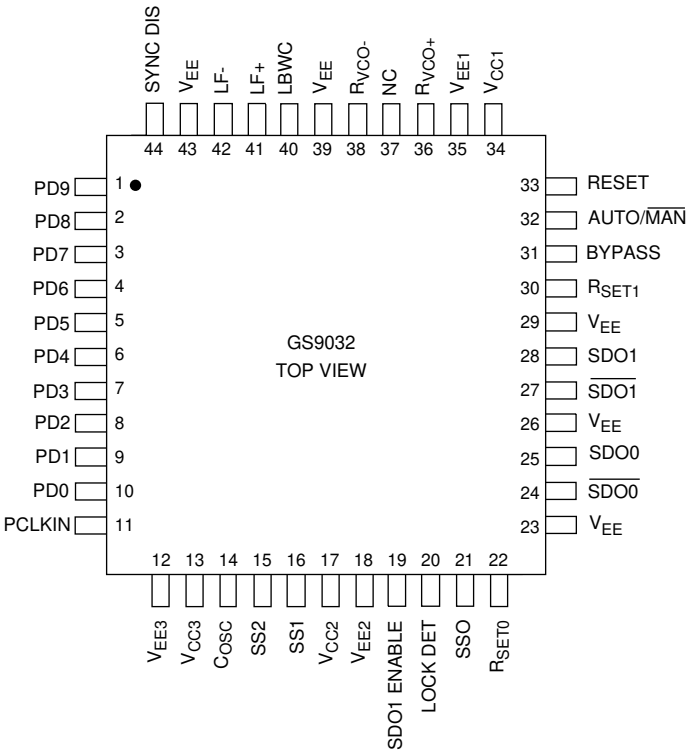
TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

NOTES

1. Depends on PCB layout.

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1-10	PD9 - PD0	I	CMOS or TTL compatible parallel data inputs. PD0 is the LSB and PD9 is the MSB.
11	PCLKIN	I	CMOS or TTL compatible parallel clock input.
12	V_{EE3}	-	Most negative power supply connection for parallel data and clock inputs.
13	V_{CC3}	-	Most positive power supply connection for parallel data and clock inputs.
14	C_{OSC}	I	Master Timer Capacitor. A capacitor should be added to decrease the system clock frequency when an external capacitor is used across LF+ and LF- (NC if not used).
15, 16, 21	SS2, SS1, SS0	I	Data rate selection when in manual mode. These pins are not used in auto mode.
17	V_{CC2}	-	Most positive power supply connection for internal logic and digital circuits.
18	V_{EE2}	-	Most negative power supply connection for internal logic and digital circuits.
19	SDO1 ENABLE	I	Enable pin for the secondary cable driver (SDO1 and $\overline{SDO1}$). Connect to most negative power supply to enable. Leave open to disable (do NOT connect to V_{CC}).
20	LOCK DET	O	TTL level which is high when the internal PLL is locked.
22	R_{SET0}	I	External resistor used to set the data output amplitude for SDO0 and $\overline{SDO0}$.
23, 26, 29	V_{EE}	-	Most negative power supply connection for shielding (not connected).
24, 25	$\overline{SDO0}$, SDO0	O	Primary, current mode, 75Ω cable driving output (inverse and true)
27, 28	$\overline{SDO1}$, SDO1	O	Secondary, current mode, 75Ω cable driving output (inverse and true)
30	R_{SET1}	I	External resistor used to set the data output amplitude for SDO1 and $\overline{SDO1}$.

PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
31	BYPASS	I	When high, the SMPTE Scrambler and NRZ encoder are bypassed.
32	AUTO/$\overline{\text{MAN}}$	I	Autostandard or manual mode selectable operation.
33	RESET	I	Resets the scrambler when asserted.
34	V_{CC1}	-	Most positive power supply connection for analog circuits.
35	V_{EE1}	-	Most negative power supply connection for analog circuits.
36, 38	R_{VCO}+, R_{VCO}-	I	Differential VCO current setting resistor that sets the VCO frequency.
37	NC	I	No Connect.
39, 43	V_{EE}	-	Most negative power supply connection (substrate).
40	LBWC	I	TTL level loop bandwidth control that adjusts the PLL bandwidth to optimize for lowest jitter. If the pin is set to ground the loop bandwidth is BW_{MIN}. If the pin is left floating, the loop bandwidth is approximately 3 BW_{MIN}, if the pin is tied to V_{CC} the loop bandwidth is approximately10 BW_{MIN}
41, 42	LF+, LF-	I	Differential loop filter pins to optimize loop transfer performance at low loop bandwidths (NC if not used).
44	SYNC DIS	I	Sync detect disable. Logic high disables sync detection. Logic low allows 8 bit operation by mapping 000-003 to 000 and 3FC-3FF to 3FF.

TYPICAL PERFORMANCE CURVES (V_S = 5V, T_A = 25°C unless otherwise shown. Guard band tested to 70°C only.)

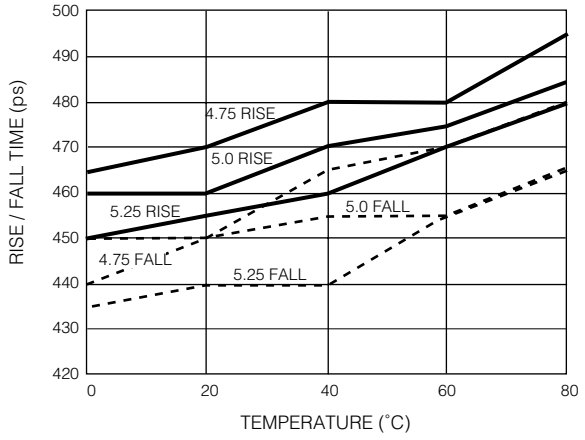


Fig. 1 Rise/Fall Times vs. Temperature

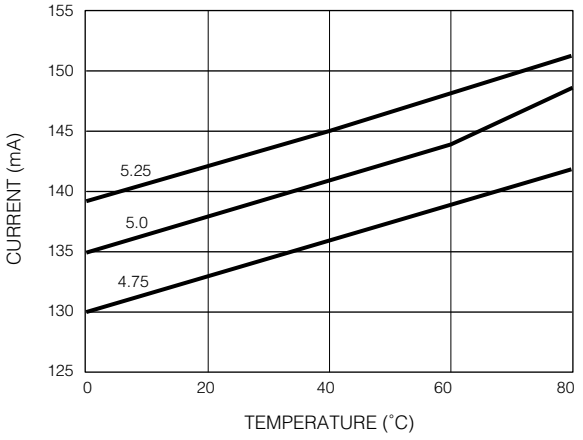


Fig. 2 Supply Current vs. Temperature (SDO0 & SDO1 ON)

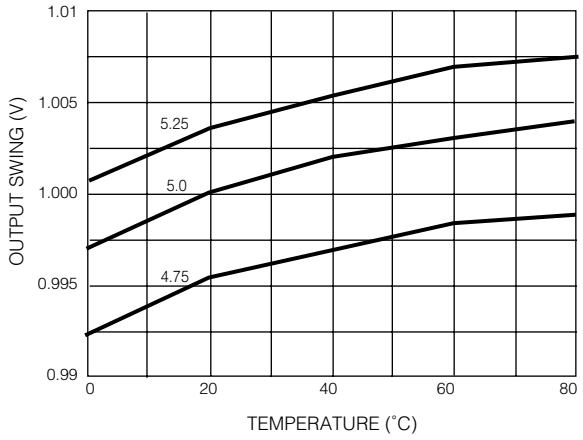


Fig. 3a Output Swing vs. Temperature (1000mV)

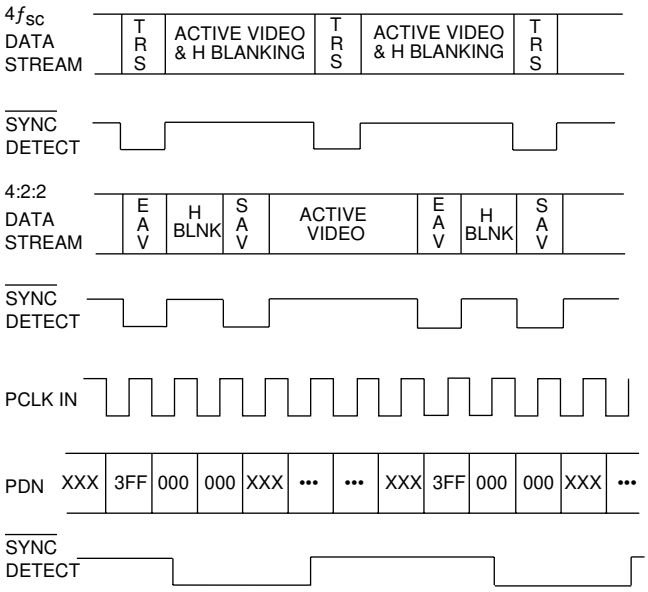


Fig. 5 Timing Diagram

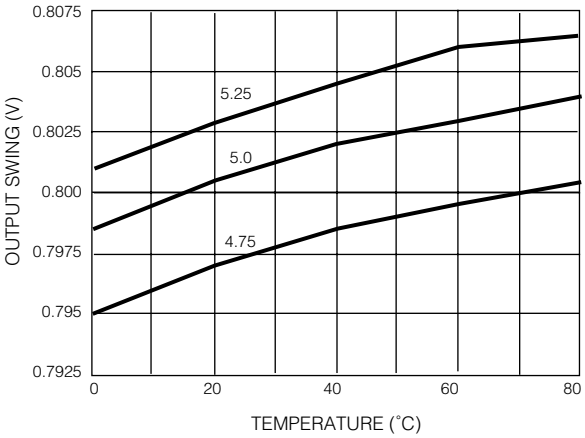


Fig. 3b Output Swing vs. Temperature (800mV)

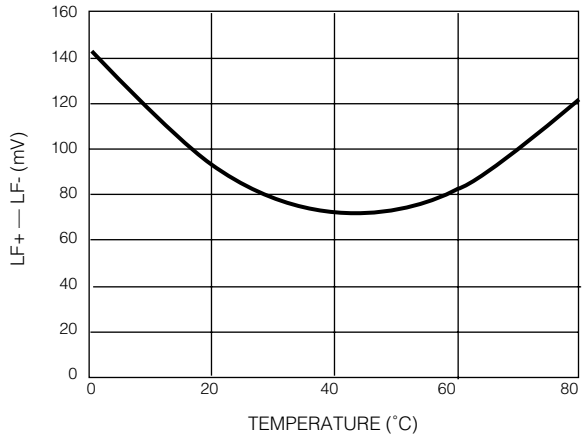


Fig. 6a Loop Filter Voltage vs. Temperature (360 Mode)

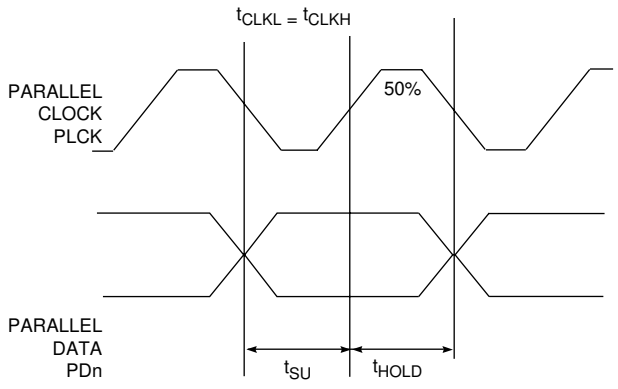


Fig. 4 Waveforms

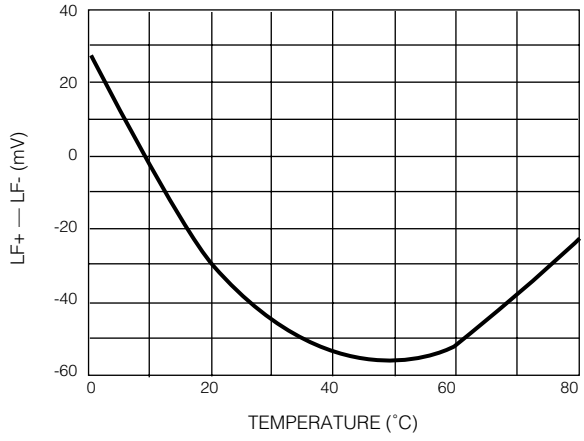


Fig. 6b Loop Filter Voltage vs. Temperature (540 Mode)

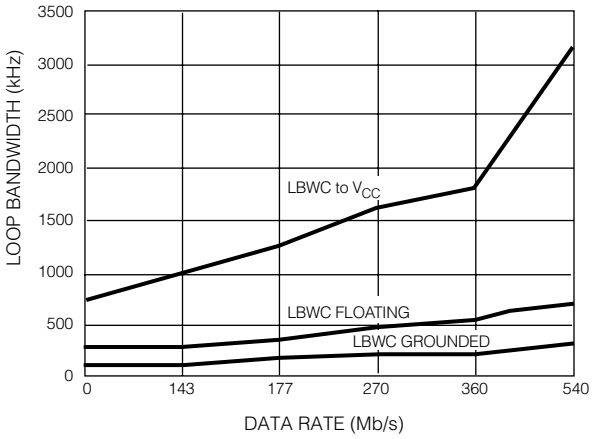


Fig. 7 Loop Bandwidth vs. Data Rate

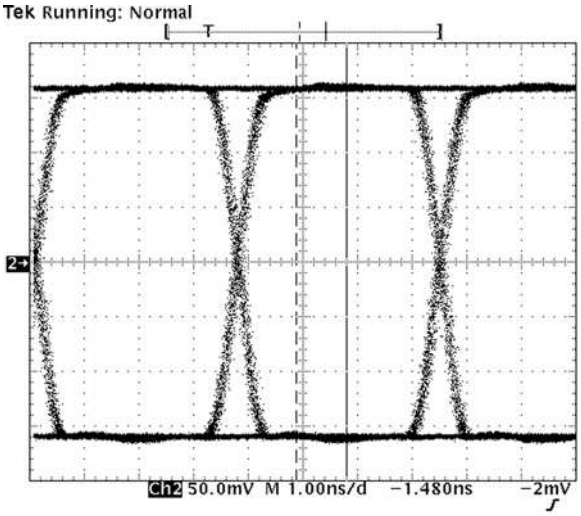


Fig. 10 Output Eye Diagram (270Mb/s)

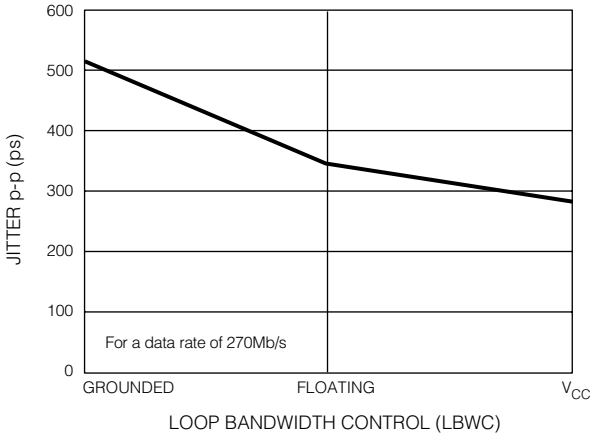


Fig. 8 Output Jitter vs. LBWC

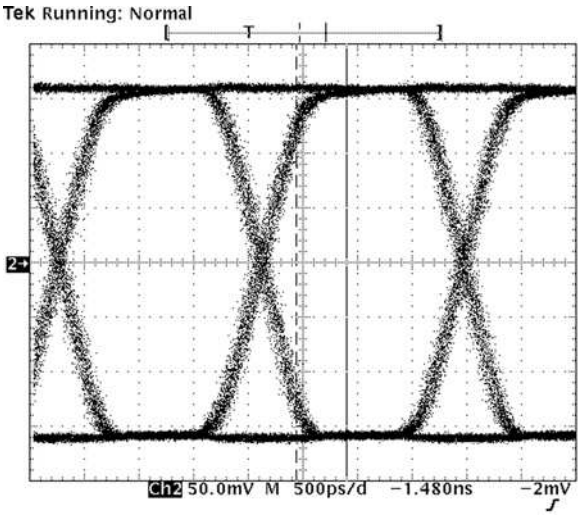


Fig. 11 Output Eye Diagram (540Mb/s)

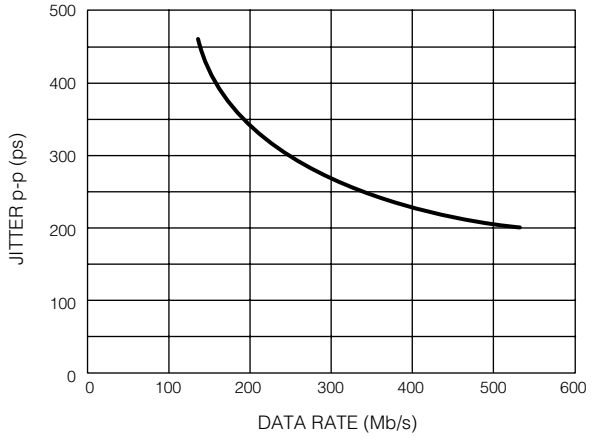


Fig. 9 Output Jitter vs. Data Rate
(Optimum LBW Setting)

DETAILED DESCRIPTION

The GS9032 Serializer is a bipolar integrated circuit used to convert parallel data into a serial format according to the SMPTE 259M standard. The device encodes both eight and ten bit TTL-compatible parallel signals producing serial data rates up to 540Mb/s. It operates from a single five volt supply and is packaged in a 44 pin TQFP.

Functional blocks within the device include the input latches, sync detector, parallel to serial converter, SMPTE scrambler, NRZ to NRZI converter, internal cable driver, PLL for 10x parallel clock multiplication and lock detect. The parallel data (PD0-PD9) and parallel clock (PCLKIN) are applied via pins 1 through 11 respectively.

1. SYNC DETECTOR

The sync detector makes the system compatible with eight or ten bit data. It looks for the reserved words 000-003 and 3FC-3FF in ten bit hexadecimal, or 00 and FF in eight bit hexadecimal, used in the TRS-ID sync word. When the occurrence of either all zeros or all ones at inputs PD2-PD9 is detected, the lower two bits PD0 and PD1 are forced to zeros or ones respectively. For non-SMPTE standard parallel data, the sync detector can be disabled through a logic input, Sync Detect Disable (44).

2. SCRAMBLER

The scrambler is a linear feedback shift register used to pseudo-randomize the incoming serial data according to the fixed polynomial (X^9+X^4+1). This minimizes the DC component in the output serial data stream. The NRZ to NRZI converter uses another polynomial (X+1) to convert a long sequence of ones to a series of transitions, minimizing polarity effects. These functions can be disabled by setting the BYPASS pin (31) high.

3. PHASE LOCKED LOOP

The PLL performs parallel clock multiplication and provides the timing signal for the serializer. It is composed of a phase/frequency detector (with no dead zone), charge pump, VCO, a divide-by-ten counter, and a divide-by-two counter.

The phase/frequency detector allows a wider capture range and faster lock time than with a phase discriminator alone. The discrimination of frequency eliminates harmonic locking. With this type of discriminator, the PLL can be over-damped for good stability without sacrificing lock time.

The charge pump delivers a 'charge packet' to the loop filter which is proportional to the system phase error. Internal voltage clamps are used to constrain the loop filter voltage between approximately 1.8 and 3.4 volts.

The VCO is a differential low phase noise, factory trimmed design that provides increased immunity to PBC noise and precise control of the VCO centre frequency. The VCO can operate in excess of 800MHz and has a pull range of ±15% about the centre frequency. The single external resistor, R_{VCO}, sets the VCO frequency *(see Figure 12)*.

4. VCO CENTRE FREQUENCY SELECTION

For a given R_{VCO} value, the VCO can oscillate at one of two frequencies. When SS0=logic 1, the VCO centre frequency corresponds to the f_L curve. For SS0=logic 0, the VCO centre frequency corresponds to the f_H curve (f_H is approximately 1.5 x f_L).

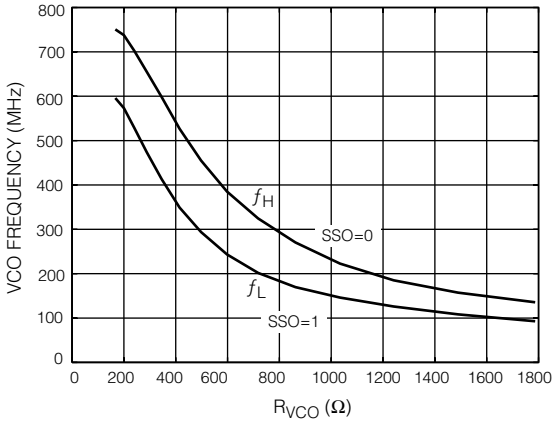


Fig. 12

The recommended R_{VCO} value for auto rate SMPTE 259M applications is 374Ω (*see the Typical Application Circuit*). This value prevents false standards indication in auto mode. For non-SMPTE applications (where data rates are x2 harmonically related) use Figure 12 to determine the R_{VCO} values.

The VCO and an internal divider generate the PLL clock. Divider moduli of 1, 2, and 4 allow the PLL to lock to data rates from 143Mb/s to 540Mb/s. The divider modulus is set by the AUTO/$\overline{\text{MAN}}$, and SS[2:0] pins (*see Truth Table for further details*). In addition, a manually selectable modulus 8 divider allows operation at data rates as low as 18Mb/s when R_{VCO} is increased to 1kΩ.

When the loop is not locked, the lock detect circuit mutes the serial data outputs. When the loop is locked, the Lock Detect output is available from pin 20 and is HIGH.

The true and complement serial data, SDO and $\overline{\text{SDO}}$, are available from pins 24, 25, 27 and 28. These outputs drive four 75Ω co-axial cables with SMPTE level serial digital video signals. To disable the outputs from pins 27 and 28 ($\overline{\text{SDO1}}$, SDO1), remove the resistor connected to the R_{SET1} pin (30) and float the SDO1 ENABLE pin (19).

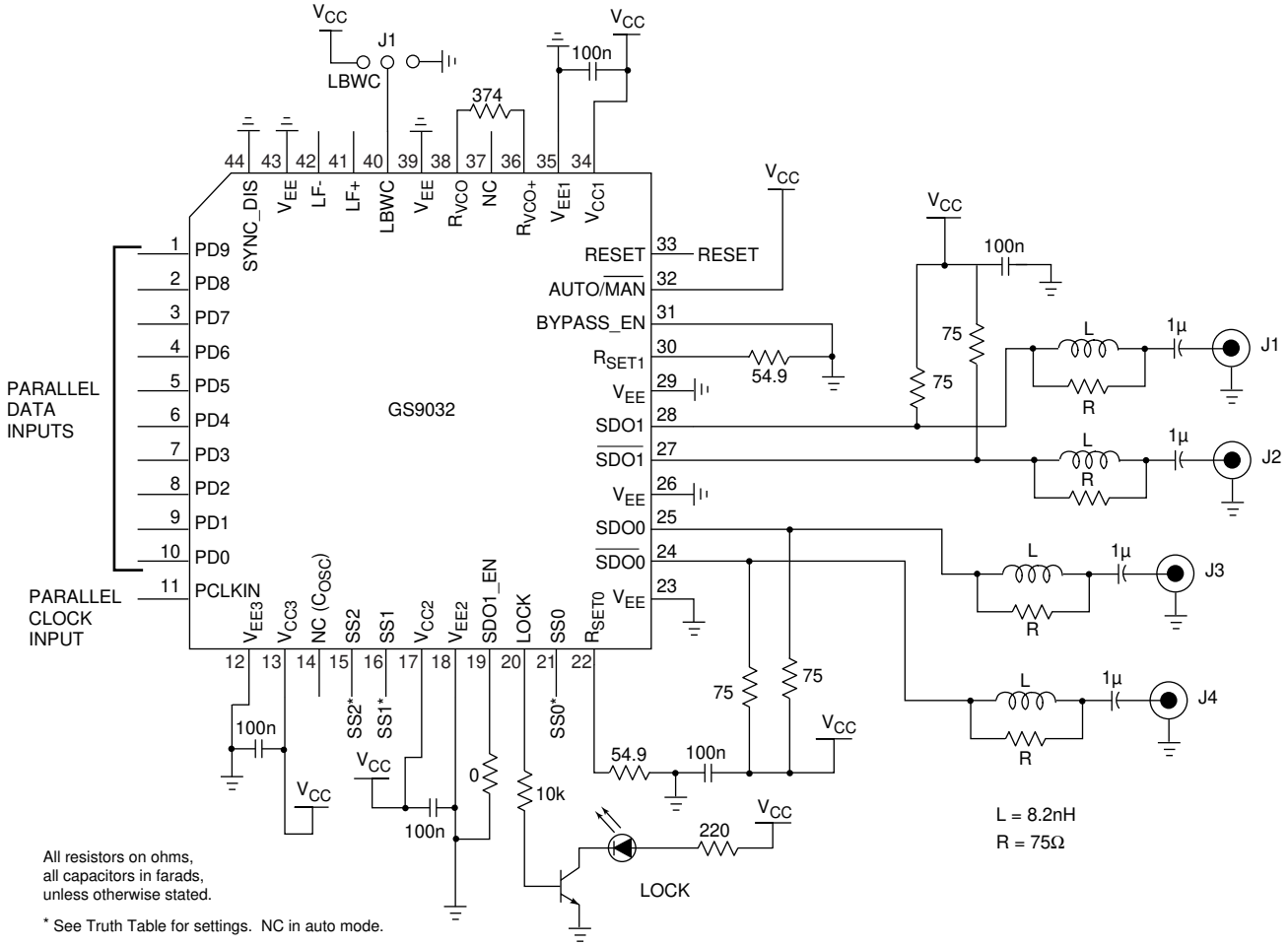
NOTE: Do NOT connect pin 19 to V_{CC}.

R_{SET} calculation:

$$R_{SET} = \frac{1.154 \times R_{LOAD}}{V_{SDO}}$$

where $R_{LOAD} = R_{PULL\text{-}UP} \parallel Z$

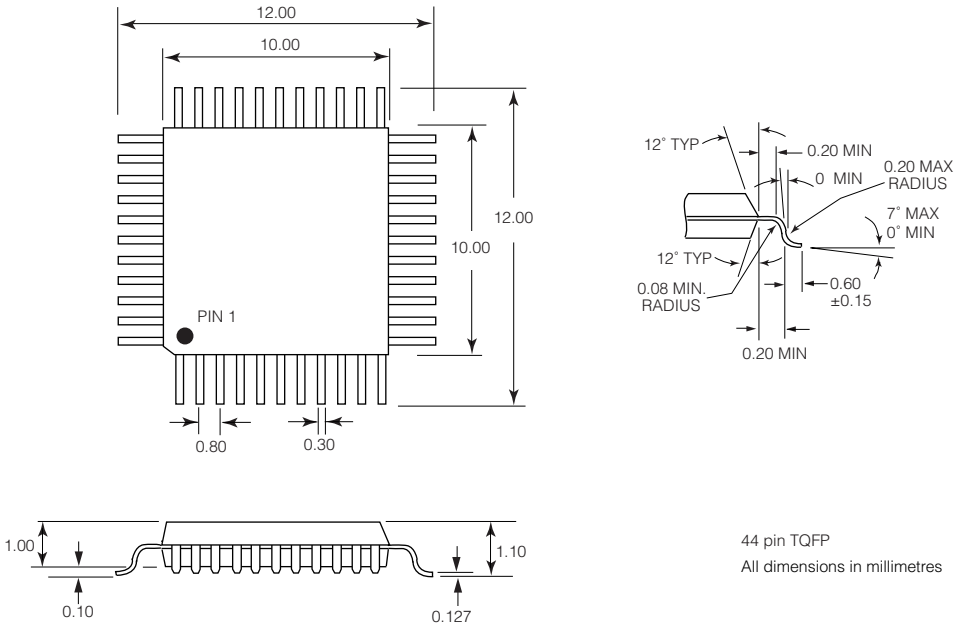
TYPICAL APPLICATION CIRCUIT (SMPTE Auto Mode)



TRUTH TABLE (Manual Mode)

DATA RATE (Mb/s)	SS2	SS1	SS0	DIVIDER MODULI	VCO FREQUENCY
143	0	0	0	4	f_H
177	0	0	1	2	f_L
270	0	1	0	2	f_H
360	0	1	1	1	f_L
540	1	0	0	1	f_H
45	1	0	1	8	f_L
68	1	1	0	8	f_H

PACKAGE DIMENSIONS



44 pin TQFP

All dimensions in millimetres

REVISION HISTORY

VERSION	ECR	DATE	CHANGES AND/OR MODIFICATIONS
9	136657	May 2005	Removed reference to EDH FPGA core. Changed 'Green' references to 'RoHS Compliant'.

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

CAUTION
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SENSITIVE DEVICES

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