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GS9060 HD-LINX® II SD-SDI and DVB-ASI Deserializer with Loop-Through Cable Driver

GS9060 Data Sheet

Key Features

- SMPTE 259M-C compliant descrambling and NRZI → NRZ decoding (with bypass)
- DVB-ASI sync word detection and 8b/10b decoding
- serial loop-through cable driver output selectable as reclocked or non-reclocked
- dual serial digital input buffers with 2 x 1 mux
- integrated serial digital signal termination
- integrated reclocker
- descrambler bypass option
- adjustable loop bandwidth
- user selectable additional processing features including:
  - TRS, ANC data checksum and EDH CRC error detection and correction
  - programmable ANC data detection
  - illegal code remapping
- internal flywheel for noise immune H, V, F extraction
- FIFO load Pulse
- 20-bit / 10-bit CMOS parallel output data bus
- 27MHz / 13.5MHz parallel digital output
- automatic standards detection and indication
- Pb-free and RoHS compliant
- 1.8V core power supply and 3.3V charge pump power supply
- 3.3V digital I/O supply
- JTAG test interface
- small footprint compatible with GS1560A, GS1561, GS1532, and GS9062

Applications

- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS9060 is a reclocking deserializer with a serial loop-through cable driver. When used in conjunction with any Gennum cable equalizer and the GO1555/GO1525* Voltage Controlled Oscillator, a received solution can be realized for SD-SDI and DVB-ASI applications.

In addition to reclocking an deserializing the input data stream, the GS9060 performs NRZI-to-NRZ decoding, descrambling as per SMPTE 259M-C, and word alignment when operating in SMPTE mode. When operating in DVB-ASI mode, the device will word align the data to K28.5 sync characters and 8b/10b decode the received stream.

Two serial digital input buffers are provided with a 2x1 multiplexer to allow the device to select from one of two serial digital input signals.

The integrated reclocker features a very wide Input Jitter Tolerance of ±0.3 UI (total 0.6 UI), a rapid asynchronous lock time, and full compliance with DVB-ASI data streams.

An integrated cable driver is provided for serial input loop-through applications and can be selected to output either buffered or reclocked data. This cable driver also features an output mute on loss of signal, high impedance mode, adjustable signal swing.

The GS9060 also includes a range of data processing functions such as error detection and correction, automatic standards detection, and EDH support. The device can also detect and extract SMTPTE 352M payload identifier packets and independently identify the received video standard. This information is read from internal registers via the host interface port.

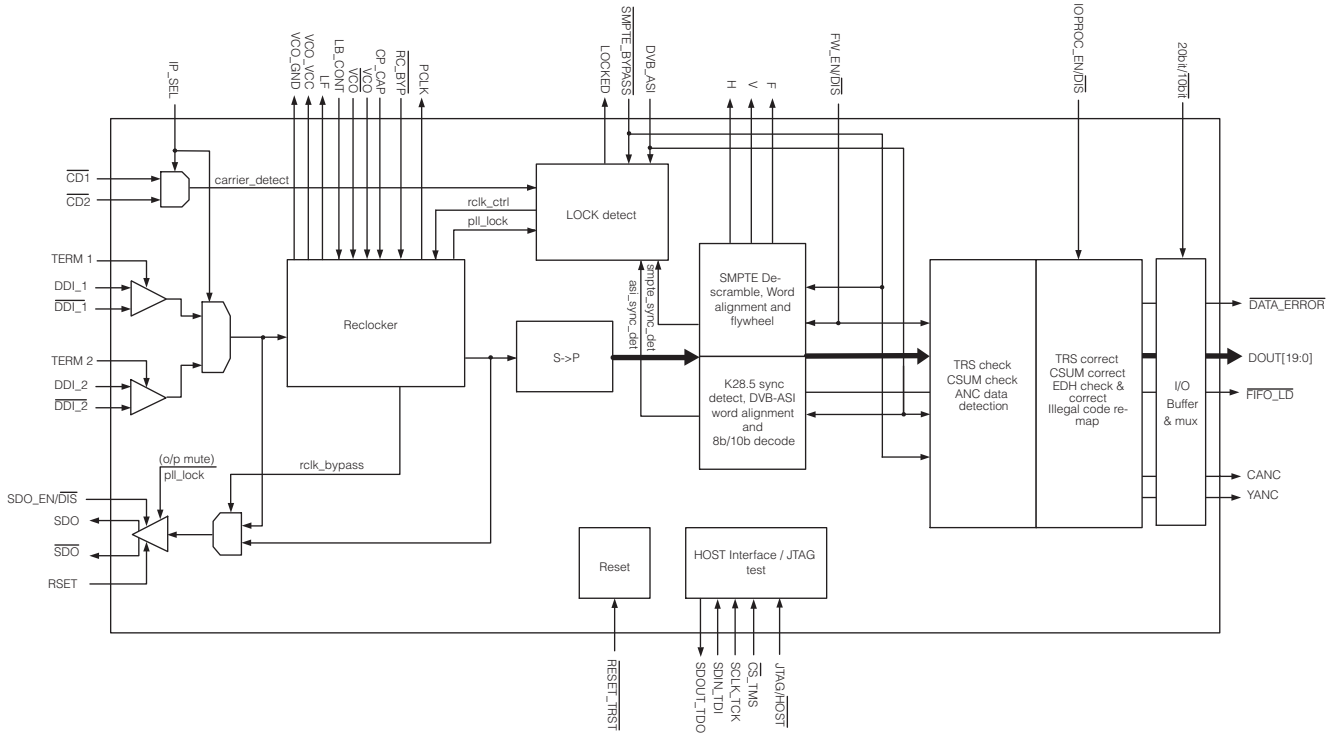
TRS errors, EDH CRC errors and ancillary data checksum errors can all be detected. A single 'DATA_ERROR' pin is provided which is a logical 'ORing' of all detectable errors. Individual error status is stored in internal 'ERROR_STATUS' registers.

Finally the device can correct detected errors and insert new TRS ID words, ancillary data checksum words, and EDH CRC words. Illegal code re-mapping is also available. All processing functions may be individually enabled or disabled via the host interface control.

The GS9060 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant (RoHS compliant).

*For new designs use GO1555

Functional Block Diagram

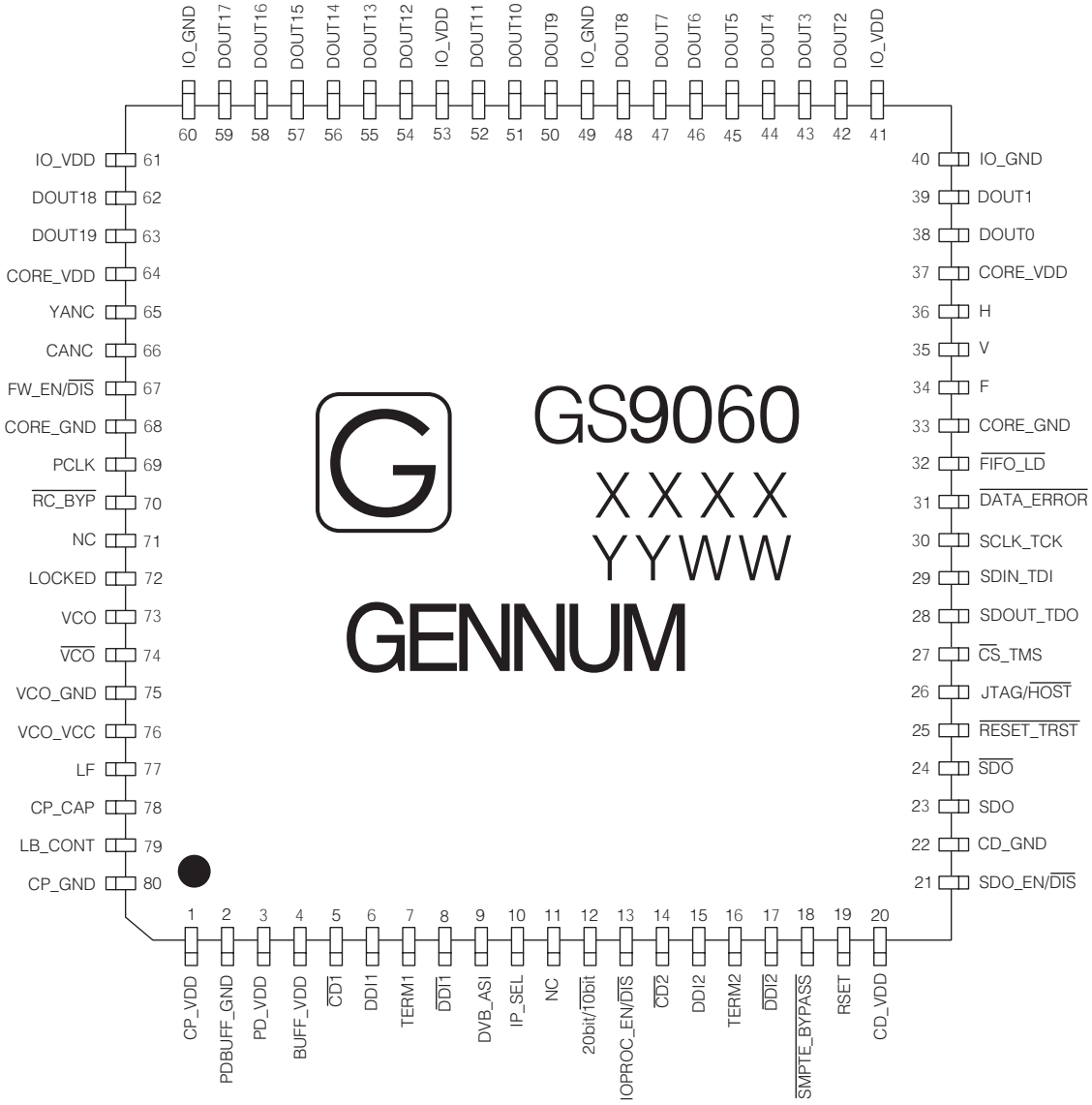


GS9060 Functional Block Diagram

Contents

1. Pin Out

1.1 Pin Assignment



1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	CP_VDD	–	Power	Power supply connection for the charge pump. Connect to +3.3V DC analog.
2	PDBUFF_GND	–	Power	Ground connection for the phase detector and serial digital input buffers. Connect to analog GND.
3	PD_VDD	–	Power	Power supply connection for the phase detector. Connect to +1.8V DC analog.
4	BUFF_VDD	–	Power	Power supply connection for the serial digital input buffers. Connect to +1.8V DC analog.
5	$\overline{CD1}$	Non Synchronous	Input	STATUS SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of a serial digital input signal. Normally generated by a Gennum automatic cable equalizer. When LOW, the serial digital input signal received at the DDI1 and $\overline{DDI1}$ pins is considered valid. When HIGH, the associated serial digital input signal is considered to be invalid. In this case, the LOCKED signal is set LOW and all parallel outputs are muted.
6,8	DDI1, $\overline{DDI1}$	Analog	Input	Differential input pair for serial digital input 1.
7	TERM1	Analog	Input	Termination for serial digital input 1. AC couple to PDBUFF_GND.
9	DVB_ASI	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set HIGH in conjunction with $\overline{SMPTE\_BYPASS}$ = LOW, the device will be configured to operate in DVB-ASI mode. When set LOW, the device will not support the decoding or word alignment of received DVB-ASI data.
10	IP_SEL	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select DDI1 / $\overline{DDI1}$ or DDI2 / $\overline{DDI2}$ as the serial digital input signal, and $\overline{CD1}$ or $\overline{CD2}$ as the carrier detect input signal. When set HIGH, DDI1 / $\overline{DDI1}$ is selected as the serial digital input and $\overline{CD1}$ is selected as the carrier detect input signal. When set LOW, DDI2 / $\overline{DDI2}$ serial digital input and $\overline{CD2}$ carrier detect input signal is selected.
11	NC	–	–	No Connect.
12	20bit/$\overline{10bit}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select the output data bus width in SMPTE or Data-Through modes. This signal is ignored in DVB-ASI mode. When set HIGH, the parallel output will be 20-bit demultiplexed data. When set LOW, the parallel outputs will be 10-bit multiplexed data.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
13	IOPROC_EN/$\overline{DIS}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • EDH CRC Error Correction • ANC Data Checksum Correction • TRS Error Correction • Illegal Code Remapping To enable a subset of these features, keep IOPROC_EN/$\overline{DIS}$ HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accesible via the host interface. When set LOW, the I/O processing features of the device are disabled, regardless of whether the features are enabled in the IOPROC_DISABLE register.
14	$\overline{CD2}$	Non Synchronous	Input	STATUS SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of a serial digital input signal. Normally generated by a Gennum automatic cable equalizer. When LOW, the serial digital input signal received at the DDI2 and $\overline{DDI2}$ pins is considered valid. When HIGH, the associated serial digital input signal is considered to be invalid. In this case, the LOCKED signal is set LOW and all parallel outputs are muted.
15,17	DDI_2, $\overline{DDI\_2}$	Analog	Input	Differential input pair for serial digital input 2.
16	TERM2	Analog	Input	Termination for serial digital input 2. AC couple to PDBUFF_GND.
18	$\overline{SMPTE\_BYPASS}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode. When set LOW, the device will not support the descrambling, decoding or word alignment of received SMPTE data. No I/O processing features will be available.
19	RSET	Analog	Input	Used to set the serial digital loop-through output signal amplitude. Connect to CD_VDD through 281Ω +/- 1% for 800mV$_{p-p}$ single-ended output swing.
20	CD_VDD	–	Power	Power supply connection for the serial digital cable driver. Connect to +1.8V DC analog.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
21	SDO_EN/$\overline{DIS}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the serial digital output loop-through stage. When set LOW, the serial digital output signals SDO and $\overline{SDO}$ are disabled and become high impedance. When set HIGH, the serial digital output signals SDO and $\overline{SDO}$ are enabled.
22	CD_GND	–	Power	Ground connection for the serial digital cable driver. Connect to analog GND.
23, 24	SDO, $\overline{SDO}$	Analog	Output	Serial digital loop-through output signal operating at 270Mb/s. The slew rate of these outputs is automatically controlled to meet SMPTE 259M specifications.
25	$\overline{RESET\_TRST}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG test sequence. Host Mode (JTAG/$\overline{HOST}$ = LOW) When asserted LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance, including the serial digital outputs SDO and $\overline{SDO}$. Must be set HIGH for normal device operation. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH) When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes.
26	JTAG/$\overline{HOST}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{CS}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured for JTAG boundary scan testing. When set LOW, $\overline{CS}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured as GSPI pins for normal host interface operation.
27	$\overline{CS}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip Select / Test Mode Select Host Mode (JTAG/$\overline{HOST}$ = LOW) $\overline{CS}$_TMS operates as the host interface chip select, $\overline{CS}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH) $\overline{CS}$_TMS operates as the JTAG test mode select, TMS, and is active HIGH. NOTE: If the host interface is not being used, tie this pin HIGH.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
28	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SDOUT_TDO operates as the JTAG test data output, TDO.
29	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data In / Test Data Input Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SDIN_TDI operates as the JTAG test data input, TDI. NOTE: If the host interface is not being used, tie this pin HIGH.
30	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Clock / Test Clock. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SCLK_TCK operates as the JTAG test clock, TCK. NOTE: If the host interface is not being used, tie this pin HIGH.
31	$\overline{\text{DATA\_ERROR}}$	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. The $\overline{\text{DATA\_ERROR}}$ signal will be LOW when an error within the received data stream has been detected by the device. This pin is a logical 'OR'ing of all detectable errors listed in the internal ERROR_STATUS register. Once an error is detected, $\overline{\text{DATA\_ERROR}}$ will remain LOW until the start of the next video frame / field, or until the ERROR_STATUS register is read via the host interface. The $\overline{\text{DATA\_ERROR}}$ signal will be HIGH when the received data stream has been detected without error. NOTE: It is possible to program which error conditions are monitored by the device by setting appropriate bits of the ERROR_MASK register HIGH. All error conditions are detected by default.
32	$\overline{\text{FIFO\_LD}}$	Synchronous with PCLK	Output	CONTROL SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used as a control signal for external FIFO(s). Normally HIGH but will go LOW for one PCLK period at SAV.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
33, 68	CORE_GND	–	Power	Ground connection for the digital core logic. Connect to digital GND.
34	F	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the ODD / EVEN field of the video signal. The F signal will be HIGH for the entire period of field 2 as indicated by the F bit in the received TRS signals. The F signal will be LOW for all lines in field 1 and for all lines in progressive scan systems.
35	V	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the portion of the video field / frame that is used for vertical blanking. The V signal will be HIGH for the entire vertical blanking period as indicated by the V bit in the received TRS signals. The V signal will be LOW for all lines outside of the vertical blanking interval.
36	H	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the portion of the video line containing active video data. H signal timing is configurable via the H_CONFIG bit of the IOPROC_DISABLE register accessible via the host interface. Active Line Blanking (H_CONFIG = 0_h) The H signal will be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words, and LOW otherwise. This is the default setting. TRS Based Blanking (H_CONFIG = 1_h) The H signal will be HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise.
37, 64	CORE_VDD	–	Power	Power supply connection for the digital core logic. Connect to +1.8V DC digital.
38, 39, 42–48, 50	DOUT[0:9]	Synchronous with PCLK	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DOUT9 is the MSB and DOUT0 is the LSB.
				20-bit mode 20bit/10bit = HIGH Chroma data output in SMPTE mode SMPTE_BYPASS = HIGH DVB_ASI = LOW Data output in Data-Through mode SMPTE_BYPASS = LOW DVB_ASI = LOW Forced LOW in DVB-ASI mode SMPTE_BYPASS = LOW DVB_ASI = HIGH
				10-bit mode 20bit/10bit = LOW Forced LOW in all modes.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
40, 49, 60	IO_GND	–	Power	Ground connection for digital I/O buffers. Connect to digital GND.
41, 53, 61	IO_VDD	–	Power	Power supply connection for digital I/O buffers. Connect to +3.3V DC digital.
51, 52, 54–59, 62, 63	DOUT[10:19]	Synchronous with PCLK	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DOUT19 is the MSB and DOUT10 is the LSB. 20-bit mode (20bit/10bit = HIGH): Luma data output in SMPTE mode (SMPTE_BYPASS = HIGH, DVB_ASI = LOW); Data output in Data-Through mode (SMPTE_BYPASS = LOW, DVB_ASI = LOW); DVB-ASI data in DVB-ASI mode (SMPTE_BYPASS = LOW, DVB_ASI = HIGH) 10-bit mode (20bit/10bit = LOW): Multiplexed Luma and Chroma data output in SMPTE mode (SMPTE_BYPASS = HIGH, DVB_ASI = LOW); Data input in data through mode (SMPTE_BYPASS = LOW, DVB_ASI = LOW); DVB-ASI data in DVB-ASI mode (SMPTE_BYPASS = LOW, DVB_ASI = HIGH)
65	YANC	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of ancillary data in the video stream. For 20-bit demultiplexed data (20bit/$\overline{10bit}$ = HIGH), the YANC signal will be HIGH when VANC or HANC data is detected in the luma video stream and LOW otherwise. For 10-bit multiplexed data (20bit/$\overline{10bit}$ = LOW), the YANC signal will be HIGH when VANC or HANC data is detected anywhere in the data stream and LOW otherwise.
66	CANC	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of ancillary data in the video stream. For 20-bit demultiplexed data (20bit/$\overline{10bit}$ = HIGH), the CANC signal will be HIGH when VANC or HANC data is detected in the chroma video stream and LOW otherwise. For 10-bit multiplexed data (20bit/$\overline{10bit}$ = LOW), the CANC signal will be HIGH when VANC or HANC data is detected anywhere in the data stream and LOW otherwise.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
67	FW_EN/$\overline{DIS}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the noise immune flywheel of the device. When set HIGH, the internal flywheel is enabled. This flywheel is used in the extraction and generation of TRS timing signals, in automatic video standards detection, and in manual switch line lock handling. When set LOW, the internal flywheel is disabled and TRS correction and insertion is unavailable.
69	PCLK	–	Output	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS/LVTTL compatible. 20-bit mode PCLK = 13.5MHz 10-bit mode PCLK = 27MHz
70	$\overline{RC\_BYP}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set HIGH, the serial digital output will be a reclocked version of the input signal regardless of whether the device is in SMPTE, DVB-ASI or Data-Through mode. When set LOW, the serial digital output will be a buffered version of the input signal in all modes.
71	NC	–	–	No connect.
72	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. The LOCKED signal will be HIGH whenever the device has correctly received and locked to SMPTE compliant data in SMPTE mode or DVB-ASI compliant data in DVB-ASI mode. It will be LOW otherwise.
73, 74	VCO, $\overline{VCO}$	Analog	Input	Differential inputs for the external VCO reference signal. For single ended devices such as the GO1555/GO1525*, $\overline{VCO}$ should be AC coupled to VCO_GND. *For new designs use GO1555
75	VCO_GND	–	Output Power	Ground reference for the external voltage controlled oscillator. Connect to pins 2, 4, 6, and 8 of the GO1555/GO1525*. This pin is an output. Should be isolated from all other grounds. *For new designs use GO1555

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
76	VCO_VCC	–	Output Power	Power supply for the external voltage controlled oscillator. Connect to pin 5 of the GO1555/GO1525*. This pin is an output. Should be isolated from all other power supplies. *For new designs use GO1555
77	LF	Analog	Output	Control voltage to external voltage controlled oscillator. Nominally +1.25V DC.
78	CP_CAP	Analog	Input	PLL lock time constant capacitor connection. Normally connected to VCO_GND through 2.2nF.
79	LB_CONT	Analog	Input	Control voltage to set the loop bandwidth of the integrated reclocker. Normally connected to VCO_GND through 40kΩ.
80	CP_GND	–	Power	Ground connection for the charge pump. Connect to analog GND.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +4.6V
Input Voltage Range (any input)	-2.0V to + 5.25V
Ambient Operating Temperature	-20°C ≤ T_A ≤ 85°C
Storage Temperature	-40°C ≤ T_{STG} ≤ 125°C
Lead Temperature (soldering, 10 sec)	230°C
ESD Protection On All Pins	1kV

NOTES:

1. See reflow solder profiles (Section 2.4 on page 18)
2. MIL STD 883 ESD protection applied to all pins on the device.

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
System								
Operation Temperature Range	T_A	–	0	–	70	°C	–	1
Digital Core Supply Voltage	CORE_VDD	–	1.65	1.8	1.95	V	1	1
Digital I/O Supply Voltage	IO_VDD	–	3.0	3.3	3.6	V	1	1
Charge Pump Supply Voltage	CP_VDD	–	3.0	3.3	3.6	V	1	1
Phase Detector Supply Voltage	PD_VDD	–	1.65	1.8	1.95	V	1	1
Input Buffer Supply Voltage	BUFF_VDD	–	1.65	1.8	1.95	V	1	1
Cable Driver Supply Voltage	CD_VDD	–	1.71	1.8	1.89	V	1	1
External VCO Supply Voltage Output	VCO_VCC	–	2.25	2.50	2.75	V	1	–
+1.8V Supply Current	I_{1V8}	–	–	–	245	mA	1	4
+3.3V Supply Current	I_{3V3}	–	–	–	55	mA	1	–
Total Device Power	P_D	–	–	–	625	mW	5	4

Table 2-1: DC Electrical Characteristics (Continued)

T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
Digital I/O								
Input Logic LOW	V_{IL}	–	–	–	0.8	V	1	–
Input Logic HIGH	V_{IH}	–	2.1	–	–	V	1	–
Output Logic LOW	V_{OL}	8mA	–	0.2	0.4	V	1	–
Output Logic HIGH	V_{OH}	8mA	IO_VDD - 0.4	–	–	V	1	–
Input								
Input Bias Voltage	V_B	–	–	1.45	–	V	6	2
RSET Voltage	V_{RSET}	RSET=281Ω	0.54	0.6	0.66	V	1	3
Output								
Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET=281Ω	0.8	1.0	1.2	V	1	–

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. All DC and AC electrical parameters within specification.
2. Input common mode is set by internal biasing resistors.
3. Set by the value of the RSET resistor.
4. Loop-through enabled.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
System								
Serial Digital Input Jitter Tolerance	IJT	Nominal loop bandwidth	0.6	–	–	UI	1	1
Slave Mode Asynchronous Lock Time		No data to SD	–	–	197	us	6,7	2
		No data to DVB-ASI	–	–	68	us	6,7	2
Device Latency		SMPTE and Data-Through modes	–	21	–	PCLK	6	–
		DVB-ASI mode	–	11	–	PCLK	6	–
Reset Pulse Width	t_{reset}	–	1	–	–	ms	7	6
Serial Digital Differential Input								
Serial Input Data Rate	DR_{DDI}	–	–	270	–	Mb/s	1	–
Serial Digital Input Signal Swing	ΔV_{DDI}	Differential with internal 100Ω input termination	200	600	1000	mV_{p-p}	1	–
Serial Digital Output								
Serial Output Data Rate	DR_{SDO}	–	–	270	–	Mb/s	1	–
Serial Output Swing	ΔV_{SDO}	RSET = 281Ω Load = 75Ω	–	800	–	mVp-p	1	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	ORL compensation using recommended circuit	400	550	1500	ps	1	–
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	ORL compensation using recommended circuit	400	550	1500	ps	1	–
Serial Output Intrinsic Jitter	t_{IJ}	Pseudorandom and pathological	–	270	350	ps	1	3
Serial Output Duty Cycle Distortion	DCD_{SDO}	–	–	20	–	ps	6,7	4
Parallel Output								
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	27.0	MHz	1	
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	50	60	%	1	
Output Data Hold Time	t_{OH}	–	19.5	–	–	ns	1	5
Output Data Delay Time	t_{OD}	–	–	–	22.8	ns	1	5
Output Data Rise/Fall Time	tr/tf	–	–	–	1.5	ns	6,7	5

Table 2-2: AC Electrical Characteristics (Continued)

T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
GSPI								
GSPI Input Clock Frequency	f_{SCLK}	–	–	–	6.6	MHz	1	–
GSPI Input Clock Duty Cycle	DC_{SCLK}	–	40	50	60	%	6,7	–
GSPI Input Data Setup Time		–	0	–	–	ns	6,7	–
GSPI Input Data Hold Time		–	1.43	–	–	ns	6,7	–
GSPI Output Data Hold Time		–	2.10	–	–	ns	6,7	–
GSPI Output Data Delay Time		–	–	–	7.27	ns	6,7	–

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. 6MHz sine wave modulation.
2. SD = 525i
3. Serial Digital Output Reclocked ($\overline{RC\_BYP}$ = HIGH).
4. Serial Duty Cycle Distortion is defined here to be the difference between the width of a ‘1’ bit, and the width of a ‘0’ bit.
5. With 15pF load.
6. See Section 3.15 on page 55, Figure 3-15.

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. The recommended standard eutectic reflow profile is shown in Figure 2-1. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-2.

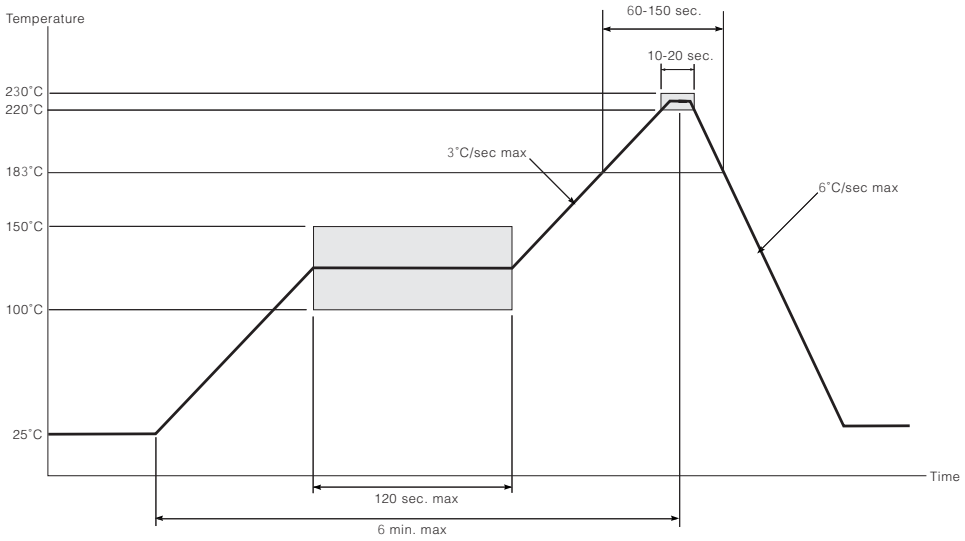


Figure 2-1: Standard Eutectic Solder Reflow Profile

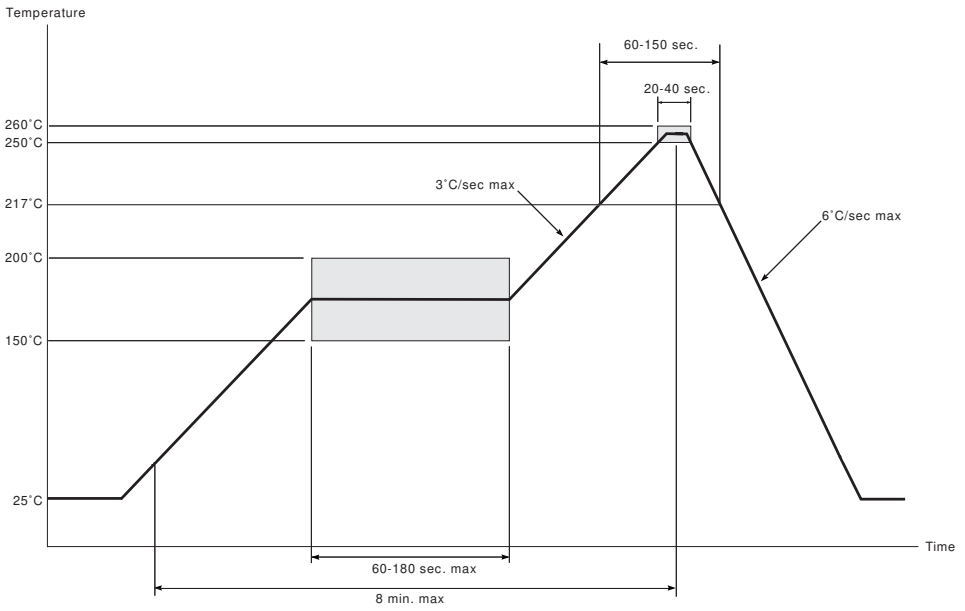


Figure 2-2: Maximum Pb-free Solder Reflow Profile (Pb-free package)

2.5 Input/Output Circuits

All resistors in ohms, all capacitors in farads, unless otherwise shown.

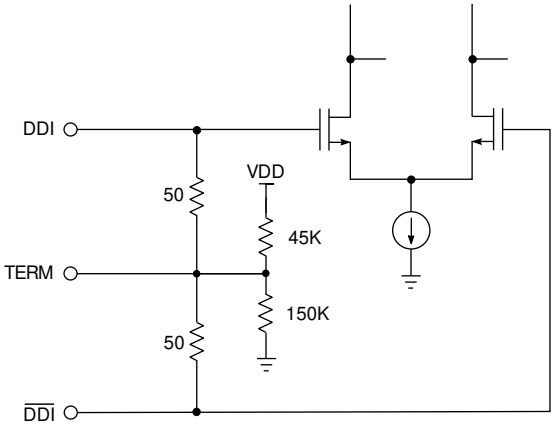


Figure 2-3: Serial Digital Input

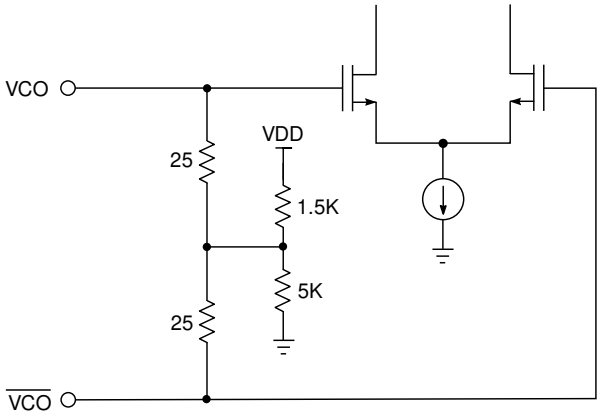


Figure 2-4: VCO Input

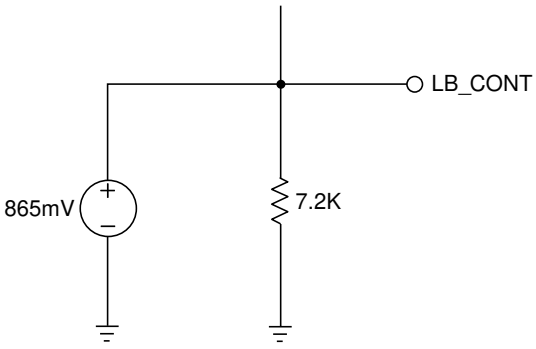


Figure 2-5: PLL Loop Bandwidth Control

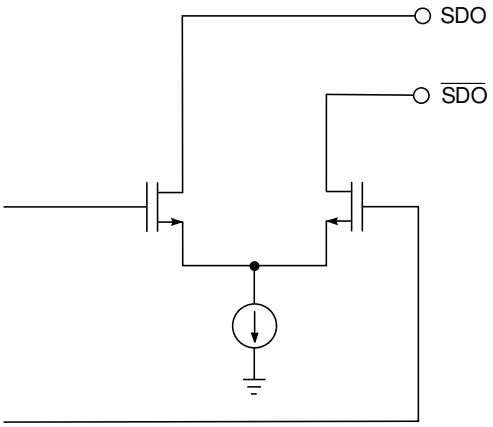


Figure 2-6: Serial Digital Output

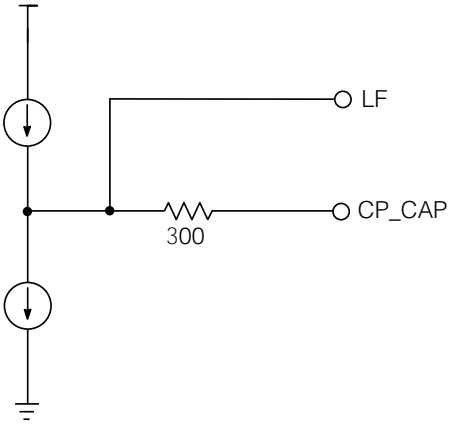


Figure 2-7: VCO Control Output & PLL Lock Time Capacitor

2.6 Host Interface Map

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROR_MASK	1Ah	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ ERR_MASK	FF_CRC_ ERR_MASK	AP_CRC_ ERR_MASK	LOCK_ ERR_MASK	Not Used	CS_ERR_ MASK	Not Used	Not Used	Not Used	SAV_ERR_ MASK	EAV_ERR_ MASK
FF_LINE_END_F1	19h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1	18h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0	17h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0	16h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1	15h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1	14h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0	13h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0	12h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE4	11h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3	10h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2	0Fh	Not Used	Not Used	Not Used	Not Used	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1	0Eh	Not Used	Not Used	Not Used	Not Used	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B	0Dh	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A	0Ch	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Bh																
	0Ah																
ANC_TYPE5	09h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE4	08h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE3	07h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE2	06h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE1	05h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_STANDARD	04h	Not Used	VDS-b4	VDS-b3	VDS-b2	VDS-b1	VDS-b0	INT_PROG	STD_ LOCK	Not Used	Not Used	Not Used	Not Used	DF-b3	DF-b2	DF-b1	DF-b0
EDH_FLAG	03h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	02h																
ERROR_STATUS	01h	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR	Not Used	CS_ERR	Not Used	Not Used	Not Used	SAV_ERR	EAV_ERR
IOPROC_DISABLE	00h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	H_CONFIG	Not Used	Not Used	ILLEGAL_ REMAP	EDH_CRC_ INS	ANC_CSUM_ INS	Not Used	Not Used	TRS_INS

2.6.1 Host Interface Map (R/W registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROR_MASK	1Ah						VD_STD_ ERR_MASK	FF_CRC_ ERR_MASK	AP_CRC_ ERR_MASK	LOCK_ ERR_MASK	Not Used	CS_ERR_ MASK	Not Used	Not Used	Not Used	SAV_ERR_ MASK	EAV_ERR_ MASK
FF_LINE_END_F1	19h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1	18h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0	17h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0	16h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1	15h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1	14h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0	13h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0	12h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	11h																
	10h																
	0Fh																
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
ANC_TYPE5	09h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE4	08h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE3	07h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE2	06h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE1	05h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	04h																
	03h																
	02h																
	01h																
IOPROC_DISABLE	00h								H_CONFIG			ILLEGAL_ REMAP	EDH_CRC_ INS	ANC_CSUM_ INS			TRS_INS

2.6.2 Host Interface Map (Read only registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1Ah																
	19h																
	18h																
	17h																
	16h																
	15h																
	14h																
	13h																
	12h																
RASTER_STRUCTURE4	11h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3	10h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2	0Fh					b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1	0Eh					b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B	0Dh	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A	0Ch	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Bh																
	0Ah																
	09h																
	08h																
	07h																
	06h																
	05h																
VIDEO_STANDARD	04h		VDS-b4	VDS-b3	VDS-b2	VDS-b1	VDS-b0	INT_PROG	STD_LOCK					DF-b3	DF-b2	DF-b1	DF-b0
EDH_FLAG	03h		ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	02h																
ERROR_STATUS	01h						VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR		CS_ERR				SAV_ERR	EAV_ERR
	00h																

3. Detailed Description

3.1 Functional Overview

The GS9060 is a dual-standard reclocking deserializer with an integrated serial digital loop-through output. When used in conjunction with any Gennum cable equalizer and the external GO1555/GO1525* Voltage Controlled Oscillator, a receive solution at 270Mb/s is realized.

The application layer must set external device pins for the correct reception of either SMPTE or DVB-ASI data. The GS9060 also supports the reclocking and deserializing of data not conforming to SMPTE or DVB-ASI streams.

The provided serial loop-through outputs may be selected as either buffered or reclocked versions of the input signal and feature a high impedance mode, output mute on loss of signal and adjustable signal swing.

In the digital signal processing core, several data processing functions are implemented including error detection and correction and automatic video standards detection. These features are all enabled by default, but may be individually disabled via internal registers accessible through the GSPI host interface.

Finally, the GS9060 contains a JTAG interface for boundary scan test implementations.

*For new designs use GO1555

3.2 Serial Digital Input

The GS9060 contains two current mode differential serial digital input buffers, allowing the device to be connected to two SMPTE 259M-C compliant input signals.

Both input buffers have internal 50Ω termination resistors which are connected to ground via the TERM1 and TERM2 pins. The input common mode level is set by internal biasing resistors such that the serial digital input signals must be AC coupled into the device. Gennum recommends using a capacitor value of 4.7uF to accommodate pathological signals.

The input buffers use a separate power supply of +1.8V DC supplied via the BUFF_VDD and PDBUFF_GND pins.

3.2.1 Input Signal Selection

A 2x1 input multiplexer is provided to allow the application layer to select between the two serial digital input streams using a single external pin. When IP_SEL is set HIGH, serial digital input 1 (DDI1 / $\overline{\text{DDI1}}$) is selected as the input to the GS9060's reclocker stage. When IP_SEL is set LOW, serial digital input 2 (DDI2 / $\overline{\text{DDI2}}$) is selected.

3.2.2 Carrier Detect Input

For each of the differential inputs, an associated carrier detect input signal is included, ($\overline{CD1}$ and $\overline{CD2}$). These signals are generated by Gennum's family of automatic cable equalizers.

When LOW, $\overline{CDx}$ indicates that a valid serial digital data stream is being delivered to the GS9060 by the equalizer. When HIGH, the serial digital input to the device should be considered invalid. If no equalizer precedes the device, the application layer should set $\overline{CD1}$ and $\overline{CD2}$ accordingly.

NOTE: If the GS9064 Automatic Cable Equalizer is used, the MUTE/$\overline{CD}$ output signal from that device must be translated to TTL levels before passing to the GS9060 $\overline{CDx}$ inputs. See Section 4.1 on page 56 for a recommended transistor network that will set the correct voltage levels.

A 2x1 input multiplexer is also provided for these signals. The internal carrier_detect signal is determined by the setting of the IP_SEL pin and is used by the lock detect block of the GS9060 to determine the lock status of the device, Section 3.6 on page 28.

3.2.3 Single Input Configuration

If the application requires a single differential input, the second set of inputs may be left unconnected. Tie the associated carrier detect pin HIGH, and leave the termination pin unconnected.

3.3 Serial Digital Reclocker

The output of the 2x1 serial digital input multiplexer passes to the GS9060's internal reclocker stage. The function of this block is to lock to the input data stream, extract a clean clock, and retime the serial digital data to remove high frequency jitter.

The reclocker was designed with a 'hexabang' phase and frequency detector. That is, the PFD used can identify six 'degrees' of phase / frequency misalignment between the input data stream and the clock signal provided by the VCO, and correspondingly signal the charge pump to produce six different control voltages. This results in fast and accurate locking of the PLL to the data stream.

If lock is achieved, the reclocker provides an internal pll_lock signal to the lock detect block of the device.