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Features

- SMPTE 259M and SMPTE 344M compliant
- Dual coaxial cable driving outputs with selectable slew rate
- 50Ω differential PECL input
- Pb-free and RoHS compliant
- Seamless interface to other HD-LINX® II family products
- Single 3.3V power supply operation
- Operating temperature range: 0°C to 70°C

Applications

- SMPTE 259M and SMPTE 344M Coaxial Cable Serial Digital Interfaces.

Description

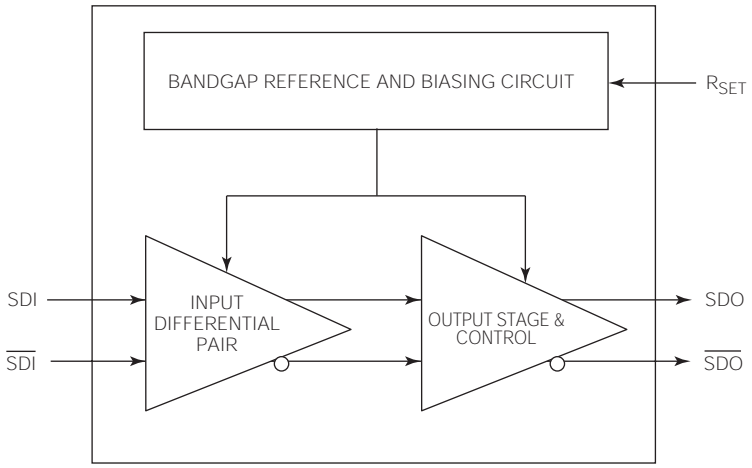
The GS9078A is a second generation high-speed BiCMOS integrated circuit designed to drive one or two 75Ω co-axial cables.

The GS9078A may drive data rates up to 540Mb/s and provides two selectable slew rates in order to achieve compliance to SMPTE 259M and SMPTE 344M.

The GS9078A accepts a LVPECL level differential input that may be AC coupled. External biasing resistors at the inputs are not required.

Power consumption is typically 168mW using a 3.3V power supply. The GS9078A is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



Functional Block Diagram

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1. Pin Out

1.1 Pin Assignment

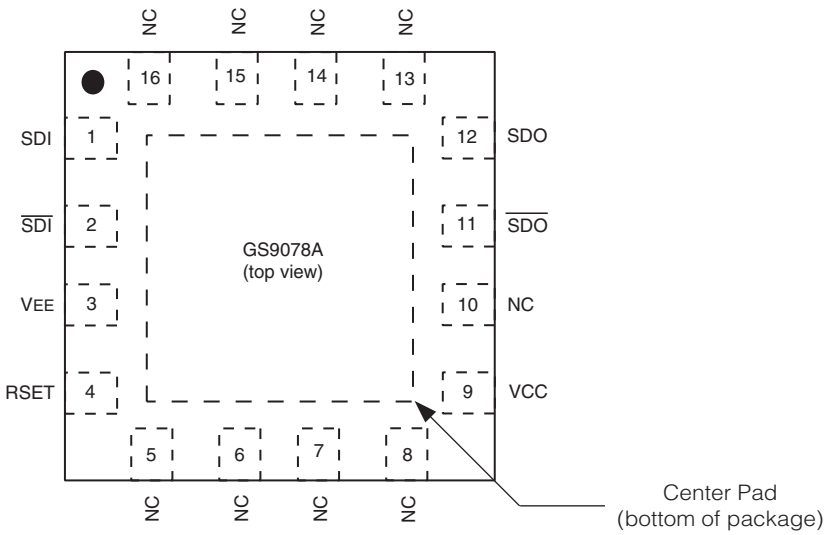


Figure 1-1: 16-Pin QFN

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1,2	SDI, $\overline{SDI}$	Analog	Input	Serial digital differential input.
3	V_{EE}	–	Power	Most negative power supply connection. Connect to GND.
4	R_{SET}	Analog	Input	External output amplitude control resistor.
5,6,7,8,10, 13,14,15,16	NC	–	–	No Connect. Not bonded internally.
9	V_{CC}	–	Power	Most positive power supply connection. Connect to +3.3V.
11,12	$\overline{SDO}$, SDO	Analog	Output	Serial digital differential output.
–	Center Pad	–	Power	Connect to most negative power supply plane following the recommendations in Recommended PCB Footprint on page 13.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6 V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Reflow Temperature	260°C

2.2 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-1.The recommended standard Pb reflow profile is shown in Figure 2-2.

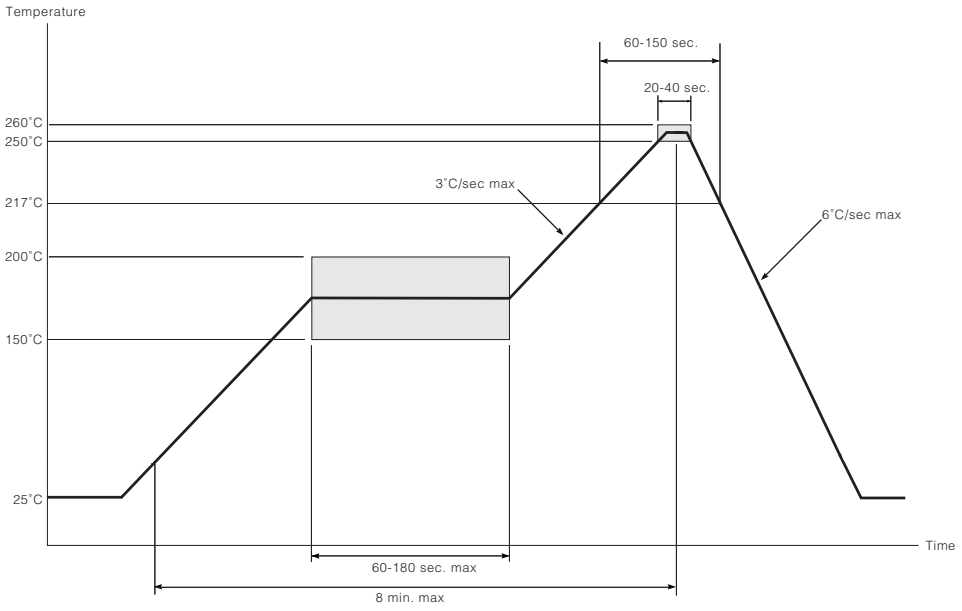


Figure 2-1: Maximum Pb-free Solder Reflow Profile (Preferred)

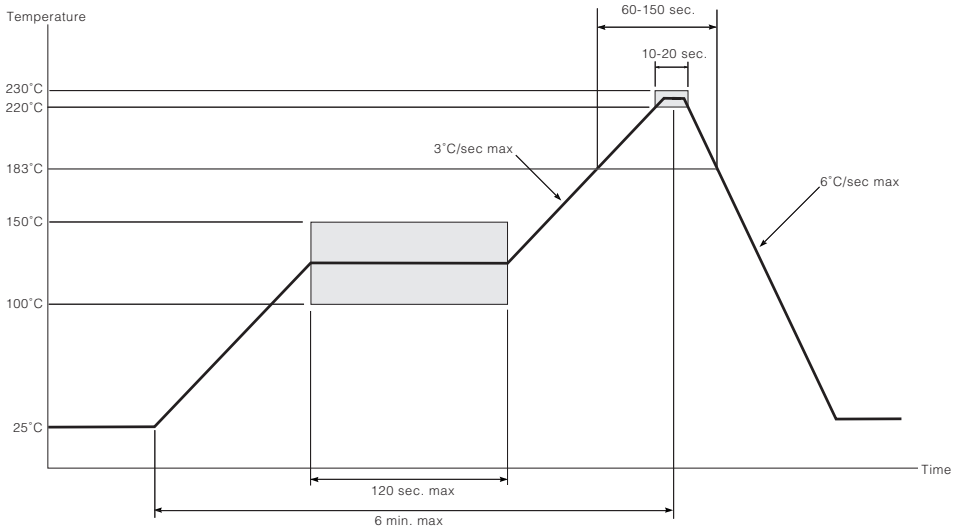


Figure 2-2: Standard Pb Reflow Profile (Pb-free package)

2.3 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Power Consumption	P_D	T_A = 25°C	–	168	–	mW
Supply Current	I_s	T_A = 25°C	–	51	64	mA
Output Voltage	V_{CMOUT}	Common mode	–	V_{CC} - V_{OUT}	–	V
Input Voltage	V_{CMIN}	Common mode	1.6 + $\Delta V_{SDI}/2$	–	V_{CC} - $\Delta V_{SDI}/2$	V

2.4 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	–	–	540	Mb/s	1
Additive jitter	–	–	–	20	–	ps_{p-p}	–
Rise/Fall time	t_r, t_f	–	400	–	800	ps	2
Mismatch in rise/fall time	$\triangle t_r$, $\triangle t_f$	–	–	–	30	ps	–
Duty cycle distortion	–	–	–	–	100	ps	–
Overshoot	–	–	–	–	8	%	–
Output Return Loss	ORL	–	15	–	–	dB	–
Output Voltage Swing	V_{OUT}	Single Ended into 75Ω external load R_{SET} = 750Ω	750	800	850	mV_{p-p}	–
Input Voltage Swing	$\triangle V_{SDI}$	Differential	300	–	2200	mV_{p-p}	–

NOTES:

1. The input coupling capacitor must be set accordingly for lower data rates.
2. Rise/Fall time measured between 20% and 80%.

3. Input / Output Circuits

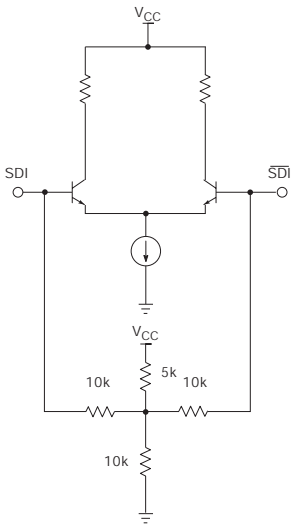


Figure 3-1: Differential Input Stage (SDI/$\overline{\text{SDI}}$)

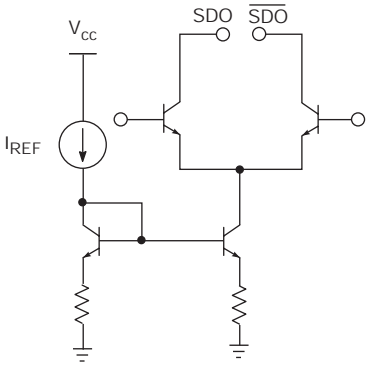


Figure 3-2: Differential Output Stage (SDO/$\overline{\text{SDO}}$)

4. Detailed Description

4.1 Input Interfacing

SDI/$\overline{\text{SDI}}$ are high impedance differential inputs. The equivalent input circuit is shown in Figure 3-1.

Several conditions must be observed when interfacing to these inputs:

- The differential input signal amplitude must be between 300 and 2000mVpp.
- The common mode voltage range must be as specified in the DC Electrical Characteristics on page 5.
- For input trace lengths longer than approximately 1cm, the inputs should be terminated as shown in the Typical Application Circuit.

The GS9078A inputs are self-biased, allowing for simple AC coupling to the device. For serial digital video, a minimum capacitor value of 4.7µF should be used to allow coupling of pathological test signals. A tantalum capacitor is recommended.

4.2 Output Interfacing

The GS9078A outputs are current mode, and will drive 800mV into a 75Ω load. These outputs are protected from accidental static damage with internal static protection diodes.

The SMPTE 344M and SMPTE 259M standards require that the output of a cable driver have a source impedance of 75Ω and a return loss of at least 15dB between 5MHz and 540MHz.

In order for an SDI output circuit using the GS9078A to meet this specification, the output application circuit shown in Typical Application Circuit on page 11 is recommended.

The value of L_{COMP} will vary depending on the PCB layout, with a typical value of 5.6nH. A 4.7µF capacitor is used for AC coupling the output of the device. This value is chosen to ensure that pathological signals can be coupled without a significant DC component occurring. Please see Application Information on page 11 for more details.

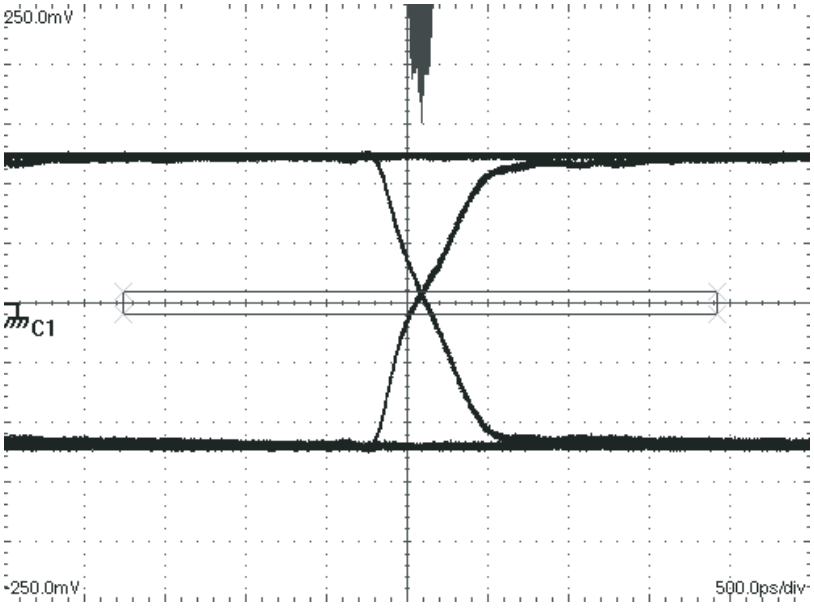


Figure 4-1: Output signal for 270Mb/s input

The output protection diodes act as a varactor (voltage controlled capacitor) as shown in Figure 4-2. Therefore, when measuring return loss at the GS9078A output, it is necessary to take the measurement for both a logic high and a logic low output condition.

Consequently, the output capacitance of the device is dependent on the logic state of the output.

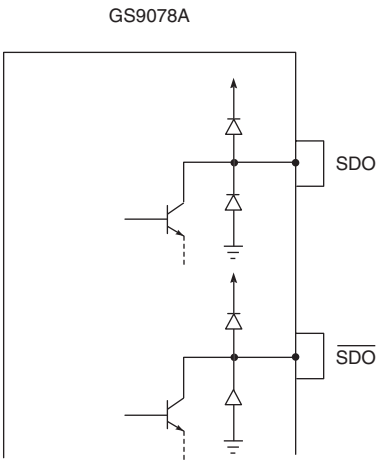


Figure 4-2: Static Protection Diodes

4.3 Output Return Loss Measurement

To perform a practical return loss measurement, it is necessary to force the GS9078A output to a DC high or low condition. The actual measured return loss will be based on the outputs being static at V_{CC} or V_{CC}-1.6V. Under normal operating conditions the outputs of the device swing between V_{CC}-0.4V and V_{CC}-1.2V, so the measured value of return loss will not represent the actual operating return loss.

A simple method of calculating the values of actual operating return loss is to interpolate the two return loss measurements. In this way, the values of return loss are estimated at V_{CC}-0.4V and V_{CC}-1.2V based on the measurements at V_{CC} and V_{CC}-1.6V.

The two values of return loss (high and low) will typically differ by several decibels. If the measured return loss is R_H for logic high and R_L for logic low, then the two values can be interpolated as follows:

$$R_{IH} = R_H - (R_H - R_L)/4 \text{ and}$$

$$R_{IL} = R_L + (R_H - R_L)/4$$

where R_{IH} is the interpolated logic high value and R_{IL} is the interpolated logic low value.

For example, if R_H = -18dB and R_L = -14dB, then the interpolated values are R_{IH} = -17dB and R_{IL} = -15dB.

4.4 Output Amplitude (RSET)

The output amplitude of the GS9078A is set to 800mV_{p-p} with a tolerance of ±7% using an RSET resistor of 750Ω. A ±1% SMT resistor should be used.

The R_{SET} resistor is part of the high speed output circuit of the GS9078A. The resistor should be placed as close as possible to the R_{SET} pin. In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the R_{SET} resistor and the R_{SET} pin.

NOTE: Only an R_{SET} value of 750Ω ±1% should be used. Using other values for R_{SET} is not recommended.

5. Application Information

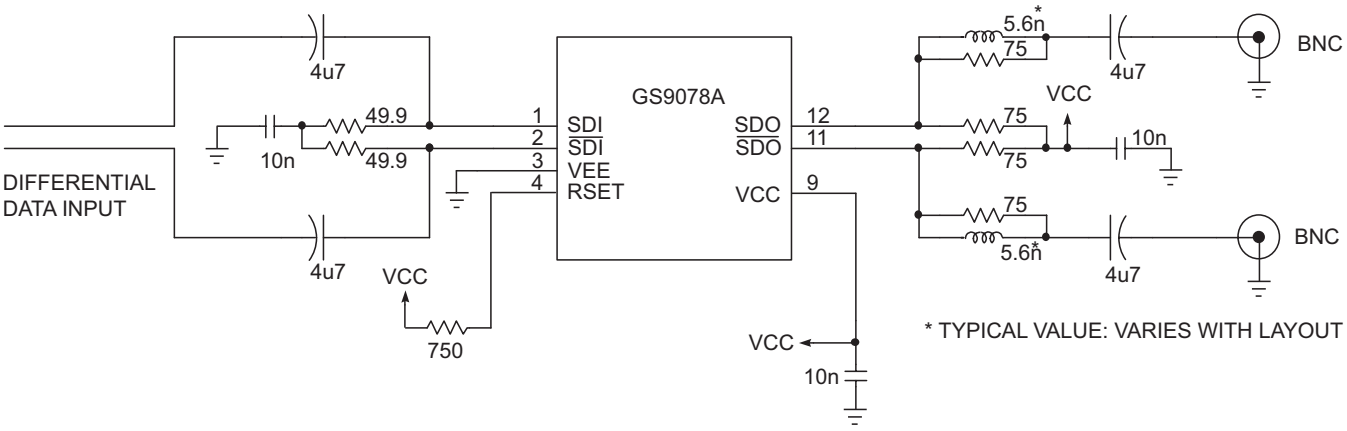
5.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for SDTV.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB trace width for SD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance.
- The PCB groundplane is removed under the GS9078A output components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS9078A R_{SET} pin and resistor to minimize parasitic capacitance.
- Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high speed traces which are curved to minimize impedance variations due to change of PCB trace width.

5.2 Typical Application Circuit

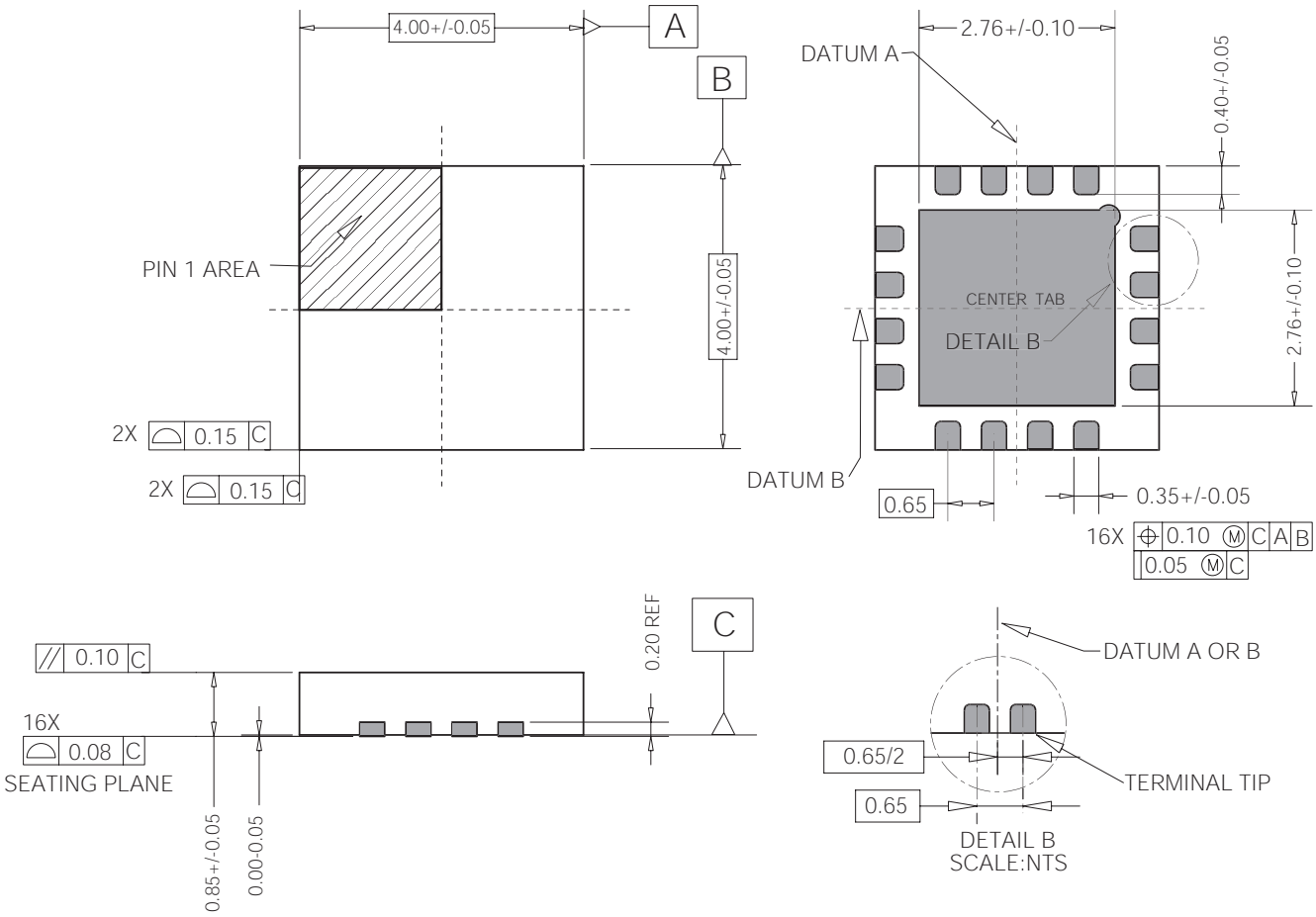


NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

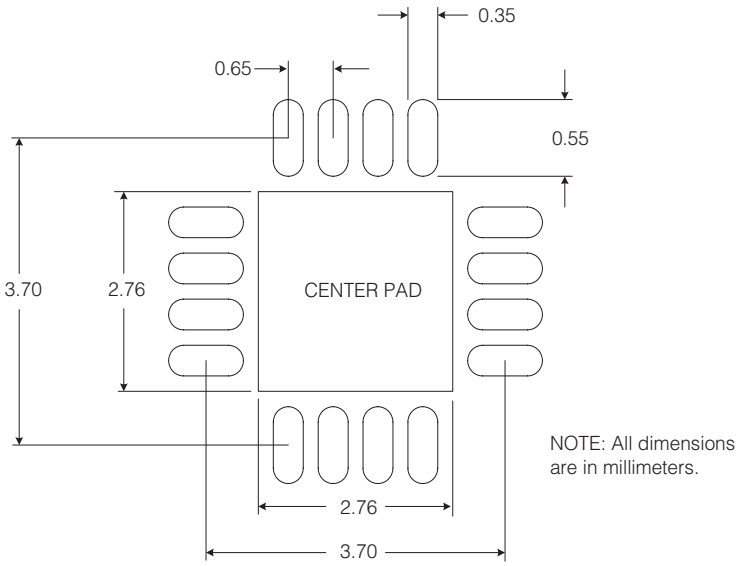
Figure 5-1: Typical Application Circuit

6. Package & Ordering Information

6.1 Package Dimensions



6.2 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane (VEE) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi	11.0°C/W
Pb-free and RoHS compliant	Yes

6.4 Ordering Information

	Part Number	Package	Temperature Range
GS9078A	GS9078ACNE3	16-pin QFN	0°C to 70°C

7. Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
A	135926	–	February 2005	New document.
0	136048	–	February 2005	Converting to Preliminary Data Sheet. Added PCB Layout section. Updated Typical Application Circuit.
1	136655	–	June 2005	Converted to Data Sheet. Changed title of Figure 2-2 to clarify that this is the Pb reflow profile. Updated Additive Jitter number in AC Electrical Characteristics table to be typically 20ps$_{p-p}$. Updated dimensions of the center pad of the PCB footprint in Section 6.2 to match the dimensions of the center pad of the device. Corrected part number in ordering information. Rephrased the RoHS Compliant statement.
2	137887	–	September 2005	Corrected process to BiCMOS.
3	139115	38124	January 2006	Corrected Input Differential Swing to 2200mV.
4	139636	38695	March 2006	Corrected pad standoff height and tolerances for pad width & package dimension. Corrected pad shape.

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