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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





## GS9090A GenLINX® III 270Mb/s Deserializer

### Key Features

- SMPTE 259M-C compatible descrambling and NRZI to NRZ decoding (with bypass)
- DVB-ASI 8b/10b decoding
- Integrated line-based FIFO for data alignment/delay, clock phase interchange, DVB-ASI data packet extraction and clock rate interchange, and ancillary data packet extraction
- Integrated VCO and reclocker
- Single serial digital input buffer with wide input sensitivity and common mode point
- User selectable additional processing features including:
  - ◆ TRS, ANC data checksum, and EDH CRC error detection and correction
  - ◆ programmable ANC data detection
  - ◆ illegal code remapping
- Internal flywheel for noise immune H, V, F extraction
- Automatic standards detection and indication
- Enhanced Gennum Serial Peripheral Interface (GSPI)
- JTAG test interface
- Polarity insensitive for DVB-ASI and SMPTE signals
- +1.8V core power supply with optional +1.8V or +3.3V I/O power supply
- Small footprint (8mm x 8mm)
- Low power operation (typically 145mW)
- Pb-free and RoHS compliant

### Applications

- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

### Description

The GS9090A is a 270Mb/s reclocking deserializer with an internal FIFO. When used in conjunction with one of Gennum's SDI Cable Equalizers, a receive solution for SD-SDI and DVB-ASI applications can be realized.

In addition to reclocking and deserializing the input data stream, the GS9090A performs NRZI-to-NRZ decoding, descrambling as per SMPTE 259M-C, and word alignment when operating in SMPTE mode. When operating in DVB-ASI mode, the device will word align the data to K28.5 sync characters and 8b/10b decode the received stream.

The integrated reclocker features a very wide Input Jitter Tolerance, and is fully compatible with both SMPTE and DVB-ASI input streams.

The GS9090A includes a range of data processing functions such as error detection and correction, automatic standards detection, and EDH support. The device can also detect and extract SMPTE 352M payload identifier packets and independently identify the received video standard. This information is read from internal registers via the host interface port.

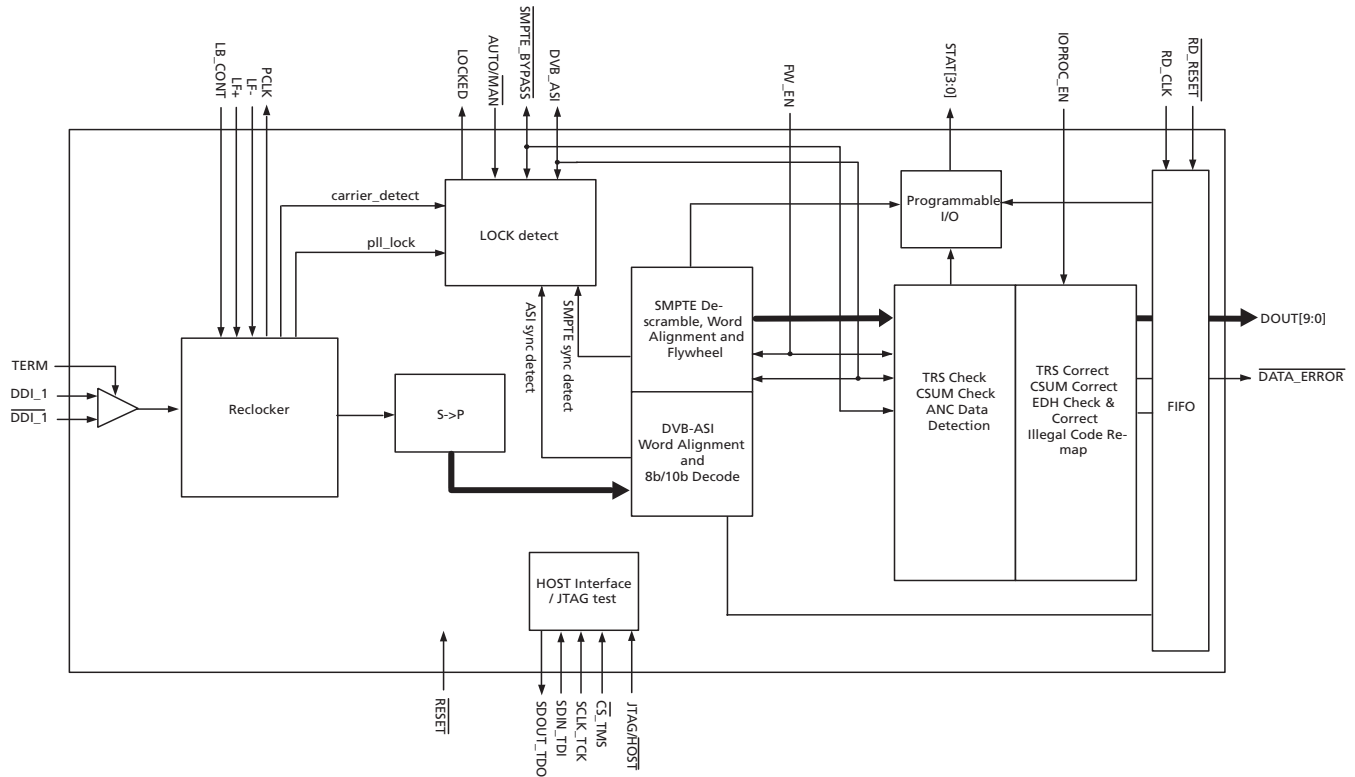
TRS errors, EDH CRC errors, and ancillary data checksum errors can all be detected and corrected. A single `DATA_ERROR` pin is provided which is an inverted logical 'OR'ing of all detectable errors. Individual error status is stored in internal 'ERROR\_STATUS' registers.

The GS9090A also incorporates a video line-based FIFO. This FIFO may be used in four user-selectable modes to carry out tasks such as data alignment / delay, clock phase interchange, MPEG packet extraction and clock rate interchange, and ancillary data packet extraction.

Parallel data outputs are provided in 10-bit multiplexed format, with the associated parallel clock output signal operating at 27MHz.

The GS9090A is Pb-free, and the encapsulation compound does not contain halogenated flame retardant (RoHS compliant).

# GS9090A Functional Block Diagram



## Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
7	154185	-	May 2010	Converted document back to Data Sheet.
6	152802	-	October 2009	Changed 6.1 Package Dimensions.
5	152067	-	June 2009	Removed 'Proprietary and Confidential' footer.
4	150197	50711	July 2008	DVB_ASI operation specification change in Auto mode.
3	143053	42121	November 2006	Updated Figure 6-2 Pb-free solder reflow profile to 260°C.
2	141671	40050	August 2006	Removed 'Proprietary and Confidential' footer. Added note on DVB-ASI functionality up to 35Mb/s in Section 3.7.
1	139624	39274	April 2006	Corrected termination dimensional tolerance on packaging diagram.
0	138238	-	February 2006	New Document.



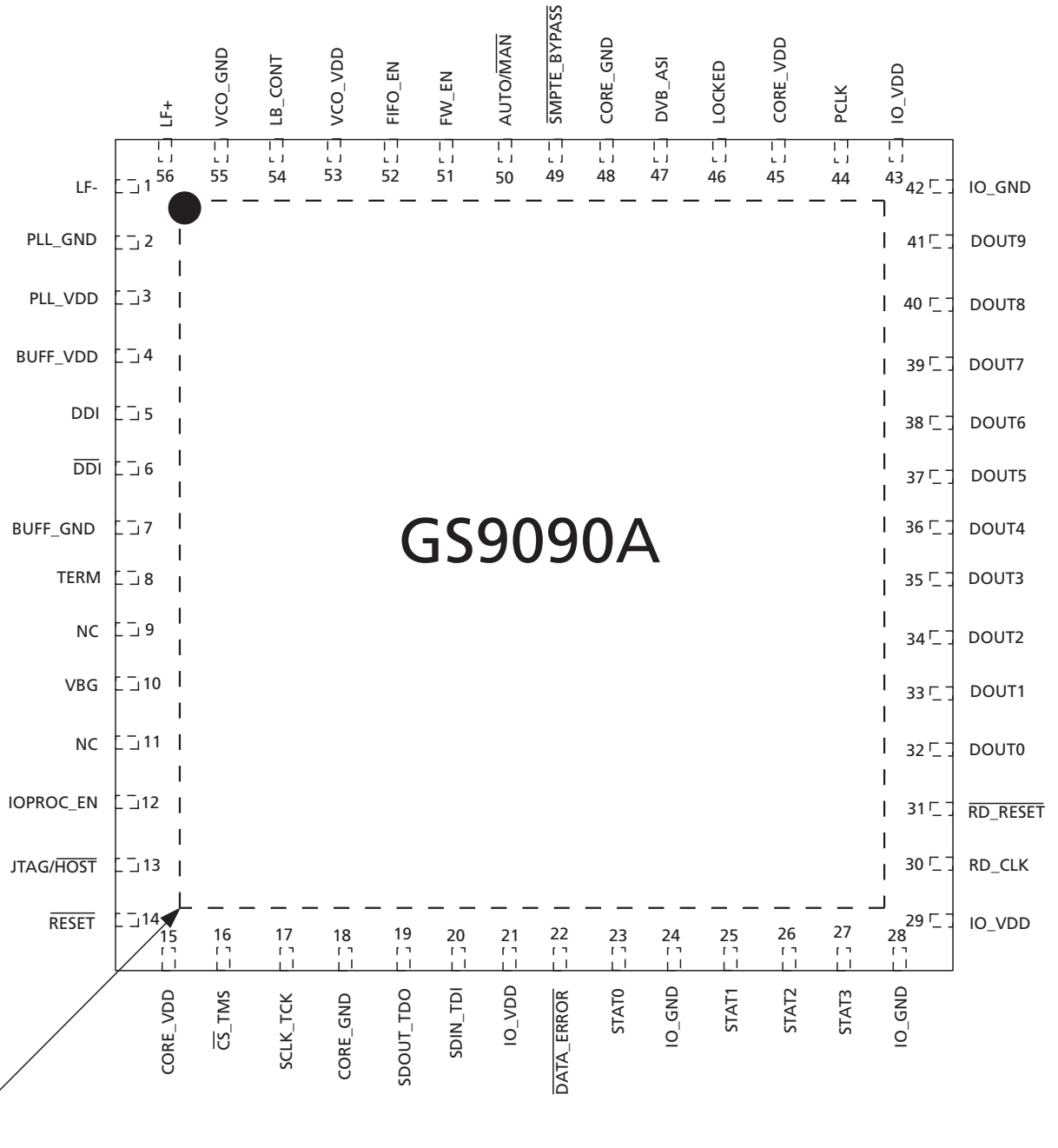
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# 1. Pin Out

## 1.1 Pin Assignment



Center Pad  
(bottom of package)

Figure 1-1: Pin Assignment

## 1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	LF-	Analog	Input	Loop filter component connection. Connect to pin 56 (LF+) as shown in <a href="#">Typical Application Circuit (Part B) on page 68</a> .
2	PLL_GND	Analog	Input Power	Ground connection for phase-locked loop. Connect to GND.
3	PLL_VDD	Analog	Input Power	Power supply connection for phase-locked loop. Connect to +1.8V DC.
4	BUFF_VDD	Analog	Input Power	Power supply connection for digital input buffers. When DDI/ $\overline{\text{DDI}}$ are AC coupled, this pin should be left unconnected. When DDI/ $\overline{\text{DDI}}$ are DC coupled, this pin should be connected to +3.3V as shown in <a href="#">Typical Application Circuit (Part B) on page 68</a> . See <a href="#">Serial Digital Input on page 22</a> for more details.
5, 6	DDI, $\overline{\text{DDI}}$	Analog	Input	Serial digital differential input pair.
7	BUFF_GND	Analog	Input Power	Ground connection for serial digital input buffer. Connect to GND.
8	TERM	Analog	Input	Termination for serial digital input. AC couple to BUFF_GND
9, 11	NC	–	–	No connect.
10	VBG	Analog	Input	Bandgap filter capacitor. Connect to GND as shown in <a href="#">Typical Application Circuit (Part B) on page 68</a> .
12	IOPROC_EN	Non Synchronous	Input	<p>CONTROL SIGNAL INPUT Signal Levels are LVCMOS / LVTTTL compatible. Used to enable or disable the I/O processing features. When set HIGH, the following I/O processing features of the device are enabled:</p> <ul style="list-style-type: none"> <li>• Illegal Code Remapping</li> <li>• EDH CRC Error Correction</li> <li>• Ancillary Data Checksum Error Correction</li> <li>• TRS Error Correction</li> <li>• EDH Flag Detection</li> </ul> <p>To enable a subset of these features, keep the IOPROC_EN pin HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When set LOW, the device will enter low-latency mode. NOTE: When the internal FIFO is configured for Video mode or Ancillary Data Extraction mode, the IOPROC_EN pin must be set HIGH (see <a href="#">Internal FIFO Operation on page 47</a>).</p>

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Timing	Type	Description
13	JTAG/ $\overline{\text{HOST}}$	Non Synchronous	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Used to select JTAG Test Mode or Host Interface Mode.</p> <p>When set HIGH, <math>\overline{\text{CS\_TMS}}</math>, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured for JTAG boundary scan testing.</p> <p>When set LOW, <math>\overline{\text{CS\_TMS}}</math>, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured as GSPI pins for normal host interface operation.</p>
14	$\overline{\text{RESET}}$	Non Synchronous	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Used to reset the internal operating conditions to default setting or to reset the JTAG test sequence.</p> <p>Host Mode (JTAG/<math>\overline{\text{HOST}}</math> = LOW): When asserted LOW, all functional blocks will be set to default conditions and all output signals become high impedance with the exception of the STAT pins and the <math>\overline{\text{DATA\_ERROR}}</math> pin which will maintain the last state they were in for the duration that <math>\overline{\text{RESET}}</math> is asserted.</p> <p>JTAG Test Mode (JTAG/<math>\overline{\text{HOST}}</math> = HIGH): When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset.</p> <p>When set HIGH, normal operation of the JTAG test sequence resumes.</p> <p>NOTE: See <a href="#">Device Power Up on page 65</a> for power on reset requirements.</p>
15, 45	CORE_VDD	Non Synchronous	Input Power	<p>Power supply for digital logic blocks. Connect to +1.8V DC.</p> <p>NOTE: For power sequencing requirements please see <a href="#">Device Power Up on page 65</a>.</p>
16	$\overline{\text{CS\_TMS}}$	Synchronous with SCLK_TCK	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Chip Select / Test Mode Select</p> <p>Host Mode (JTAG/<math>\overline{\text{HOST}}</math> = LOW): <math>\overline{\text{CS\_TMS}}</math> operates as the host interface chip select, <math>\overline{\text{CS}}</math>, and is active LOW.</p> <p>JTAG Test Mode (JTAG/<math>\overline{\text{HOST}}</math> = HIGH): <math>\overline{\text{CS\_TMS}}</math> operates as the JTAG test mode select, TMS, and is active HIGH.</p>
17	SCLK_TCK	Non Synchronous	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Serial Data Clock / Test Clock. All JTAG / Host Interface address and data are shifted into/out of the device synchronously with this clock.</p> <p>Host Mode (JTAG/<math>\overline{\text{HOST}}</math> = LOW): SCLK_TCK operates as the host interface serial data clock, SCLK.</p> <p>JTAG Test Mode (JTAG/<math>\overline{\text{HOST}}</math> = HIGH): SCLK_TCK operates as the JTAG test clock, TCK.</p>
18, 48	CORE_GND	Non Synchronous	Input Power	<p>Ground connection for digital logic blocks. Connect to GND.</p>



**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Timing	Type	Description
19	SDOUT_TDO	Synchronous with SCLK_TCK	Output	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Serial Data Output / Test Data Output</p> <p>Host Mode (JTAG/<math>\overline{\text{HOST}}</math> = LOW): SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device.</p> <p>JTAG Test Mode (JTAG/<math>\overline{\text{HOST}}</math> = HIGH): SDOUT_TDO operates as the JTAG test data output, TDO.</p>
20	SDIN_TDI	Synchronous with SCLK_TCK	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Serial Data Input / Test Data Input</p> <p>Host Mode (JTAG/<math>\overline{\text{HOST}}</math> = LOW): SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device.</p> <p>JTAG Test Mode (JTAG/<math>\overline{\text{HOST}}</math> = HIGH): SDIN_TDI operates as the JTAG test data input, TDI.</p>
21, 29, 43	IO_VDD	Non Synchronous	Input Power	<p>Power supply for digital I/O.</p> <p>For a 3.3V tolerant I/O, connect pins to either +1.8V DC or +3.3V DC.</p> <p>For a 5V tolerant I/O, connect pins to a +3.3V DC.</p> <p>NOTE: For power sequencing requirements please see <a href="#">Device Power Up on page 65</a>.</p>
22	DATA_ERROR	Synchronous with PCLK	Output	<p>STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTTL compatible.</p> <p>The <math>\overline{\text{DATA\_ERROR}}</math> signal will be LOW when an error within the received data stream has been detected by the device. This pin is an inverted logical 'OR'ing of all detectable errors listed in the internal ERROR_STATUS register.</p> <p>Once an error is detected, <math>\overline{\text{DATA\_ERROR}}</math> will remain LOW until the start of the next video frame / field, or until the ERROR_STATUS register is read via the host interface.</p> <p>The <math>\overline{\text{DATA\_ERROR}}</math> signal will be HIGH when the received data stream has been detected without error.</p> <p>NOTE: It is possible to program which error conditions are monitored by the device by setting appropriate bits in the ERROR_MASK register HIGH. All error conditions are detected by default.</p>

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Timing	Type	Description
23, 25, 26, 27	STAT[0:3]	Synchronous with PCLK or RD_CLK	Output	<p>MULTI FUNCTION I/O PORT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Programmable multi-function outputs. By programming the bits in the IO_CONFIG register, each pin can output one of the following signals:</p> <ul style="list-style-type: none"> <li>• H</li> <li>• V</li> <li>• F</li> <li>• <math>\overline{\text{FIFO\_LD}}</math></li> <li>• ANC_DETECT</li> <li>• EDH_DETECT</li> <li>• FIFO_FULL</li> <li>• FIFO_EMPTY</li> </ul> <p>These pins are set to certain default values depending on the configuration of the device and the internal FIFO mode selected. See <a href="#">Programmable Multi-Function Outputs on page 57</a> for details.</p>
24, 28, 42	IO_GND	Non Synchronous	Input Power	Ground connection for digital I/O. Connect to GND.
30	RD_CLK	–	Input	<p>FIFO READ CLOCK Signal levels are LVCMOS / LVTTTL compatible.</p> <p>The application layer clocks the parallel data out of the FIFO on the rising edge of RD_CLK.</p>
31	$\overline{\text{RD\_RESET}}$	Synchronous with RD_CLK	Input	<p>FIFO READ RESET Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Valid input only when the device is in SMPTE mode (<math>\text{SMPTE\_BYPASS} = \text{HIGH}</math> and <math>\text{DVB-ASI} = \text{LOW}</math>), and the internal FIFO is configured for video mode (<a href="#">Video Mode on page 47</a>).</p> <p>A HIGH to LOW transition will reset the FIFO pointer to address zero of the memory.</p>
32 - 41	DOUT[0:9]	Synchronous with RD_CLK or PCLK	Output	<p>PARALLEL VIDEO DATA BUS Signal levels are LVCMOS / LVTTTL compatible.</p> <p>When the internal FIFO is enabled and configured for either video mode or DVB-ASI mode, parallel data will be clocked out of the device on the rising edge of RD_CLK.</p> <p>When the internal FIFO is in bypass mode, parallel data will be clocked out of the device on the rising edge of PCLK.</p> <p>DOUT9 is the MSB and DOUT0 is the LSB.</p>
44	PCLK	–	Output	<p>PIXEL CLOCK OUTPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>27MHz parallel clock output.</p>

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Timing	Type	Description
46	LOCKED	Synchronous with PCLK	Output	<p>STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>The LOCKED signal will be HIGH whenever the device has correctly received and locked to SMPTE compliant data in SMPTE mode or DVB-ASI compliant data in DVB-ASI mode, or when the reclocker has achieved lock in Data-Through mode.</p> <p>It will be LOW otherwise. When the signal is LOW, all digital output signals will be forced to logic LOW levels.</p>
47	DVB_ASI	Non Synchronous	Input / Output	<p>CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>This pin and its function are only supported in Manual mode (AUTO/<math>\overline{\text{MAN}}</math> = LOW).</p> <p>When set HIGH, the device will be configured to operate in DVB-ASI mode. The <math>\overline{\text{SMPTE\_BYPASS}}</math> pin will be ignored.</p> <p>When set LOW, the device will not support the decoding or word alignment of received DVB-ASI data.</p>
49	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input / Output	<p>CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>This pin is an input set in Manual mode, and an output set by the device in Auto mode.</p> <p>Auto Mode (AUTO/<math>\overline{\text{MAN}}</math> = HIGH): The <math>\overline{\text{SMPTE\_BYPASS}}</math> signal will be HIGH only when the device has locked to a SMPTE compliant data stream. It will be LOW otherwise. When the signal is LOW, no I/O processing features are available.</p> <p>Manual Mode (AUTO/<math>\overline{\text{MAN}}</math> = LOW): When set HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode.</p> <p>When the <math>\overline{\text{SMPTE\_BYPASS}}</math> pin is set LOW, the device will not support the descrambling, decoding, or word alignment of received SMPTE data. No I/O processing features will be available.</p>
50	AUTO/ $\overline{\text{MAN}}$	Non Synchronous	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>When set HIGH, the GS9090A will operate in Auto mode. The <math>\overline{\text{SMPTE\_BYPASS}}</math> pin becomes an output status signal set by the device. In this mode, the GS9090A will automatically detect, relock, deserialize, and process SMPTE compliant input data.</p> <p>When set LOW, the GS9090A will operate in Manual mode. The DVB_ASI and <math>\overline{\text{SMPTE\_BYPASS}}</math> pins become input control signals. In this mode, the pins must be set for the correct reception of either SMPTE or DVB-ASI data. Manual mode also supports the relocking and deserializing of data not conforming to SMPTE or DVB-ASI streams.</p>

**Table 1-1: Pin Descriptions (Continued)**

Pin Number	Name	Timing	Type	Description
51	FW_EN	Non Synchronous	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Used to enable or disable the noise immune flywheel of the device.</p> <p>When set HIGH, the internal flywheel is enabled. This flywheel is used in the extraction of timing signals, the generation of TRS signals, the automatic detection of video standards, and in manual switch line lock handling.</p> <p>When set LOW, the internal flywheel is disabled. Timing based TRS errors will not be detected.</p>
52	FIFO_EN	Non Synchronous	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTTL compatible.</p> <p>Used to enable / disable the internal FIFO.</p> <p>When FIFO_EN is HIGH, the internal FIFO will be enabled. Data will be clocked out of the device on the rising edge of the RD_CLK input pin if the FIFO is in video mode or DVB-ASI mode.</p> <p>When FIFO_EN is LOW, the internal FIFO is bypassed and parallel data is clocked out on the rising edge of the PCLK output.</p>
53	VCO_VDD	Analog	Input Power	<p>Power supply connection for Voltage-Controlled-Oscillator. Connect to +1.8V DC.</p>
54	LB_CONT	Analog	Input	<p>CONTROL SIGNAL INPUT Control voltage to fine-tune the loop bandwidth of the PLL.</p>
55	VCO_GND	Analog	Input Power	<p>Ground connection for Voltage-Controlled-Oscillator. Connect to GND.</p>
56	LF+	Analog	Input	<p>Loop filter component connection. Connect to pin 1 (LF-) as shown in <a href="#">Typical Application Circuit (Part B)</a> on page 68.</p>
–	Center Pad	–	Power	<p>Connect to GND following recommendations in <a href="#">Recommended PCB Footprint</a> on page 70</p>

## 2. Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +3.47V
Input Voltage Range (any input)	-2.0V to + 5.25V
Ambient Operating Temperature	-20°C ≤ T <sub>A</sub> ≤ 85°C
Storage Temperature	-40°C ≤ T <sub>STG</sub> ≤ 125°C
ESD protection on all pins (see Note 1)	1kV

NOTES:

1. HBM, per JESDA - 114B

### 2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V<sub>DD</sub> = 1.8V, T<sub>A</sub> = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
<b>System</b>							
Operating Temperature Range	T <sub>A</sub>	–	0	25	70	°C	1
Core power supply voltage	CORE_VDD	–	1.71	1.8	1.89	V	–
Digital I/O Buffer Power Supply Voltage	IO_VDD	1.8V Operation	1.71	1.8	1.89	V	–
	IO_VDD	3.3V Operation	3.13	3.3	3.47	V	–
PLL Power Supply Voltage	PLL_VDD	–	1.71	1.8	1.89	V	–
Input Buffer Power Supply Voltage	BUFF_VDD	1.8V Operation	1.71	1.8	1.89	V	–
	BUFF_VDD	3.3V Operation	3.13	3.3	3.47	V	–
VCO Power Supply Voltage	VCO_VDD	–	1.71	1.8	1.89	V	–
Typical System Power	P <sub>D</sub>	CORE_VDD = 1.8V IO_VDD = 1.8V T = 25°C	–	145	–	mW	–
Max. System Power	P <sub>D</sub>	CORE_VDD = 1.89V IO_VDD = 3.47V T = 70°C	–	–	270	mW	–



**Table 2-2: DC Electrical Characteristics (Continued)**

$V_{DD} = 1.8V$ ,  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ , unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
<b>Digital I/O</b>							
Input Voltage, Logic LOW	$V_{IL}$	1.8V Operation or 3.3V Operation	–	–	$0.35 \times IO\_VDD$	V	–
Input Voltage, Logic HIGH	$V_{IH}$	1.8V Operation or 3.3V Operation	$0.65 \times IO\_VDD$	–	–	V	–
Output Voltage, Logic LOW	$V_{OL}$	$I_{OL} = 8mA @ 3.3V$ , $4mA @ 1.8V$	–	–	0.4	V	–
Output Voltage, Logic HIGH	$V_{OH}$	$I_{OL} = -8mA @ 3.3V$ , $-4mA @ 1.8V$	$IO\_VDD - 0.4$	–	–	V	–
<b>Serial Digital Input</b>							
Input Common Mode Voltage Range	$V_{CMIN}$	BUFF_VDD connected to 3.3V supply	$BUFF\_GND + (V_{DIFF} / 2)$	–	$BUFF\_VDD - (V_{DIFF} / 2)$	V	–
Input Termination Resistance	$R_{IN}$	–	37.5	50	62.5	$\Omega$	–

**NOTES**

1. All DC and AC electrical parameters within specification.
2. Guaranteed functional.

## 2.3 AC Electrical Characteristics

**Table 2-3: AC Electrical Characteristics**

$V_{DD} = 1.8V$ ,  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ , unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
<b>System</b>							
Asynchronous Lock Time (LOCKED signal set HIGH)	$t_{LOCK}$	Input jitter of 0.2UI, No data to SMPTE, $\overline{SMPTE\_BYPASS} = HIGH$ DVB_ASI = LOW, at 25°C	–	–	235	us	1
Asynchronous Lock Time (LOCKED signal set HIGH)	$t_{LOCK}$	Input jitter of 0.2UI, No data to DVB-ASI, $\overline{SMPTE\_BYPASS} = HIGH$ DVB_ASI = HIGH, at 25°C	–	–	185	us	1
Asynchronous Lock Time (LOCKED signal set HIGH)	$t_{LOCK}$	Input jitter of 0.2UI, No data to non-SMPTE, $\overline{SMPTE\_BYPASS} = LOW$ DVB_ASI = LOW, at 25°C	–	–	165	us	1

**Table 2-3: AC Electrical Characteristics (Continued)**V<sub>DD</sub> = 1.8V, T<sub>A</sub> = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
<b>Serial Digital Input</b>							
Serial Input Data Rate	DR <sub>SDI</sub>	–	–	270	–	Mb/s	–
Serial Input Jitter Tolerance	IJT	–	–	0.5	–	UI	2
Differential Input Voltage Range	–	BUFF_VDD = 1.8V	200	800	1700	mV <sub>p-p</sub>	–
	–	BUFF_VDD = 3.3V	100	800	2200	mV <sub>p-p</sub>	–
<b>Parallel Output</b>							
Parallel Output Clock Frequency	f <sub>PCLK</sub>	–	–	27	–	MHz	–
Parallel Output Clock Duty Cycle	DC <sub>PCLK</sub>	–	40	–	60	%	–
Variation of Parallel Output Clock (from 27MHz)	–	Device Unlocked T <sub>A</sub> = -20°C to +85°C IO_VDD = 1.8V	-7.5	–	+7.5	%	3
Output Data Hold Time	t <sub>OH</sub>	With 15pF load	3.0	–	–	ns	4
Output Delay Time	t <sub>OD</sub>	With 15pF load	–	–	10.0	ns	4
<b>GSPI</b>							
GSPI Input Clock Frequency	f <sub>GSPI</sub>	–	–	–	54.0	MHz	–
GSPI Clock Duty Cycle	DC <sub>GSPI</sub>	–	40	–	60	%	–
GSPI Setup Time	t <sub>GS</sub>	–	1.5	–	–	ns	–
GSPI Hold Time	t <sub>GH</sub>	–	–	–	1.5	ns	–

**NOTES**

1. No signal to signal present, or a switch from another data rate to 270Mb/s.
2. Power supply noise 50mV<sub>pp</sub> at 15kHz, 100kHz, 1MHz sinusoidal modulation.
3. When the serial input to the GS9090A is removed, the PCLK output signal will continue to operate at 27MHz and the internal VCO will remain at this frequency within +/- 7.5% over the range -20°C to +85°C.
4. Timing includes the following outputs: DOUT[9:0], STAT[3:0]. When the FIFO is enabled, the outputs are measured with respect to RD\_CLK.

## 2.4 Host Interface Map

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_LD_POSITION[12:0]	28h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	27h																
	26h																
ERROR_MASK_REGISTER	25h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ER R_MASK	FF_CRC_ER R_MASK	AP_CRC_ER R_MASK	LOCK_ERR _MASK	CCS_ERR_ MASK	SAV_ERR_ MASK	EAV_ERR_ MASK
FF_PIXEL_END_F1[12:0]	24h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE4[10:0]	14h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B(4,3)	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A(2,1)	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
ANC_TYPE(5)[15:0]	0Eh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(4)[15:0]	0Dh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(3)[15:0]	0Ch	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(2)[15:0]	0Bh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(1)[15:0]	0Ah	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_B[10:0]	09h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_EMPTY_OFFSET	06h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h	Not Used	Not Used	Not Used	ANC_DATA_SWITCH	STAT3_CONFIG b2	STAT3_CONFIG b1	STAT3_CONFIG b0	STAT2_CONFIG b2	STAT2_CONFIG b1	STAT2_CONFIG b0	STAT1_CONFIG b2	STAT1_CONFIG b1	STAT1_CONFIG b0	STAT0_CONFIG b2	STAT0_CONFIG b1	STAT0_CONFIG b0
DATA_FORMAT	04h	Not Used	Not Used	Not Used	Not Used	EDH_FLAG_UPDATE	AP_CRC_V	FF_CRC_V	EDH_DETECT	VERSION_352M	Not Used	Not Used	STD_LOCK	DATA_FORMAT b3	DATA_FORMAT b2	DATA_FORMAT b1	DATA_FORMAT b0
EDH_FLAG_OUT	03h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
EDH_FLAG_IN	02h	Not Used	ANC-UES_IN	ANC-IDA_IN	ANC-IDH_IN	ANC-EDA_IN	ANC-EDH_IN	FF-UES_IN	FF-IDA_IN	FF-IDH_IN	FF-EDA_IN	FF-EDH_IN	AP-UES_IN	AP-IDA_IN	AP-IDH_IN	AP-EDA_IN	AP-EDH_IN
ERROR_STATUS	01h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR	CCS_ERR	SAV_ERR	EAV_ERR
IOPROC_DISABLE	00h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	ANC_PKT_EXT	FIFO_MODE b1	FIFO_MODE b0	H_CONFIG	Not Used	Not Used	ILLEGAL_REMAP	EDH_CRC_INS	ANC_CSUM_INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

## 2.4.1 Host Interface Map (R/W registers)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_LD_POSITION[12:0]	28h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	27h																
	26h																
ERROR_MASK_REGISTER	25h										VD_STD_ERR_MASK	FF_CRC_ERR_MASK	AP_CRC_ERR_MASK	LOCK_ERR_MASK	CCS_ERR_MASK	SAV_ERR_MASK	EAV_ERR_MASK
FF_PIXEL_END_F1[12:0]	24h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	14h																
	13h																
	12h																
	11h																
	10h																
	0Fh																
ANC_TYPE(5)[15:0]	0Eh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(4)[15:0]	0Dh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(3)[15:0]	0Ch	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(2)[15:0]	0Bh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(1)[15:0]	0Ah	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_B[10:0]	09h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0





Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_EMPTY_OFFSET	06h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h				ANC_DATA_SWITCH	STAT3_CONFIG b2	STAT3_CONFIG b1	STAT3_CONFIG b0	STAT2_CONFIG b2	STAT2_CONFIG b1	STAT2_CONFIG b0	STAT1_CONFIG b2	STAT1_CONFIG b1	STAT1_CONFIG b0	STAT0_CONFIG b2	STAT0_CONFIG b1	STAT0_CONFIG b0
DATA_FORMAT	04h					EDH_FLAG_UPDATE											
	03h																
	02h																
	01h																
IOPROC_DISABLE	00h							ANC_PKT_EXT	FIFO_MODE b1	FIFO_MODE b0	H_CONFIG			ILLEGAL_R EMAP	EDH_CRC_INS	ANC_CSUM_INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

## 2.4.2 Host Interface Map (Read only registers)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	28h																
	27h																
	26h																
	25h																
	24h																
	23h																
	22h																
	21h																
	20h																
	1Fh																
	1Eh																
	1Dh																
	1Ch																
	1Bh																
	1Ah																
	19h																
	18h																
	17h																
	16h																
	15h																
RASTER_STRUCTURE4[10:0]	14h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B(4,3)	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A(2,1)	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
	09h																
	08h																
	07h																

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	06h																
	05h																
DATA_FORMAT	04h						AP_CRC_V	FF_CRC_V	EDH_DETECT	VERSION_352M			STD_LOCK	DATA_FORMAT_b3	DATA_FORMAT_b2	DATA_FORMAT_b1	DATA_FORMAT_b0
EDH_FLAG_OUT	03h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
EDH_FLAG_IN	02h	Not Used	ANC-UES_IN	ANC-IDA_IN	ANC-IDH_IN	ANC-EDA_IN	ANC-EDH_IN	FF-UES_IN	FF-IDA_IN	FF-IDH_IN	FF-EDA_IN	FF-EDH_IN	AP-UES_IN	AP-IDA_IN	AP-IDH_IN	AP-EDA_IN	AP-EDH_IN
ERROR_STATUS	01h										VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR	CCS_ERR	SAV_ERR	EAV_ERR
	00h																

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see [Section 3.10.3](#)).

## 3. Detailed Description

- [Functional Overview on page 21](#)
- [Serial Digital Input on page 22](#)
- [Clock and Data Recovery on page 22](#)
- [Serial-To-Parallel Conversion on page 22](#)
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- [SMPTE Functionality on page 26](#)
- [DVB-ASI Functionality on page 29](#)
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- [Parallel Data Outputs on page 56](#)
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### 3.1 Functional Overview

The GS9090A is a 270Mb/s reclocking deserializer with an internal FIFO and programmable multi-function output port. The device has two basic modes of operation which determine precisely how SMPTE or DVB-ASI compliant input data streams are reclocked and processed.

In Auto mode ( $\text{AUTO}/\overline{\text{MAN}} = \text{HIGH}$ ), the GS9090A will automatically detect, reclock, deserialize, and process SD SMPTE 259M-C input data.

In Manual mode ( $\text{AUTO}/\overline{\text{MAN}} = \text{LOW}$ ), the external device pins must be set for the correct reception of either SMPTE or DVB-ASI data. Manual mode also supports the reclocking and deserializing of 270Mb/s data not conforming to SMPTE or DVB-ASI streams.

The digital signal processing core implements several data processing functions including error detection and correction and automatic video standards detection. These features are all enabled by default, but may be individually disabled via internal registers accessible through the GSPI host interface.

The provided programmable multi-function output pins may be configured to output various status signals including H, V, and F timing, ancillary data detection, EDH detection, and a FIFO load pulse. The internal FIFO supports 4 modes of operation, which may be used for data alignment / delay, MPEG packet extraction, or ancillary data extraction.

The GS9090A contains a JTAG interface for boundary scan test implementations.

## 3.2 Serial Digital Input

The GS9090A contains a current mode differential serial digital input buffer. The input buffer has internal 50Ω termination resistors, which are connected to ground via the TERM pin.

If the input signal is AC coupled to the device, the signal source common mode level will be set internally to typically 1.45V. If the input signal is DC coupled to the device, the internal biasing will be ignored. Please see [AC Electrical Characteristics on page 13](#) for Common Mode range and swing characteristics.

## 3.3 Clock and Data Recovery

The GS9090A contains an integrated clock and data recovery block. The function of this block is to lock to the input data stream, extract a clean clock, and retime the serial digital data to remove high frequency jitter.

### 3.3.1 Internal VCO and Phase Detector

The GS9090A uses an internal VCO and PFD as part of the internal clock and data recovery block's phase-locked loop. Each block requires a +1.8V DC power supply, which is supplied via the VCO\_VDD / VCO\_GND and PLL\_VDD / PLL\_GND pins.

## 3.4 Serial-To-Parallel Conversion

The retimed data and phase-locked clock signals from the internal clock and data recovery block are fed to the serial-to-parallel converter. The function of this block is to extract 10-bit parallel data words from the reclocked serial data stream and simultaneously present them to the SMPTE and DVB-ASI word alignment blocks.

## 3.5 Modes Of Operation

The GS9090A has two basic modes of operation: Auto mode and Manual mode. Auto mode is enabled when the AUTO/ $\overline{\text{MAN}}$  pin is set HIGH, and Manual mode is enabled when the AUTO/ $\overline{\text{MAN}}$  pin is set LOW. As indicated in [Figure 3-1](#), DVB\_ASI and data-through are only supported in Manual mode.



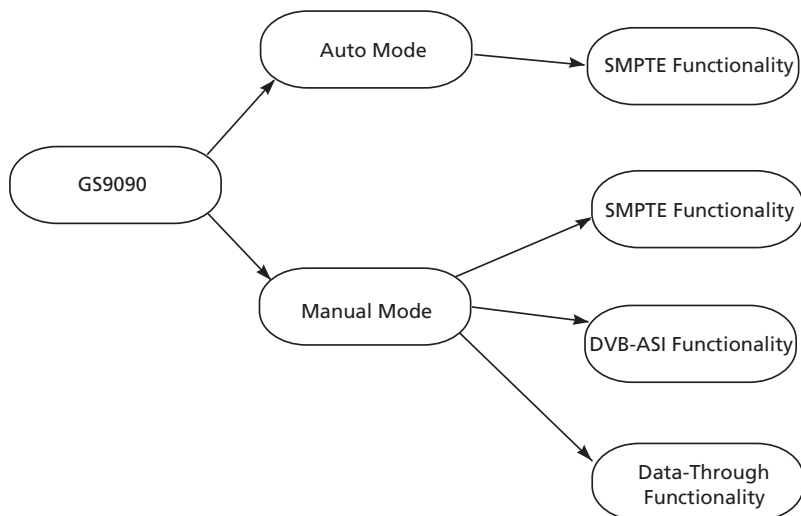


Figure 3-1: GS9090A's Modes of Operation

### 3.5.1 Lock Detect

Once the internal reclocker has locked to the received serial digital data stream, the lock detect block of the GS9090A searches for the appropriate sync words, and indicates via the LOCKED output pin when the device has successfully achieved lock. The LOCKED pin is designed to be stable. It will not toggle during the locking process, nor will it glitch during a synchronous switch.

Lock detection is a continuous process, which begins after a system reset and continues until the device is powered down or held in reset. This process is summarized in [Figure 3-2](#).

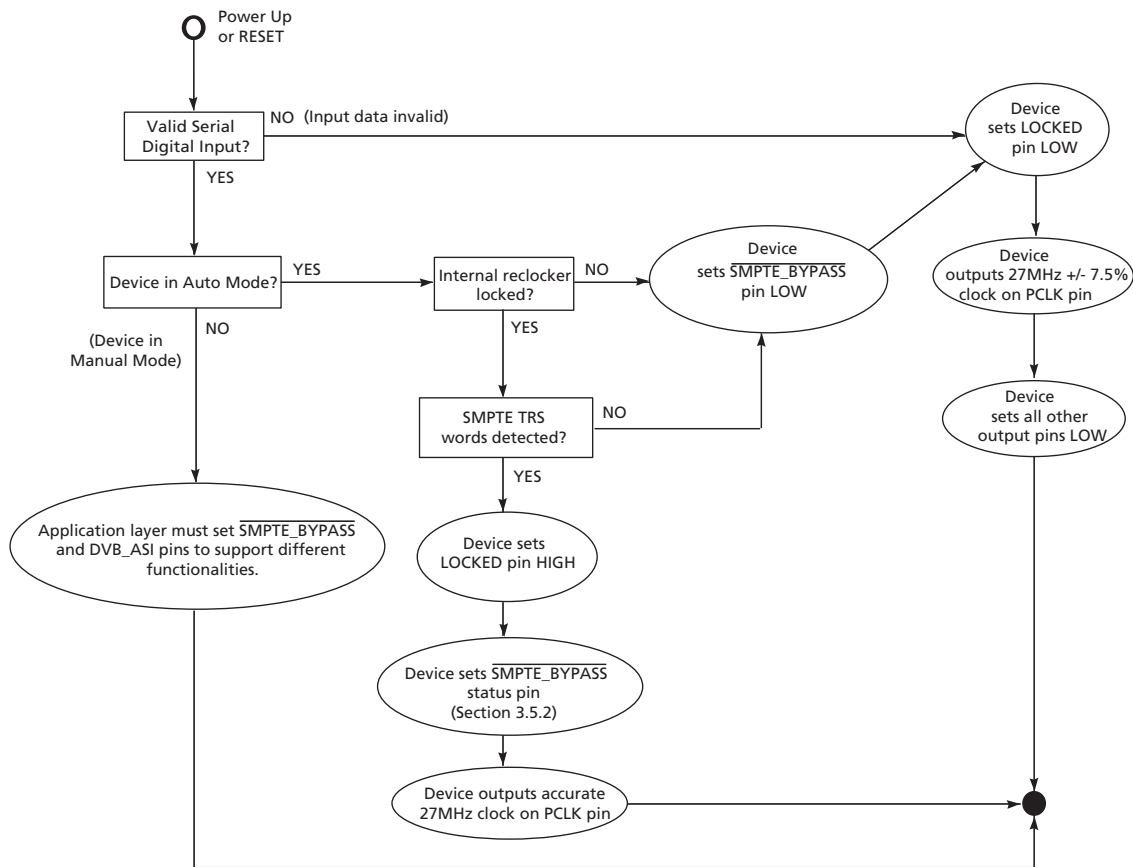


Figure 3-2: Lock Detection Process

The lock detection algorithm first determines if a valid serial digital input signal has been presented to the device by sampling the internal carrier\_detect signal. When the serial data input is considered invalid the LOCKED pin will be set LOW, and all device outputs will be forced LOW, except PCLK. The PCLK output frequency will be 27MHz +/- 7.5% over the temperature range of -20°C to +85°C.

If a valid serial digital input signal has been detected, and the device is in Auto mode, the lock algorithm will attempt to detect the presence of SMPTE TRS words. Assuming that a valid 270Mb/s SMPTE signal has been applied to the device, the LOCKED pin will be set HIGH and the synchronous and asynchronous lock times will be as listed in the [AC Electrical Characteristics](#) table.

In Manual mode, the SMPTE\_BYPASS and DVB\_ASI pins must be set appropriately so that the lock detect block will search for either SMPTE TRS or DVB-ASI sync words. Synchronous and asynchronous lock times are also listed in the [AC Electrical Characteristics](#) table.

NOTE: The PCLK output will continue to operate at 27MHz +/- 7.5% during the lock detection process. Only when the device is locked (LOCKED = HIGH) will the PCLK output an accurate 27MHz signal.

For SMPTE and DVB-ASI inputs, the lock detect block will only assert the LOCKED output pin HIGH if (1) the reclocker has locked to the input data stream, and (2) TRS or DVB-ASI sync words have been correctly identified.

For serial inputs that do not conform to SMPTE or DVB-ASI formats, one of the following will occur once the reclocker has locked:

1. In Manual mode, data will be passed directly to the parallel outputs without any further processing taking place and the LOCKED signal will be asserted HIGH if and only if the  $\overline{\text{SMPTE\_BYPASS}}$  and DVB\\_ASI input pins are set LOW (see [Data-Through functionality on page 30](#)); or
2. In Auto mode, the LOCKED signal will be asserted LOW, the parallel outputs will be set to logic LOW, and the  $\overline{\text{SMPTE\_BYPASS}}$  signal will also be set LOW.

If the internal reclocker does not lock to the input, the internal pll\_lock signal will be LOW, and the lock detect block will not search for sync words. The LOCKED signal will be set LOW, and all device outputs except PCLK will be forced LOW. The PCLK output frequency will be 27MHz +/- 7.5% over the temperature range of -20°C to +85°C.

### 3.5.2 Auto Mode

Recall that the GS9090A is in Auto mode when the AUTO/ $\overline{\text{MAN}}$  input pin is set HIGH. In this mode,  $\overline{\text{SMPTE\_BYPASS}}$  becomes an output status pin. [Table 3-1](#) shows the status of this pin when different serial digital video signals are applied.

**Table 3-1: Auto Mode Output Status Signals**

Format	Pin Settings
	$\overline{\text{SMPTE\_BYPASS}}$
SD SMPTE	HIGH
NOT SMPTE	LOW