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GS9090B GenLINX® III 270Mb/s Deserializer for SDI

Key Features

- SMPTE 259M-C compliant descrambling and NRZI to NRZ decoding (with bypass)
- DVB-ASI 8b/10b decoding
- Integrated line-based FIFO for data alignment/delay, clock phase interchange, DVB-ASI data packet extraction and clock rate interchange, and ancillary data packet extraction
- Integrated VCO and reclocker
- User selectable additional processing features including:
  - TRS, ANC data checksum, and EDH CRC error detection and correction
  - programmable ANC data detection
  - illegal code remapping
- Internal flywheel for noise immune H, V, F extraction
- Automatic standards detection and indication
- Enhanced Gennum Serial Peripheral Interface (GSPI)
- JTAG test interface
- Polarity insensitive for DVB-ASI and SMPTE signals
- +1.8V core power supply with optional +1.8V or +3.3V I/O power supply
- Small footprint (8mm x 8mm)
- Low power operation (typically 145mW)
- Pb-free

Applications

- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS9090B is a 270Mb/s reclocking deserializer with an internal FIFO. It provides a complete receive solution for SD-SDI and DVB-ASI applications.

In addition to reclocking and deserializing the input data stream, the GS9090B performs NRZI-to-NRZ decoding, descrambling as per SMPTE 259M-C, and word alignment when operating in SMPTE mode. When operating in DVB-ASI mode, the device will word align the data to K28.5 sync characters and 8b/10b decode the received stream.

The internal reclocker features a very wide input jitter tolerance, and is fully compatible with both SMPTE and DVB-ASI input streams.

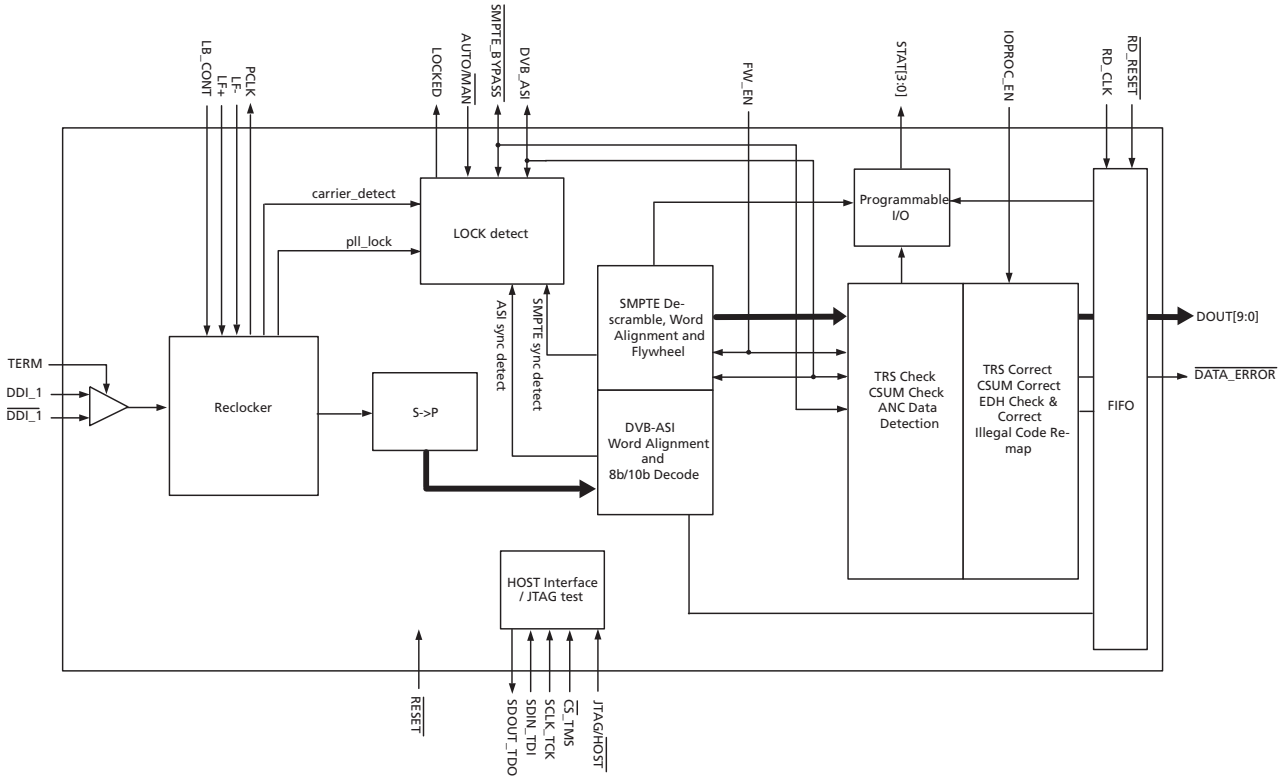
The GS9090B includes a range of data processing functions such as EDH support (error detection and handling), and automatic standards detection. The device can also detect and extract SMPTE 352M payload identifier packets and independently identify the received video standard. This information is read from internal registers via the host interface port.

The GS9090B also incorporates a video line-based FIFO. This FIFO may be used in four user-selectable modes to carry out tasks such as data alignment / delay, clock phase interchange, MPEG packet extraction and clock rate interchange, and ancillary data packet extraction.

Parallel data outputs are provided in 10-bit multiplexed format, with the associated parallel clock output signal operating at 27MHz.

The device may also be used in a low-latency data pass through mode where only descrambling and word alignment will be performed in SMPTE mode.

Functional Block Diagram



GS9090B Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
5	154185	–	May 2010	Converted document back to Data Sheet.
4	152803	–	October 2009	Changed 6.1 Package Dimensions.
3	150198	50711	July 2008	DVB_ASI operation specification change in Master mode.
2	143668	–	January 2007	Added DVB-ASI payload data rate parameter to Table 2-3: AC Electrical Characteristics.
1	143101	–	December 2006	Converting to data sheet. Removed 'Proprietary and Confidential' footer. Added section.
0	141913	–	September 2006	New Document.

Contents

1. Pin Out

1.1 Pin Assignment

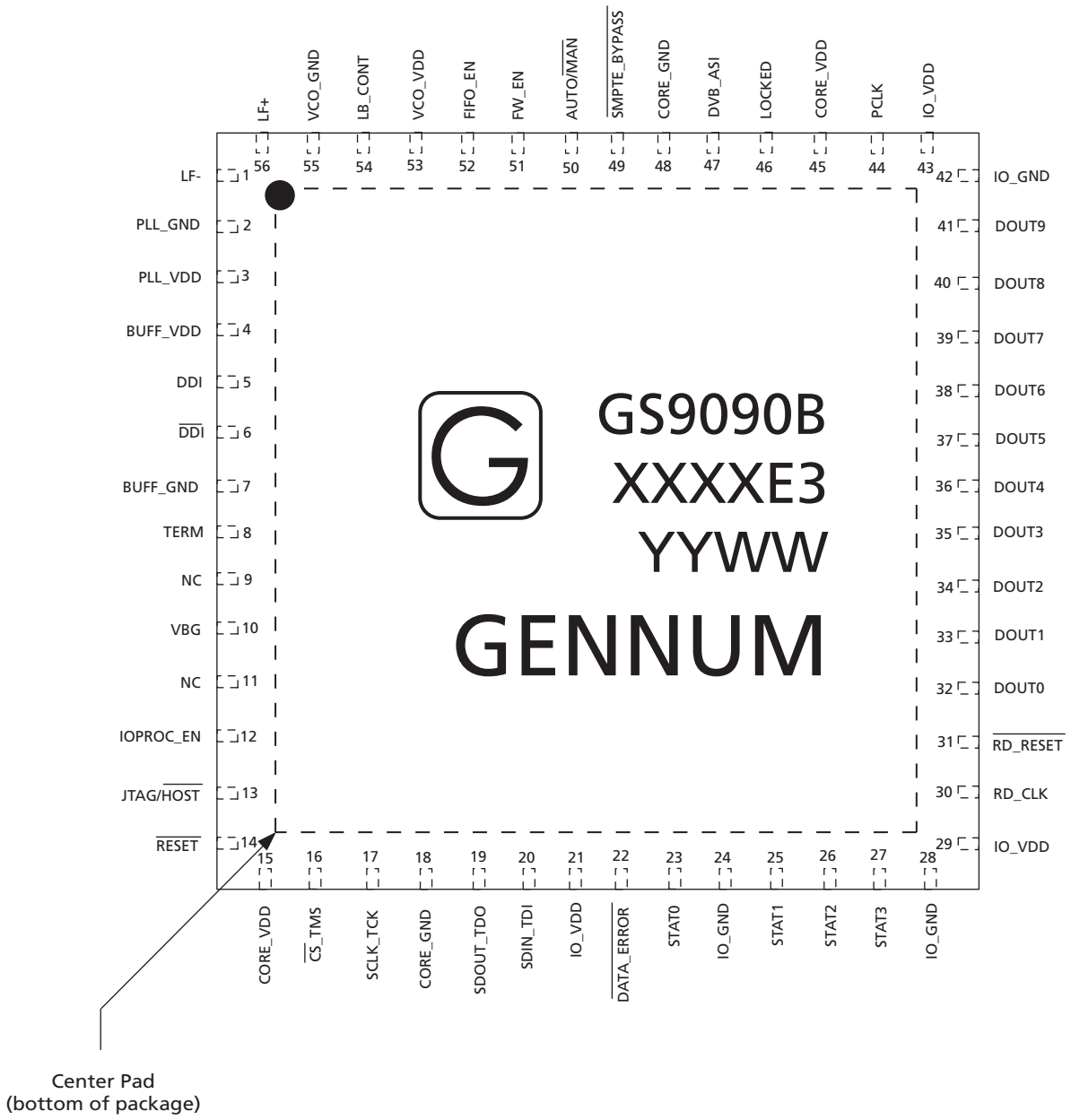


Figure 1-1: Pin Assignment

Table 1-1: Pin List and Description

Pin Number	Name	Timing	Type	Description
1	LF-	Analog	Input	Loop filter component connection. Connect to pin 56 (LF+) as shown in Typical Application Circuit (Part B) on page 68.
2	PLL_GND	Analog	Input Power	Ground connection for phase-locked loop. Connect to GND.
3	PLL_VDD	Analog	Input Power	Power supply connection for phase-locked loop. Connect to +1.8V DC.
4	BUFF_VDD	Analog	Input Power	Power supply connection for digital input buffers. When DDI/$\overline{\text{DDI}}$ are AC coupled, this pin should be left unconnected. When DDI/$\overline{\text{DDI}}$ are DC coupled, this pin should be connected to +3.3V as shown in Typical Application Circuit (Part B) on page 68. See Serial Digital Input on page 22 for more details.
5, 6	DDI, $\overline{\text{DDI}}$	Analog	Input	Serial digital differential input pair.
7	BUFF_GND	Analog	Input Power	Ground connection for serial digital input buffer. Connect to GND.
8	TERM	Analog	Input	Termination for serial digital input. AC couple to BUFF_GND
9, 11	NC	–	–	No connect.
10	VBG	Analog	Input	Bandgap filter capacitor. Connect to GND as shown in Typical Application Circuit (Part B) on page 68.
12	IOPROC_EN	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal Levels are LVCMOS / LVTTL compatible. Used to enable or disable the I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • Illegal Code Remapping • EDH CRC Error Correction • Ancillary Data Checksum Error Correction • TRS Error Correction • EDH Flag Detection To enable a subset of these features, keep the IOPROC_EN pin HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When set LOW, the device will enter low-latency mode. NOTE: When the internal FIFO is configured for Video mode or Ancillary Data Extraction mode, the IOPROC_EN pin must be set HIGH (see Internal FIFO Operation on page 47).
13	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{\text{CS}}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured as GSPI pins for normal host interface operation.

Table 1-1: Pin List and Description (Continued)

14	$\overline{\text{RESET}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to reset the internal operating conditions to default setting or to reset the JTAG test sequence. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): When asserted LOW, all functional blocks will be set to default conditions and all output signals become high impedance with the exception of the STAT pins and the $\overline{\text{DATA\_ERROR}}$ pin which will maintain the last state they were in for the duration that $\overline{\text{RESET}}$ is asserted. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes. NOTE: See Device Power Up on page 64 for power on reset requirements.
15, 45	CORE_VDD	Non Synchronous	Input Power	Power supply for digital logic blocks. Connect to +1.8V DC. NOTE: For power sequencing requirements please see Device Power Up on page 64.
16	$\overline{\text{CS}}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Chip Select / Test Mode Select Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): $\overline{\text{CS}}$_TMS operates as the host interface chip select, $\overline{\text{CS}}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): $\overline{\text{CS}}$_TMS operates as the JTAG test mode select, TMS, and is active HIGH.
17	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Clock / Test Clock. All JTAG / Host Interface address and data are shifted into/out of the device synchronously with this clock. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): SCLK_TCK operates as the host interface serial data clock, SCLK. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): SCLK_TCK operates as the JTAG test clock, TCK.
18, 48	CORE_GND	Non Synchronous	Input Power	Ground connection for digital logic blocks. Connect to GND.
19	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): SDOUT_TDO operates as the JTAG test data output, TDO.

Table 1-1: Pin List and Description (Continued)

20	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Input / Test Data Input Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): SDIN_TDI operates as the JTAG test data input, TDI.
21, 29, 43	IO_VDD	Non Synchronous	Input Power	Power supply for digital I/O. For a 3.3V tolerant I/O, connect pins to either +1.8V DC or +3.3V DC. For a 5V tolerant I/O, connect pins to a +3.3V DC. NOTE: For power sequencing requirements please see Device Power Up on page 64.
22	$\overline{\text{DATA\_ERROR}}$	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. The $\overline{\text{DATA\_ERROR}}$ signal will be LOW when an error within the received data stream has been detected by the device. This pin is an inverted logical 'OR'ing of all detectable errors listed in the internal ERROR_STATUS register. Once an error is detected, $\overline{\text{DATA\_ERROR}}$ will remain LOW until the start of the next video frame / field, or until the ERROR_STATUS register is read via the host interface. The $\overline{\text{DATA\_ERROR}}$ signal will be HIGH when the received data stream has been detected without error. NOTE: It is possible to program which error conditions are monitored by the device by setting appropriate bits in the ERROR_MASK register HIGH. All error conditions are detected by default.
23, 25, 26, 27	STAT[0:3]	Synchronous with PCLK or RD_CLK	Output	MULTI FUNCTION I/O PORT Signal levels are LVCMOS / LVTTL compatible. Programmable multi-function outputs. By programming the bits is the IO_CONFIG register, each pin can output one of the following signals: • H • V • F • $\overline{\text{FIFO\_LD}}$ • ANC_DETECT • EDH_DETECT • FIFO_FULL • FIFO_EMPTY These pins are set to certain default values depending on the configuration of the device and the internal FIFO mode selected. See Programmable Multi-Function Outputs on page 56 for details.
24, 28, 42	IO_GND	Non Synchronous	Input Power	Ground connection for digital I/O. Connect to GND.

Table 1-1: Pin List and Description (Continued)

30	RD_CLK	–	Input	FIFO READ CLOCK Signal levels are LVCMOS / LVTTL compatible. The parallel data will be clocked out of the FIFO on the rising edge of RD_CLK.
31	$\overline{\text{RD\_RESET}}$	Synchronous with RD_CLK	Input	FIFO READ RESET Signal levels are LVCMOS / LVTTL compatible. Valid input only when the device is in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB-ASI = LOW), and the internal FIFO is configured for video mode (See Video Mode on page 47). A HIGH to LOW transition will reset the FIFO pointer to address zero of the memory.
32 - 41	DOUT[0:9]	Synchronous with RD_CLK or PCLK	Output	PARALLEL VIDEO DATA BUS Signal levels are LVCMOS / LVTTL compatible. When the internal FIFO is enabled and configured for either video mode or DVB-ASI mode, parallel data will be clocked out of the device on the rising edge of RD_CLK. When the internal FIFO is in bypass mode, parallel data will be clocked out of the device on the rising edge of PCLK. DOUT9 is the MSB and DOUT0 is the LSB.
44	PCLK	–	Output	PIXEL CLOCK OUTPUT Signal levels are LVCMOS / LVTTL compatible. 27MHz parallel clock output.
46	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. The LOCKED signal will be HIGH whenever the device has correctly received and locked to SMPTE compliant data in SMPTE mode or DVB-ASI compliant data in DVB-ASI mode, or when the reclocker has achieved lock in Data-Through mode. It will be LOW otherwise. When the signal is LOW, all digital output signals will be forced to logic LOW levels.
47	DVB_ASI	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. This pin and its function are only supported in Manual mode (AUTO/$\overline{\text{MAN}}$ = LOW). When this pin is set HIGH, the device will be configured to operate in DVB-ASI mode. The $\overline{\text{SMPTE\_BYPASS}}$ pin will be ignored. When set LOW, the device will not support the decoding or word alignment of received DVB-ASI data.

Table 1-1: Pin List and Description (Continued)

49	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. This pin is an input in Manual mode, and an output set by the device in Auto mode. Auto Mode (AUTO/$\overline{\text{MAN}}$ = HIGH): The $\overline{\text{SMPTE\_BYPASS}}$ signal will be HIGH only when the device has locked to a SMPTE compliant data stream. It will be LOW otherwise. When the signal is LOW, no I/O processing features are available. Manual Mode (AUTO/$\overline{\text{MAN}}$ = LOW): When this pin is set HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode. When the $\overline{\text{SMPTE\_BYPASS}}$ pin is set LOW, the device will not support the descrambling, decoding, or word alignment of received SMPTE data. No I/O processing features will be available.
50	AUTO/$\overline{\text{MAN}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. When set HIGH, the GS9090B will operate in Auto mode. The $\overline{\text{SMPTE\_BYPASS}}$ pin becomes an output status signal set by the device. In this mode, the GS9090B will automatically detect, reclock, deserialize, and process SMPTE compliant input data. When set LOW, the GS9090B will operate in Manual mode. The DVB_ASI and $\overline{\text{SMPTE\_BYPASS}}$ pins become input control signals. In this mode, these two external pins must be set for the correct reception of either SMPTE or DVB-ASI data. Manual mode also supports the reclocking and deserializing of data not conforming to SMPTE or DVB-ASI streams.
51	FW_EN	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable or disable the noise immune flywheel of the device. When set HIGH, the internal flywheel is enabled. This flywheel is used in the extraction of timing signals, the generation of TRS signals, the automatic detection of video standards, and in manual switch line lock handling. When set LOW, the internal flywheel is disabled. Timing based TRS errors will not be detected.
52	FIFO_EN	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable / disable the internal FIFO. When FIFO_EN is HIGH, the internal FIFO will be enabled. Data will be clocked out of the device on the rising edge of the RD_CLK input pin if the FIFO is in video mode or DVB-ASI mode. When FIFO_EN is LOW, the internal FIFO is bypassed and parallel data is clocked out on the rising edge of the PCLK output.

Table 1-1: Pin List and Description (Continued)

53	VCO_VDD	Analog	Input Power	Power supply connection for Voltage-Controlled-Oscillator. Connect to +1.8V DC.
54	LB_CONT	Analog	Input	CONTROL SIGNAL INPUT Control voltage to fine-tune the loop bandwidth of the PLL.
55	VCO_GND	Analog	Input Power	Ground connection for Voltage-Controlled-Oscillator. Connect to GND.
56	LF+	Analog	Input	Loop filter component connection. Connect to pin 1 (LF-) as shown in Typical Application Circuit (Part B) on page 68.
–	Center Pad	–	Power	Connect to GND following recommendations in Recommended PCB Footprint on page 70

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +3.47V
Input Voltage Range (any input)	-2.0V to + 5.25V
Ambient Operating Temperature	$-20°C \leq T_A \leq 85°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
ESD protection on all pins (see Note 1)	1kV
Solder Reflow Temperature	260°C
NOTES: 1. HBM, per JESD22 - A114B	

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.

2.2 DC Characteristics

Table 2-2: DC Electrical Characteristics

V_{DD} = 1.8V ±5%, 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise specified. Typical values: V_{CC} = 1.8V, 3.3V and T_A =25°C

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Core Power Supply Voltage	CORE_VDD	–	1.71	1.8	1.89	V	–
Digital I/O Buffer Power Supply Voltage	IO_VDD	1.8V Operation	1.71	1.8	1.89	V	–
	IO_VDD	3.3V Operation	3.13	3.3	3.47	V	–
PLL Power Supply Voltage	PLL_VDD	–	1.71	1.8	1.89	V	–
VCO Power Supply Voltage	VCO_VDD	–	1.71	1.8	1.89	V	–
Typical System Power	P_D	CORE_VDD = 1.8V IO_VDD = 1.8V T = 25°C	–	145	–	mW	–
Max. System Power	P_D	CORE_VDD = 1.89V IO_VDD = 3.47V T = 70°C	–	–	270	mW	–

Table 2-2: DC Electrical Characteristics (Continued)

V_{DD} = 1.8V ±5%, 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise specified. Typical values: V_{CC} = 1.8V, 3.3V and T_A =25°C

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
Digital I/O							
Input Voltage, Logic LOW	V_{IL}	1.8V Operation or 3.3V Operation	–	–	0.35 x IO_VDD	V	–
Input Voltage, Logic HIGH	V_{IH}	1.8V Operation or 3.3V Operation	0.65 x IO_VDD	–	–	V	–
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 8mA @ 3.3V, 4mA @ 1.8V	–	–	0.4	V	–
Output Voltage, Logic HIGH	V_{OH}	I_{OL} = -8mA @ 3.3V, -4mA @ 1.8V	IO_VDD - 0.4	–	–	V	–
Serial Digital Inputs							
Input Common Mode Voltage	V_{CMIN}	BUFF_VDD connected to 3.3V supply	BUFF_GND + (V_{DIFF} / 2)	–	BUFF_VDD - (V_{DIFF} / 2)	V	–
Input Termination Resistance	R_{IN}	–	37.5	50	62.5	Ω	–

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

V_{DD} = 1.8V ±5%, 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise specified. Typical values: V_{CC} = 1.8V, 3.3V and T_A =25°C

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Asynchronous Lock Time (LOCKED signal set HIGH)	t_{LOCK}	Input jitter of 0.2UI, No data to SMPTE, $\overline{\text{SMPTE\_BYPASS}}$ = HIGH DVB_ASI = LOW, at 25°C	–	–	235	us	1
Asynchronous Lock Time (LOCKED signal set HIGH)	t_{LOCK}	Input jitter of 0.2UI, No data to non-SMPTE, $\overline{\text{SMPTE\_BYPASS}}$ = LOW DVB_ASI = LOW, at 25°C	–	–	165	us	1

Table 2-3: AC Electrical Characteristics (Continued)

V_{DD} = 1.8V ±5%, 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise specified. Typical values: V_{CC} = 1.8V, 3.3V and T_A =25°C

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
Serial Digital Input							
Serial Input Data Rate	DR_{SDI}	–	–	270	–	Mb/s	–
DVB-ASI Payload Data Rate	DR_{ASI}	204 byte mode	–	–	213.9	Mb/s	2,4
		188 byte mode	–	–	213.7	Mb/s	3,4
Serial Input Jitter Tolerance	IJT	–	–	0.5	–	UI	5
Differential Input Voltage Range	–	BUFF_VDD = 1.8V	200	800	1700	mV_{p-p}	–
	–	BUFF_VDD = 3.3V	100	800	2200	mV_{p-p}	–
Parallel Output							
Parallel Output Clock Frequency	f_{PCLK}	–	–	27	–	MHz	–
Parallel Output Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Variation of Parallel Output Clock (from 27MHz)	–	Device Unlocked	-7.5	–	+7.5	%	6
Output Data Hold Time	t_{OH}	With 15pF load	3	–	–	ns	7
Output Delay Time	t_{OD}	With 15pF load	–	–	10	ns	7
GSPI							
GSPI Input Clock Frequency	f_{GSPI}	–	–	–	54	MHz	–
GSPI Clock Duty Cycle	DC_{GSPI}	–	40	–	60	%	–
GSPI Setup Time	t_{GS}	–	1.5	–	–	ns	–
GSPI Hold Time	t_{GH}	–	–	–	1.5	ns	–

NOTES

1. No signal to signal present, or a switch from another data rate to 270Mb/s.
2. Transmission format includes 204 byte data packets preceded by two K28.5 synchronization characters. Payload data rate excludes the two K28.5 synchronization characters.
3. Transmission format includes 188 byte data packets preceded by two K28.5 synchronization characters. Payload data rate excludes the two K28.5 synchronization characters.
4. Maximum payload is achieved via data packet mode,however, any combination of burst and packet mode is supported as long as each byte or packet is preceded by two K28.5 characters.
5. Power supply noise 50mV_{pp} at 15kHz, 100kHz, 1MHz sinusoidal modulation.
6. When the serial input to the GS9090B is removed, the PCLK output signal will continue to operate at 27MHz and the internal VCO will remain at this frequency within +/-7.5%.
7. Timing includes the following outputs: DOUT[9:0], H, V, F, ANC, EDH_DETECT, FIFO_FULL, FIFO_EMPTY, $\overline{\text{FIFO\_LD}}$, WORDERR, SYNCOUT. When the FIFO is enabled, the outputs are measured with respect to RD_CLK.

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-1. The recommended standard eutectic reflow profile is shown in Figure 2-2.

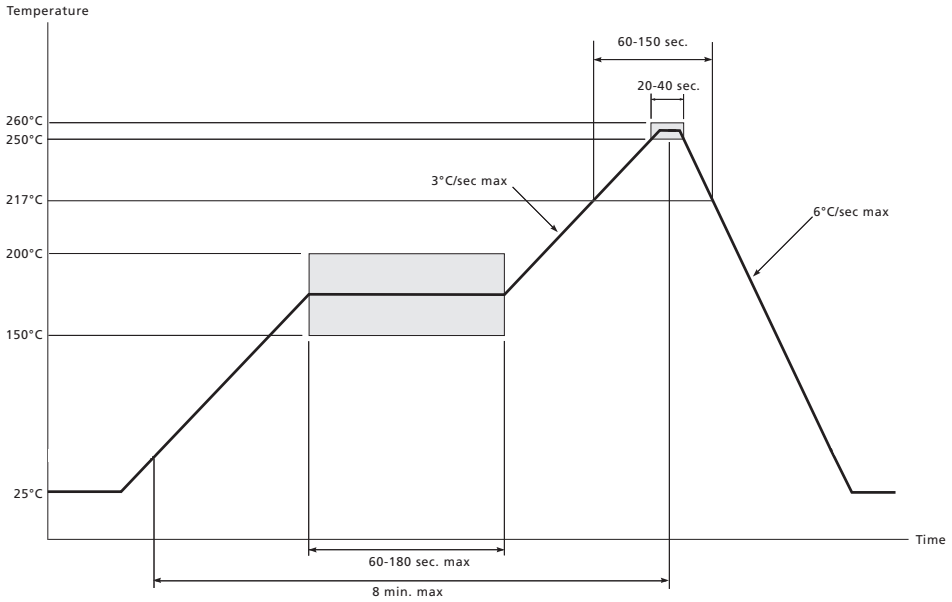


Figure 2-1: Maximum Pb-free Solder Reflow Profile (Preferred)

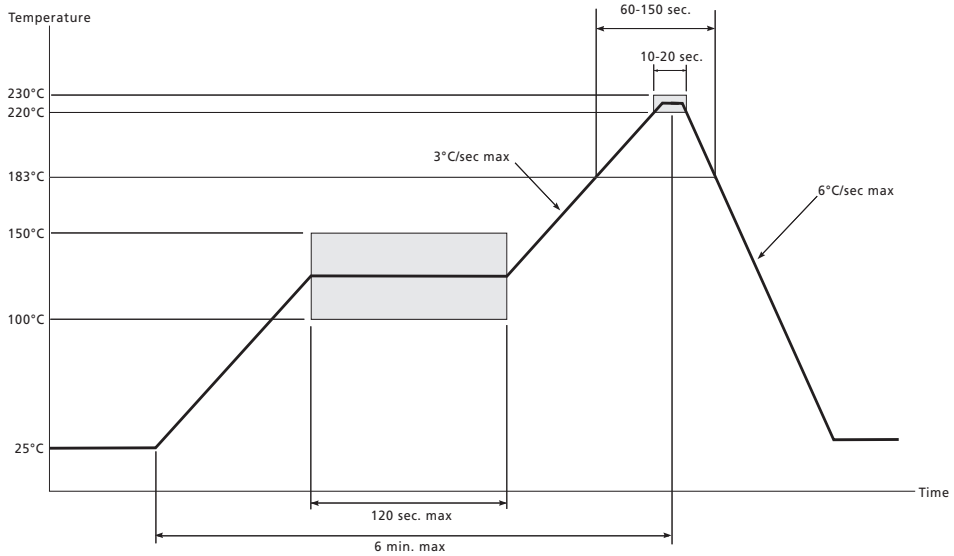


Figure 2-2: Standard Pb Solder Reflow Profile

2.5 Host Interface Map

Table 2-4: Host Interface Map

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_LD_POSITION[12:0]	28h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	27h																
	26h																
ERROR_MASK_REGISTER	25h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ ERR_ MASK	FF_CRC_ ERR_ MASK	AP_CRC_ ERR_ MASK	LOCK_ ERR_ MASK	CCS_ERR_ MASK	SAV_ERR_ MASK	EAV_ERR _MASK
FF_PIXEL_END_F1[12:0]	24h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE4[10:0]	14h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Table 2-4: Host Interface Map (Continued)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RASTER_STRUCTURE2[12:0]	12h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B(4,3)	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A(2,1)	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
ANC_TYPE(5)[15:0]	0Eh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(4)[15:0]	0Dh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(3)[15:0]	0Ch	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(2)[15:0]	0Bh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(1)[15:0]	0Ah	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_B[10:0]	09h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_EMPTY_OFFSET	06h	Not Used	Not Used	Not Used	Not Used	ANC_ DATA_ DELETE	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h	Not Used	Not Used	Not Used	ANC_ DATA_ SWITCH	STAT3_ CONFIG b2	STAT3_ CONFIG b1	STAT3_ CONFIG b0	STAT2_ CONFIG b2	STAT2_ CONFIG b1	STAT2_ CONFIG b0	STAT1_ CONFIG b2	STAT1_ CONFIG b1	STAT1_ CONFIG b0	STAT0_ CONFIG b2	STAT0_ CONFIG b1	STAT0_ CONFIG b0
DATA_FORMAT	04h	Not Used	Not Used	Not Used	Not Used	EDH_ FLAG_ UPDATE	AP_CRC _V	FF_CRC _V	EDH_ DETECT	VERSION_ 352M	Not Used	Not Used	STD_ LOCK	DATA_ FORMAT b3	DATA_ FORMAT b2	DATA_ FORMAT b1	DATA_ FORMAT b0
EDH_FLAG_OUT	03h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
EDH_FLAG_IN	02h	Not Used	ANC-UE _IN	ANC-IDA _IN	ANC-IDH _IN	ANC-EDA _IN	ANC-EDH _IN	FF-UES_ IN	FF-IDA_IN	FF-IDH _IN	FF-EDA _IN	FF-EDH _IN	AP-UES _IN	AP-IDA_I N	AP-IDH_I N	AP-EDA_I N	AP-EDH_I N
ERROR_STATUS	01h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ ERR	FF_CRC_ ERR	AP_CRC_ ERR	LOCK_ ERR	CCS_ERR	SAV_ERR	EAV_ERR
IOPROC_DISABLE	00h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	ANC_PKT _EXT	FIFO_ MODE b1	FIFO_ MODE b0	H_ CONFIG	Not Used	Not Used	ILLEGAL_ REMAP	EDH_CRC _INS	ANC_ CSUM_ INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

2.5.1 Host Interface Map (R/W registers)

Table 2-5: Host Interface Map (R/W registers)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_LD_POSITION[12:0]	28h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	27h																
	26h																
ERROR_MASK_REGISTER	25h										VD_STD_ ERR_ MASK	FF_CRC_ ERR_ MASK	AP_CRC_ ERR_ MASK	LOCK_ ERR_ MASK	CCS_ERR_ MASK	SAV_ERR_ MASK	EAV_ERR _MASK
FF_PIXEL_END_F1[12:0]	24h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	14h																
	13h																
	12h																

Table 2-5: Host Interface Map (R/W registers) (Continued)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	11h																
	10h																
	0Fh																
ANC_TYPE(5)[15:0]	0Eh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(4)[15:0]	0Dh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(3)[15:0]	0Ch	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(2)[15:0]	0Bh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(1)[15:0]	0Ah	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_B[10:0]	09h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_EMPTY_OFFSET	06h					ANC_ DATA_ DELETE		b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h				ANC_ DATA_ SWITCH	STAT3_ CONFIG b2	STAT3_ CONFIG b1	STAT3_ CONFIG b0	STAT2_ CONFIG b2	STAT2_ CONFIG b1	STAT2_ CONFIG b0	STAT1_ CONFIG b2	STAT1_ CONFIG b1	STAT1_ CONFIG b0	STAT0_ CONFIG b2	STAT0_ CONFIG b1	STAT0_ CONFIG b0
DATA_FORMAT	04h					EDH_ FLAG_ UPDATE											
	03h																
	02h																
	01h																
IOPROC_DISABLE	00h							ANC_PKT _EXT	FIFO_ MODE b1	FIFO_ MODE b0	H_ CONFIG			ILLEGAL_ REMAP	EDH_CRC _INS	ANC_ CSUM_ INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

2.5.2 Host Interface Map (Read only registers)

Table 2-6: Host Interface Map (Read only registers)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	28h																
	27h																
	26h																
	25h																
	24h																
	23h																
	22h																
	21h																
	20h																
	1Fh																
	1Eh																
	1Dh																
	1Ch																
	1Bh																
	1Ah																
	19h																
	18h																
	17h																
	16h																
	15h																
RASTER_STRUCTURE4[10:0]	14h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Table 2-6: Host Interface Map (Read only registers) (Continued)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO_FORMAT_OUT_B(4,3)	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A(2,1)	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
	09h																
	08h																
	07h																
	06h																
	05h																
DATA_FORMAT	04h						AP_CRC_V	FF_CRC_V	EDH_DETECT	VERSION_352M			STD_LOCK	DATA_FORMAT b3	DATA_FORMAT b2	DATA_FORMAT b1	DATA_FORMAT b0
EDH_FLAG_OUT	03h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
EDH_FLAG_IN	02h	Not Used	ANC-UES_IN	ANC-IDA_IN	ANC-IDH_IN	ANC-EDA_IN	ANC-EDH_IN	FF-UES_IN	FF-IDA_IN	FF-IDH_IN	FF-EDA_IN	FF-EDH_IN	AP-UES_IN	AP-IDA_IN	AP-IDH_IN	AP-EDA_IN	AP-EDH_IN
ERROR_STATUS	01h										VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR	CCS_ERR	SAV_ERR	EAV_ERR
	00h																

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

3. Detailed Description

3.1 Functional Overview

The GS9090B is a 270Mb/s reclocking deserializer with an internal FIFO and programmable multi-function output port. The device has two basic modes of operation. In Auto mode, the GS9090B can automatically detect SMPTE data streams at its input. In Manual mode, the device can be set to process SMPTE or DVB/ASI data streams.

The digital signal processing core handles ancillary data detection/indication, error detection and handling (EDH), SMPTE352M extraction, and automatic video standards detection. These features are all enabled by default, but may be individually disabled via internal registers accessible through the GSPI host interface.

The provided programmable multi-function output pins may be configured to output various status signals including H, V, and F timing, ancillary data detection, EDH detection, and a FIFO load pulse. The internal FIFO supports 4 modes of operation, which may be used for data alignment, data delay, MPEG packet extraction, or ancillary data extraction.

The GS9090B contains a JTAG interface for boundary scan test implementations.

3.2 Serial Digital Input

The GS9090B contains a current mode differential serial digital input buffer. The input buffer has internal 50Ω termination resistors, which are connected to ground via the TERM pin.

If the input signal is AC coupled to the device, the signal source common mode level will be set internally to typically 1.45V. If the input signal is DC coupled to the device, the internal biasing will be ignored. Please see AC Electrical Characteristics for Common Mode range and swing characteristics.

3.3 Clock and Data Recovery

The GS9090B contains an integrated clock and data recovery block. The function of this block is to lock to the input data stream, extract a clean clock, and retime the serial digital data to remove high frequency jitter.

3.3.1 Internal VCO and Phase Detector

The GS9090B uses an internal VCO and PFD as part of the reclocker's phase-locked loop. Each block requires a +1.8V DC power supply, which is supplied via the VCO_VDD / VCO_GND and PLL_VDD / PLL_GND pins.

3.4 Serial-To-Parallel Conversion

The retimed data and phase-locked clock signals from the reclocker are fed to the serial-to-parallel converter. The function of this block is to extract 10-bit parallel data words from the reclocked serial data stream and simultaneously present them to the SMPTE and DVB-ASI word alignment blocks.

3.5 Modes Of Operation

The GS9090B has two basic modes of operation: Auto mode and Manual mode. Auto mode is enabled when AUTO/$\overline{\text{MAN}}$ is set HIGH, and Manual mode is enabled when AUTO/$\overline{\text{MAN}}$ is set LOW. As indicated in Figure 3-1. DVB_ASI and data-through are only supported in Manual mode.

In Auto mode (AUTO/$\overline{\text{MAN}}$ = HIGH), the GS9090B will automatically detect, reclock, deserialize, and process SMPTE 259M-C input data.

In Manual mode (AUTO/$\overline{\text{MAN}}$ = LOW), the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins must be set as per Table 3-2 for the correct reception of either SMPTE or DVB-ASI data. Manual mode also supports the reclocking and deserializing of 270Mb/s data not conforming to SMPTE or DVB-ASI streams.

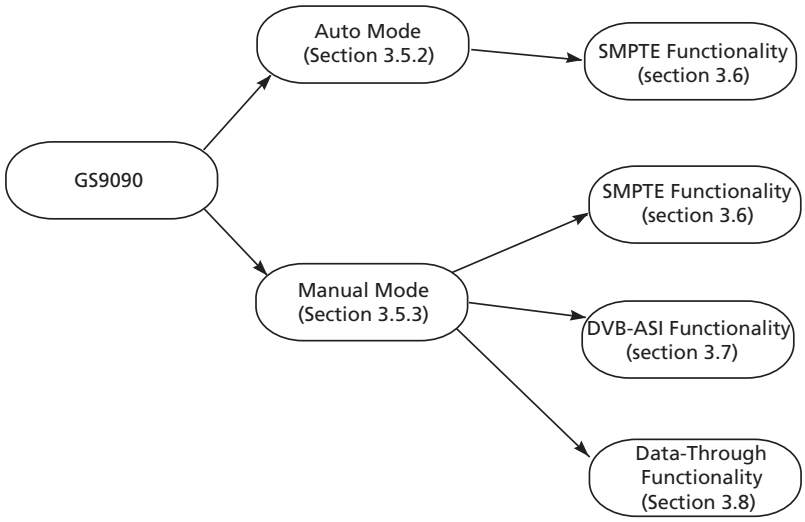


Figure 3-1: GS9090B's Modes of Operation

3.5.1 Lock Detect

Once the reclocker has locked to the received serial digital data stream, the lock detect block of the GS9090B searches for the appropriate sync words, and indicates via the LOCKED output pin when the device has successfully achieved lock. The LOCKED pin is designed to be stable. It will not toggle during the locking process, nor will it glitch during a SMPTE synchronous switch.

The lock detection process is summarized in Figure 3-2.

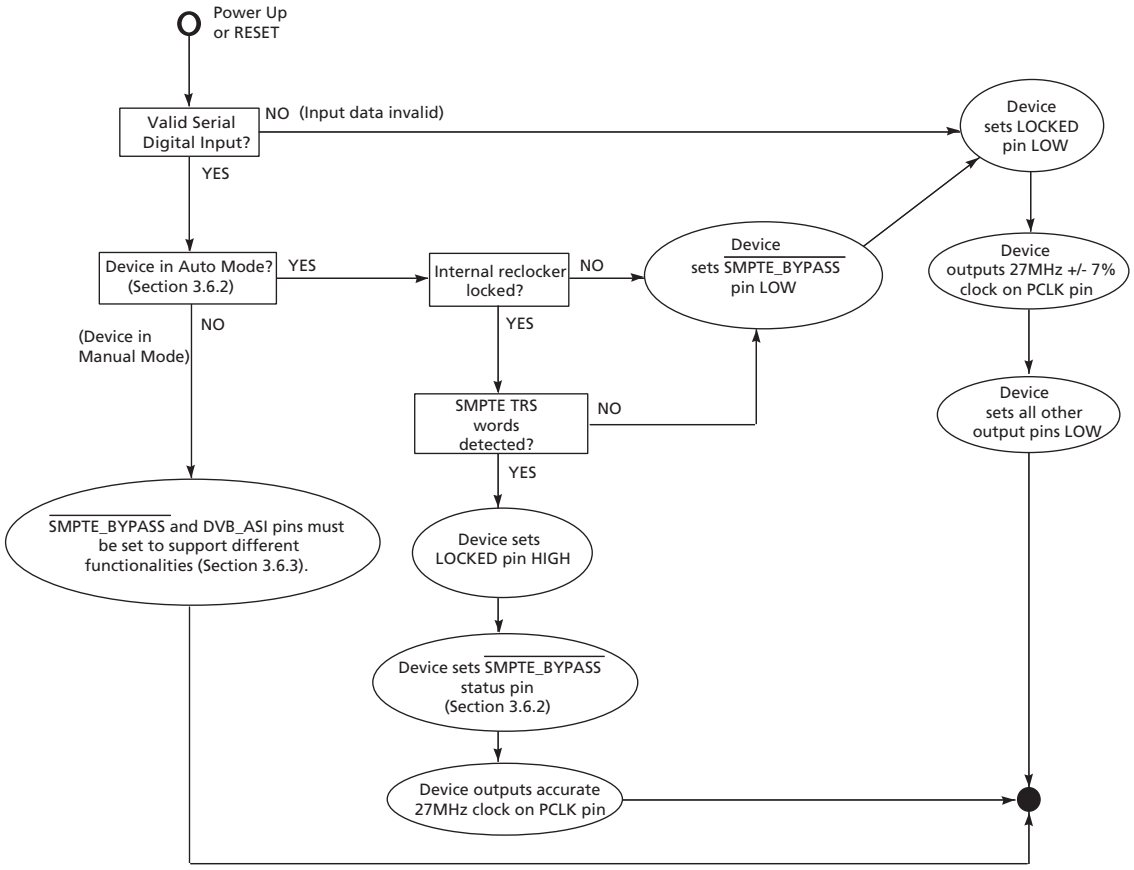


Figure 3-2: Lock Detection Process

The lock detection algorithm (Figure 3-2) first determines if the input is a 270Mb/s serial digital data stream.

When the serial data input signal is considered invalid, the LOCKED pin will be set LOW, and all device outputs will be forced LOW, except PCLK.

If a valid serial digital input signal has been detected, and the device is in Auto mode, the lock algorithm will attempt to detect the presence of SMPTE TRS words. Assuming that a valid 270Mb/s SMPTE signal has been applied to the device, the LOCKED pin will be set HIGH.

The PCLK output frequency will be 27MHz +/- 7.5% when the device is not locked, as well as during the lock detection process.

For serial inputs that do not conform to SMPTE or DVB-ASI formats, the device can only achieve the locked state in manual mode. In Auto mode, the LOCKED signal will be asserted LOW, the parallel outputs will be latched to logic LOW, and the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI output signals will also be set LOW.