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SEMTECH
GENNUM PRODUCTS

GS9091B

GenLINX® II 270Mb/s Deserializer for SDI and DVB-ASI

Key Features

- SMPTE 259M-C compliant descrambling and NRZI to NRZ decoding (with bypass)
- DVB-ASI 8b/10b decoding
- Integrated Cable Equalizer
- 500m typical equalization of Belden 1694A cable
- Integrated line-based FIFO for data alignment/delay, clock phase interchange, DVB-ASI data packet extraction and clock rate interchange, and ancillary data packet extraction
- Integrated VCO and reclocker
- User selectable additional processing features including:
  - TRS, ANC data checksum, and EDH CRC error detection and correction
  - programmable ANC data detection
  - illegal code remapping
- Internal flywheel for noise immune H, V, F extraction
- Automatic standards detection and indication
- Enhanced Gennum Serial Peripheral Interface (GSPI)
- JTAG test interface
- Polarity insensitive for DVB-ASI and SMPTE signals
- +1.8V core power supply with optional +1.8V or +3.3V I/O power supply
- Small footprint (11mm x 11mm)
- Low power operation (typically 350mW)
- Pb-free and RoHS compliant

Applications

- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS9091B is a 270Mb/s equalizing and reclocking deserializer with an internal FIFO. It provides a complete receive solution for SD-SDI and DVB-ASI applications.

In addition to equalizing, reclocking and deserializing the input data stream, the GS9091B performs NRZI -to-NRZ decoding, descrambling as per SMPTE 259M-C, and word alignment when operating in SMPTE mode. When operating in DVB-ASI mode, the device will word align the data to K28.5 sync characters and 8b/10b decode the received stream.

The integrated equalizer is optimized for 270Mb/s and can typically equalize up to 500m of Belden 1694A cable. Both the equalizer and the internal reclocker are fully compatible with both SMPTE and DVB-ASI input streams.

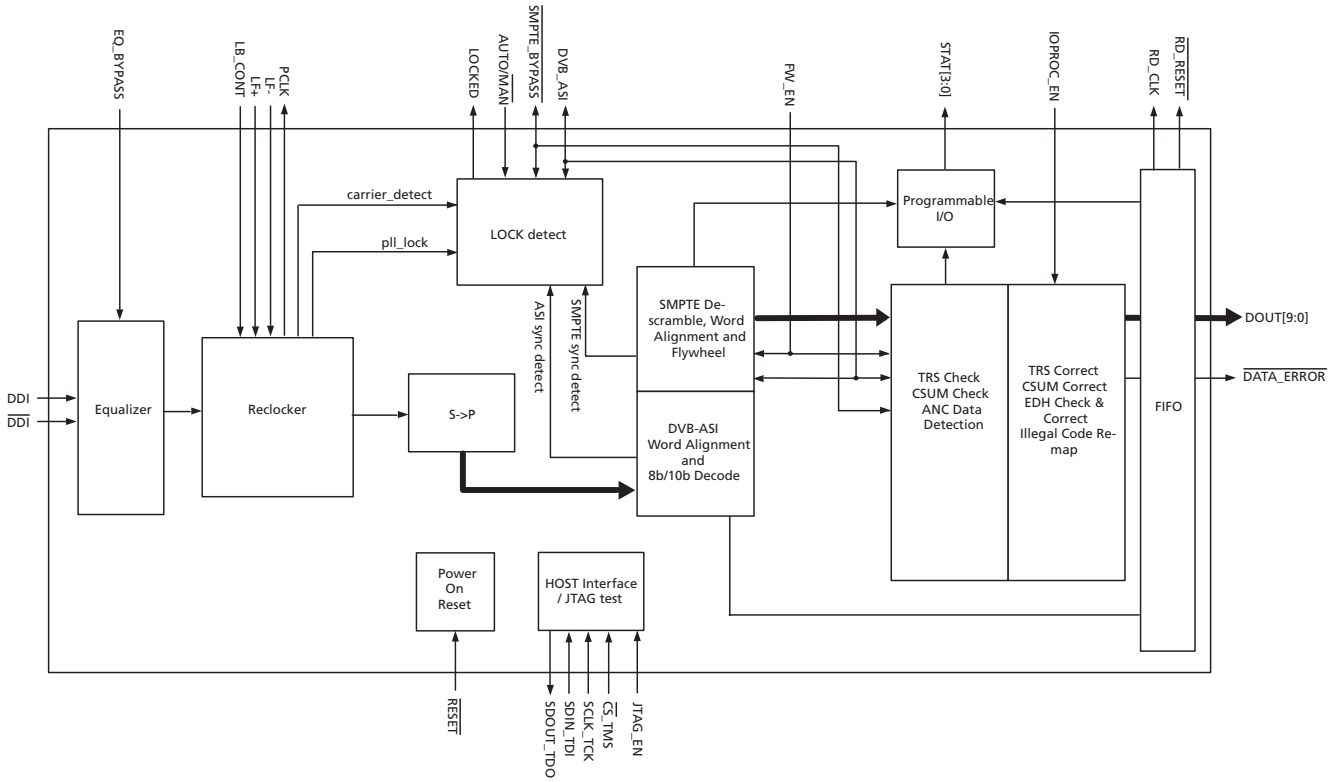
The GS9091B includes a range of data processing functions such as EDH support (error detection and handling), and automatic standards detection. The device can also detect and extract SMPTE 352M payload identifier packets and independently identify the received video standard. This information is read from internal registers via the host interface port.

The GS9091B also incorporates a video line-based FIFO. This FIFO may be used in four user-selectable modes to carry out tasks such as data alignment / delay, clock phase interchange, MPEG packet extraction and clock rate interchange, and ancillary data packet extraction.

Parallel data outputs are provided in 10-bit multiplexed format, with the associated parallel clock output signal operating at 27MHz.

The device may also be used in a low-latency data pass through mode where only descrambling and word alignment will be performed in SMPTE mode.

Functional Block Diagram



GS9091B Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
3	011367	–	February 2013	Updated to the Semtech template.
2	150199	50711	July 2008	DVB_ASI operation specification change in Auto mode.
1	144807	–	April 2007	Converting to Data Sheet. Modified Electrical Characteristics.
0	139930	–	November 2006	New Document.

Contents

1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	LF+	NC	LB_ CONT	VCO_ VDD	VBG	FIFO_EN	AUTO/ $\overline{\text{MAN}}$	LOCKED	PCLK	DOUT9
B	LF-	PLL_ VDD	PLL_ GND	VCO_ GND	NC	FW_EN	CORE _VDD	$\overline{\text{SMPTE\_}}$ $\overline{\text{BYPASS}}$	DVB_ASI	DOUT8
C	ANA_ VDD	ANA_ VDD	NC	NC	NC	NC	NC	IO_VDD	NC	DOUT7
D	ANA_ GND	ANA_ GND	NC	CORE _GND	CORE _GND	IO_GND	IO_GND	NC	NC	DOUT6
E	EQ_GND	TERM	NC	CORE _GND	CORE _GND	IO_GND	IO_GND	NC	IO_VDD	DOUT5
F	SDI	HEAT_ SINK_ GND	HEAT_ SINK_ GND	CORE _GND	CORE _GND	IO_GND	IO_GND	NC	IO_VDD	DOUT4
G	$\overline{\text{SDI}}$	HEAT_ SINK_ GND	HEAT_ SINK_ GND	CORE _GND	CORE _GND	IO_GND	IO_GND	NC	NC	DOUT3
H	EQ_VDD	HEAT_ SINK_ GND	HEAT_ SINK_ GND	NC	NC	NC	NC	IO_VDD	$\overline{\text{RD\_}}$ $\overline{\text{RESET}}$	DOUT2
J	AGC+	EQ_ BYPASS	JTAG_EN	$\overline{\text{CS\_}}$ TMS	SDOUT _TDO	CORE _VDD	$\overline{\text{DATA\_}}$ $\overline{\text{ERROR}}$	STAT2	STAT3	DOUT1
K	AGC-	NC	IOPROC _EN	$\overline{\text{RESET}}$	SCLK _TCK	SDIN _TDI	STAT0	STAT1	RD_CLK	DOUT0

Figure 1-1: Pin Assignment

Table 1-1: Ball List and Description

Ball	Name	Timing	Type	Description
A1	LF+	Analog	Input	Loop filter component connection. Connect to LF- through a 4.4nF capacitor.
A2, B5, C3, C4, C5, C6, C7, C9, D3, D8, D9, E3, E8, F8, G8, G9, H4, H5, H6, H7, K2	NC	–	–	No connect. Not connected internally.
A3	LB_CONT	Analog	Input	CONTROL SIGNAL INPUT Control voltage to fine-tune the loop bandwidth of the PLL.
A4	VCO_VDD	Analog	Input Power	Power supply connection for Voltage-Controlled-Oscillator. Connect to +1.8V DC.
A5	VBG	Analog	Input	Bandgap filter capacitor. Connect to GND as shown in Typical Application Circuit.
A6	FIFO_EN	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable / disable the internal FIFO. When FIFO_EN is HIGH, the internal FIFO will be enabled. Data will be clocked out of the device on the rising edge of the RD_CLK input pin if the FIFO is in video mode or DVB-ASI mode. When FIFO_EN is LOW, the internal FIFO is bypassed and parallel data is clocked out on the rising edge of the PCLK output.
A7	AUTO/$\overline{\text{MAN}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. When set HIGH, the GS9091B will operate in Auto mode. The $\overline{\text{SMPTE\_BYPASS}}$ pin becomes an output status signal set by the device. In this mode, the GS9091B will automatically detect, reclock, deserialize, and process SMPTE compliant input data. When set LOW, the GS9091B will operate in Manual mode. The DVB_ASI and $\overline{\text{SMPTE\_BYPASS}}$ pins become input control signals. In this mode, the application layer must set these two external pins for the correct reception of either SMPTE or DVB-ASI data. Manual mode also supports the reclocking and deserializing of data not conforming to SMPTE or DVB-ASI streams.
A8	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. The LOCKED pin will be HIGH whenever the device has correctly received and locked to SMPTE compliant data in SMPTE mode or DVB-ASI compliant data in DVB-ASI mode, or when the reclocker has achieved lock in Data-Through mode. It will be LOW otherwise. When the pin is LOW, all digital output signals will be forced to logic LOW levels.
A9	PCLK	–	Output	PIXEL CLOCK OUTPUT Signal levels are LVCMOS / LVTTL compatible. 27MHz parallel clock output.

Table 1-1: Ball List and Description (Continued)

Ball	Name	Timing	Type	Description
A10, B10, C10, D10, E10, F10, G10, H10, J10, K10	DOUT[9:0]	Synchronous with RD_CLK or PCLK	Output	PARALLEL VIDEO DATA BUS Signal levels are LVCMOS / LVTTL compatible. When the internal FIFO is enabled and configured for either video mode or DVB-ASI mode, parallel data will be clocked out of the device on the rising edge of RD_CLK. When the internal FIFO is in bypass mode, parallel data will be clocked out of the device on the rising edge of PCLK. DOUT9 is the MSB and DOUT0 is the LSB.
B1	LF-	Analog	Input	Loop filter component connection. Connect to LF+ through a 4.4nF capacitor.
B2	PLL_VDD	Analog	Input Power	Power supply connection for phase-locked loop. Connect to +1.8V DC.
B3	PLL_GND	Analog	Input Power	Ground connection for phase-locked loop. Connect to GND.
B4	VCO_GND	Analog	Input Power	Ground connection for Voltage-Controlled-Oscillator. Connect to GND.
B6	FW_EN	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable or disable the noise immune flywheel of the device. When set HIGH, the internal flywheel is enabled. This flywheel is used in the extraction of timing signals, the generation of TRS signals, the automatic detection of video standards, and in manual switch line lock handling. When set LOW, the internal flywheel is disabled. Timing based TRS errors will not be detected.
B7, J6	CORE_VDD	Non Synchronous	Input Power	Power supply for digital logic blocks. Connect to +1.8V DC.
B8	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. This pin is an input set by the application layer in Manual mode, and an output set by the device in Auto mode. Auto Mode (AUTO/$\overline{\text{MAN}}$ = HIGH): The $\overline{\text{SMPTE\_BYPASS}}$ pin will be HIGH only when the device has locked to a SMPTE compliant data stream. It will be LOW otherwise. When the pin is LOW, no I/O processing features are available. Manual Mode (AUTO/$\overline{\text{MAN}}$ = LOW): When the application layer sets this pin HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode. When $\overline{\text{SMPTE\_BYPASS}}$ is set LOW, the device will not support the descrambling, decoding, or word alignment of received SMPTE data. No I/O processing features will be available.

Table 1-1: Ball List and Description (Continued)

Ball	Name	Timing	Type	Description
B9	DVB_ASI	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. This pin and its function are only supported in Manual mode (AUTO/$\overline{\text{MAN}}$ = LOW). When the application layer sets this pin HIGH, the device will be configured to operate in DVB-ASI mode. The $\overline{\text{SMPTE\_BYPASS}}$ pin will be ignored. When set LOW, the device will not support the decoding or word alignment of received DVB-ASI data.
C1, C2	ANA_VDD	Analog	Input Power	Power supply connection for analog core. Connect to +3.3V DC.
C8, E9, F9, H8	IO_VDD	Non Synchronous	Input Power	Power supply for digital I/O. For a 3.3V tolerant I/O, connect pins to either +1.8V DC or +3.3V DC. For a 5V tolerant I/O, connect pins to a +3.3V DC.
D1, D2	ANA_GND	Analog	Input Power	Ground connection for analog core. Connect to GND.
D4, D5, E4, E5, F4, F5, G4, G5	CORE_GND	Non Synchronous	Input Power	Ground connection for digital logic blocks. Connect to GND.
D6, D7, E6, E7, F6, F7, G6, G7	IO_GND	Non Synchronous	Input Power	Ground connection for digital I/O. Connect to GND.
E1	EQ_GND	Analog	Input Power	Ground connection for equalizer core. Connect to GND.
E2	TERM	Analog	Input	Termination for serial digital input. AC couple to ANA_GND
F1, G1	SDI, $\overline{\text{SDI}}$	Analog	Input	Serial digital differential input pair.
F2, F3, G2, G3, H2, H3	HEAT_SINK_GND	Analog	Input Power	Heat sink connection. Connect to main ground plane of application board.
H1	EQ_VDD	Analog	Input Power	Power supply connection for equalizer core. Connect to +3.3V DC.
H9	$\overline{\text{RD\_RESET}}$	Synchronous with RD_CLK	Input	FIFO READ RESET Signal levels are LVCMOS / LVTTL compatible. Valid input only when the device is in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB-ASI = LOW), and the internal FIFO is configured for video mode (Section 3.10.1). A HIGH to LOW transition will reset the FIFO pointer to address zero of the memory.
J1, K1	AGC+, AGC-	Analog	Input	External AGC capacitor connection. Connect J1 and K1 together through a 1uF capacitor.
J2	EQ_BYPASS	Analog	Input	CONTOL SIGNAL INPUT Signal levels are 3.3V CMOS / LVTTL compatible. Equalizer bypass. When EQ_BYPASS is HIGH, the equalizer stages are bypassed. When EQ_BYPASS is LOW, normal operation of the equalizer stages resumes.

Table 1-1: Ball List and Description (Continued)

Ball	Name	Timing	Type	Description
J3	JTAG_EN	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{CS}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured for JTAG boundary scan testing. When set LOW, $\overline{CS}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured as GSPI pins for normal host interface operation.
J4	$\overline{CS}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Chip Select / Test Mode Select Host Mode (JTAG_EN = LOW): $\overline{CS}$_TMS operates as the host interface chip select, $\overline{CS}$, and is active LOW. JTAG Test Mode (JTAG_EN = HIGH): $\overline{CS}$_TMS operates as the JTAG test mode select, TMS, and is active HIGH.
J5	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG_EN = LOW): SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG_EN = HIGH): SDOUT_TDO operates as the JTAG test data output, TDO.
J7	$\overline{DATA\_ERROR}$	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. The $\overline{DATA\_ERROR}$ pin will be LOW when an error within the received data stream has been detected by the device. This pin is an inverted logical OR-ing of all detectable errors listed in the internal ERROR_STATUS register. Once an error is detected, $\overline{DATA\_ERROR}$ will remain LOW until the start of the next video frame / field, or until the ERROR_STATUS register is read via the host interface. The $\overline{DATA\_ERROR}$ pin will be HIGH when the received data stream has been detected without error. NOTE: It is possible to program which error conditions are monitored by the device by setting appropriate bits in the ERROR_MASK register HIGH. All error conditions are detected by default.

Table 1-1: Ball List and Description (Continued)

Ball	Name	Timing	Type	Description
K3	IOPROC_EN	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal Levels are LVCMOS / LVTTL compatible. Used to enable or disable the I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • Illegal Code Remapping • EDH CRC Error Correction • Ancillary Data Checksum Error Correction • TRS Error Correction • EDH Flag Detection To enable a subset of these features, keep IOPROC_EN HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When set LOW, the device will enter low-latency mode. NOTE: When the internal FIFO is configured for Video mode or Ancillary Data Extraction mode, IOPROC_EN must be set HIGH (see Section 3.10).
K4	$\overline{\text{RESET}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to reset the internal operating conditions to default setting or to reset the JTAG test sequence. Host Mode (JTAG_EN = LOW): When asserted LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance. When set HIGH, normal operation of the device resumes 10usec after the LOW-to-HIGH transition of the $\overline{\text{RESET}}$ signal. JTAG Test Mode (JTAG_EN = HIGH): When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes.
K5	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Clock / Test Clock. All JTAG / Host Interface address and data are shifted into/out of the device synchronously with this clock. Host Mode (JTAG_EN = LOW): SCLK_TCK operates as the host interface serial data clock, SCLK. JTAG Test Mode (JTAG_EN = HIGH): SCLK_TCK operates as the JTAG test clock, TCK.
K6	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Input / Test Data Input Host Mode (JTAG_EN = LOW): SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG_EN = HIGH): SDIN_TDI operates as the JTAG test data input, TDI.

Table 1-1: Ball List and Description (Continued)

Ball	Name	Timing	Type	Description
K7, K8, J8, J9	STAT[0:3]	Synchronous with PCLK or RD_CLK	Output	MULTI FUNCTION I/O PORT Signal levels are LVCMOS / LVTTL compatible. Programmable multi-function outputs. By programming the bits is the IO_CONFIG register, each pin can output one of the following signals: • H • V • F • $\overline{\text{FIFO\_LD}}$ • ANC • EDH_DETECT • FIFO_FULL • FIFO_EMPTY These pins are set to certain default values depending on the configuration of the device and the internal FIFO mode selected. See Section 3.12 for details.
K9	RD_CLK	–	Input	FIFO READ CLOCK Signal levels are LVCMOS / LVTTL compatible. The application layer clocks the parallel data out of the FIFO on the rising edge of RD_CLK.

2. Electrical Characteristics

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +3.47V
Input Voltage Range (LF+, LF-, LB_CONT, VBG)	-0.5V to +2.3V
Input Voltage Range (SDI, $\overline{SDI}$, AGC+, AGC-, EQ_BYPASS)	-0.5V to +3.6V
Input Voltage Range (All Other)	-0.5V to +5.25V
Ambient Operating Temperature	$-20°C \leq T_A \leq 85°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
ESD protection on all pins (see Note 1)	1kV

Notes:

1. MIL STD 883 ESD protection will be applied to all pins on the device.
2. Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.

2.1 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V_{DD} = 1.8V ±5%, 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise specified. Typical values: V_{CC} = 1.8V, 3.3V and T_A =25°C

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Operating Temperature Range	T_A	–	0	25	70	°C	1
Core Power Supply Voltage	CORE_VDD	–	1.71	1.8	1.89	V	–
Analog Core Power Supply Voltage	ANA_VDD	–	3.13	3.3	3.47	V	–
Digital I/O Buffer Power Supply Voltage	IO_VDD	1.8V Operation	1.71	1.8	1.89	V	–
	IO_VDD	3.3V Operation	3.13	3.3	3.47	V	–
PLL Power Supply Voltage	PLL_VDD	–	1.71	1.8	1.89	V	–
VCO Power Supply Voltage	VCO_VDD	–	1.71	1.8	1.89	V	–
Equalizer Power Supply Voltage	EQ_VDD	–	3.13	3.3	3.47	V	–
Core Supply Current	I_{DD}	Total 1.8V Supply	–	64	80	mA	2
		Total 3.3V Supply	–	69	92	mA	3

Table 2-2: DC Electrical Characteristics (Continued)

V_{DD} = 1.8V ±5%, 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise specified. Typical values: V_{CC} = 1.8V, 3.3V and T_A =25°C

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
I/O Supply Current	I_{IO}	I/O Supply, 1.8V Operation	–	4.5	8	mA	4
		I/O Supply, 3.3V Operation	–	8.5	14	mA	4
Power Dissipation	P_D	CORE_VDD = 1.8V IO_VDD = 1.8V	–	350	–	mW	–
		CORE_VDD = 1.89V IO_VDD = 3.47V	–	–	490	mW	–
Digital I/O							
Input Voltage, Logic LOW	V_{IL}	1.8V Operation or 3.3V Operation	–	–	0.35 x IO_VDD	V	–
Input Voltage, Logic HIGH	V_{IH}	1.8V Operation or 3.3V Operation	0.65 x IO_VDD	–	–	V	–
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 8mA @ 3.3V, 4mA @ 1.8V	–	–	0.4	V	–
Output Voltage, Logic HIGH	V_{OH}	I_{OL} = -8mA @ 3.3V, -4mA @ 1.8V	IO_VDD - 0.4	–	–	V	–
EQ_BYPASS Input Voltage	V_{IL}	Logic LOW	–	–	0.8	V	–
	V_{IH}	Logic HIGH	2.4	–	–	V	–
Serial Digital Inputs							
Input Common Mode Voltage	V_{CMIN}	T_A = 25°C	–	1.75	–	V	–
Input Resistance	–	single ended	–	1.64	–	kΩ	–

Notes:

1. All DC and AC electrical parameters within specification.
2. Maximum supply current at T_A = 0°C and V_{DD} = 1.89V supply.
3. Maximum supply current at T_A = 75°C and V_{DD} = 3.47V supply.
4. I/O currents are based on output drivers driving one CMOS load.

2.2 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

V_{DD} = 1.8V ±5%, 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise specified. Typical values: V_{CC} = 1.8V, 3.3V and T_A =25°C

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Input Voltage Swing	ΔV_{SDI}	T_A =25°C, differential	720	800	950	mV_{p-p}	1
Lock Time (Asynchronous Switch)	t_{LOCK}	T_A =25°C, 500m of Belden 1694A	–	560	–	us	2
Serial Digital Input							
Serial Input Data Rate	DR_{SDI}	–	–	270	–	Mb/s	–
DVB-ASI Payload Data Rate	DR_{ASI}	204 byte mode	–	–	213.9	Mb/s	3,5
		188 byte mode	–	–	213.7	Mb/s	4,5
Achievable Cable Length	–	Belden 1694A Cable 270MHz	–	500	–	m	–
Input Return Loss	–	–	15	–	–	dB	6
Input Capacitance	–	single ended	–	1	–	pF	–
Parallel Output							
Parallel Output Clock Frequency	f_{PCLK}	–	–	27	–	MHz	–
Parallel Output Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Variation of Parallel Output Clock (from 27MHz)	–	Device Unlocked T_A = 5°C to 45°C	-7	–	+7	%	7
Output Data Hold Time	t_{OH}	With 15pF load	3.0	–	–	ns	8
Output Delay Time	t_{OD}	With 15pF load	–	–	10.0	ns	8
GSPI							
GSPI Input Clock Frequency	f_{GSPI}	–	–	–	54.0	MHz	–
GSPI Clock Duty Cycle	DC_{GSPI}	–	40	–	60	%	–
GSPI Setup Time	t_{GS}	–	1.5	–	–	ns	–

Table 2-3: AC Electrical Characteristics (Continued)

V_{DD} = 1.8V ±5%, 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise specified. Typical values: V_{CC} = 1.8V, 3.3V and T_A =25°C

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
GSPI Hold Time	t_{GH}	–	1.5	–	–	ns	–

Notes:

1. 0m cable length.
2. Time from input no-data to data switch and LOCKED pin set HIGH.
3. Transmission format includes 204 byte data packets preceded by two K28.5 synchronization characters. Payload data rate excludes the two K28.5 synchronization characters.
4. Transmission format includes 188 byte data packets preceded by two K28.5 synchronization characters. Payload data rate excludes the two K28.5 synchronization characters.
5. Maximum payload is achieved via data packet mode, however, any combination of burst and packet mode is supported as long as each byte or packet is preceded by two K28.5 characters.
6. 5MHz to 270MHz.
7. When the serial input to the GS9091B is removed, the PCLK output signal will continue to operate at 27MHz and the internal VCO will remain at this frequency within +/-7% over the range 5°C to 45°C. Over the full operating temperature range (0°C to 70°C), the VCO may deviate from 27MHz up to +/-13%.
8. Timing includes the following outputs: DOUT[9:0], H, V, F, ANC, EDH_DETECT, FIFO_FULL, FIFO_EMPTY, $\overline{\text{FIFO\_LD}}$, WORDERR, SYNCOUT. When the FIFO is enabled, the outputs are measured with respect to RD_CLK.

2.3 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-1. The recommended standard eutectic reflow profile is shown in Figure 2-2.

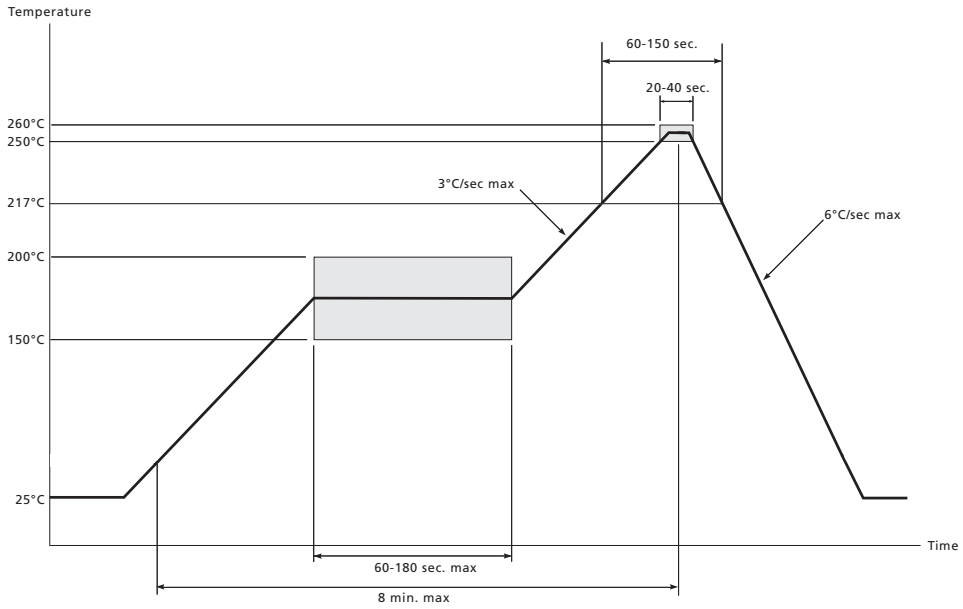


Figure 2-1: Maximum Pb-free Solder Reflow Profile (Preferred)

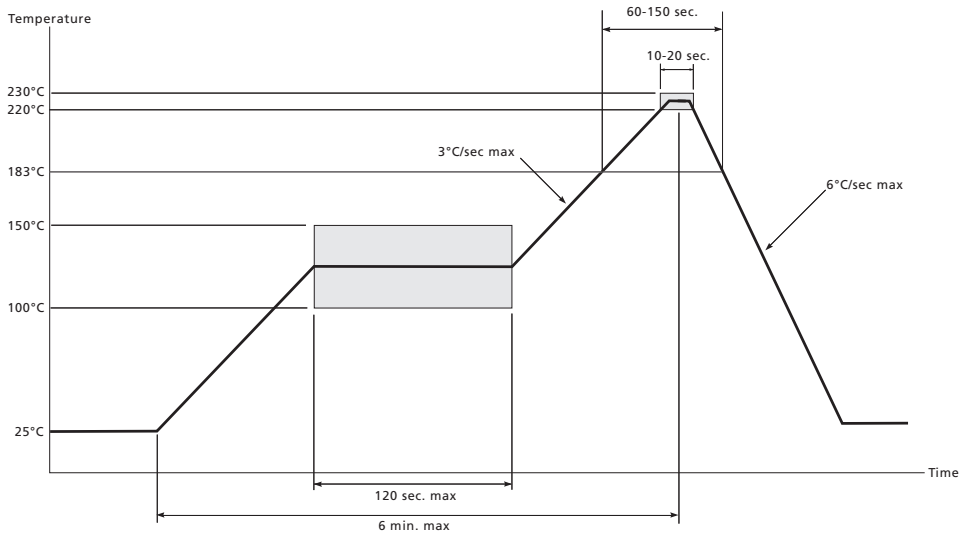


Figure 2-2: Standard Eutectic Solder Reflow Profile

2.4 Host Interface Map

Table 2-4: Host Interface Map

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_LD_POSITION[12:0]	28h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	27h																
	26h																
ERROR_MASK_REGISTER	25h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ERR_MASK	FF_CRC_ERR_MASK	AP_CRC_ERR_MASK	LOCK_ERR_MASK	CCS_ERR_MASK	SAV_ERR_MASK	EAV_ERR_MASK
FF_PIXEL_END_F1[12:0]	24h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Table 2-4: Host Interface Map (Continued)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FF_LINE_END_F0[10:0]	1Ah	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE4[10:0]	14h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B(4,3)	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A(2,1)	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
ANC_TYPE(5)[15:0]	0Eh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(4)[15:0]	0Dh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(3)[15:0]	0Ch	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(2)[15:0]	0Bh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(1)[15:0]	0Ah	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_B[10:0]	09h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Table 2-4: Host Interface Map (Continued)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANC_LINE_A[10:0]	08h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_EMPTY_OFFSET	06h	Not Used	Not Used	Not Used	Not Used	ANC_DATA_DELETE	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h	Not Used	Not Used	Not Used	ANC_DATA_SWITCH	STAT3_CONFIG b2	STAT3_CONFIG b1	STAT3_CONFIG b0	STAT2_CONFIG b2	STAT2_CONFIG b1	STAT2_CONFIG b0	STAT1_CONFIG b2	STAT1_CONFIG b1	STAT1_CONFIG b0	STAT0_CONFIG b2	STAT0_CONFIG b1	STAT0_CONFIG b0
DATA_FORMAT	04h	Not Used	Not Used	Not Used	Not Used	EDH_FLAG_UPDATE	AP_CRC_V	FF_CRC_V	EDH_DETECT	VERSION_352M	Not Used	Not Used	STD_LOCK	DATA_FORMAT b3	DATA_FORMAT b2	DATA_FORMAT b1	DATA_FORMAT b0
EDH_FLAG_OUT	03h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
EDH_FLAG_IN	02h	Not Used	ANC-UES_IN	ANC-IDA_IN	ANC-IDH_IN	ANC-EDA_IN	ANC-EDH_IN	FF-UES_IN	FF-IDA_IN	FF-IDH_IN	FF-EDA_IN	FF-EDH_IN	AP-UES_IN	AP-IDA_IN	AP-IDH_IN	AP-EDA_IN	AP-EDH_IN
ERROR_STATUS	01h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR	CCS_ERR	SAV_ERR	EAV_ERR
IOPROC_DISABLE	00h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	ANC_PKT_EXT	FIFO_MODE b1	FIFO_MODE b0	H_CONFIG	Not Used	Not Used	ILLEGAL_REMAP	EDH_CRC_INS	ANC_CSUM_INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

2.4.1 Host Interface Map (R/W registers)

Table 2-5: Host Interface Map (R/W registers)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_LD_POSITION[12:0]	28h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	27h																
	26h																
ERROR_MASK_REGISTER	25h										VD_STD_ERR_MASK	FF_CRC_ERR_MASK	AP_CRC_ERR_MASK	LOCK_ERR_MASK	CCS_ERR_MASK	SAV_ERR_MASK	EAV_ERR_MASK
FF_PIXEL_END_F1[12:0]	24h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	14h																

Table 2-5: Host Interface Map (R/W registers) (Continued)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	13h																
	12h																
	11h																
	10h																
	0Fh																
ANC_TYPE(5)[15:0]	0Eh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(4)[15:0]	0Dh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(3)[15:0]	0Ch	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(2)[15:0]	0Bh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(1)[15:0]	0Ah	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_B[10:0]	09h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_EMPTY_OFFSET	06h					ANC_ DATA_ DELETE		b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h				ANC_ DATA_ SWITCH	STAT3_ CONFIG b2	STAT3_ CONFIG b1	STAT3_ CONFIG b0	STAT2_ CONFIG b2	STAT2_ CONFIG b1	STAT2_ CONFIG b0	STAT1_ CONFIG b2	STAT1_ CONFIG b1	STAT1_ CONFIG b0	STAT0_ CONFIG b2	STAT0_ CONFIG b1	STAT0_ CONFIG b0
DATA_FORMAT	04h					EDH_ FLAG_ UPDATE											
	03h																
	02h																
	01h																

Table 2-5: Host Interface Map (R/W registers) (Continued)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOPROC_DISABLE	00h							ANC_PKT_EXT	FIFO_MODE b1	FIFO_MODE b0	H_CONFIG			ILLEGAL_REMAP	EDH_CRC_INS	ANC_CSUM_INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

2.4.2 Host Interface Map (Read only registers)

Table 2-6: Host Interface Map (Read only registers)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	28h																
	27h																
	26h																
	25h																
	24h																
	23h																
	22h																
	21h																
	20h																
	1Fh																
	1Eh																
	1Dh																
	1Ch																
	1Bh																
	1Ah																
	19h																
	18h																
	17h																
	16h																
	15h																
RASTER_STRUCTURE4[10:0]	14h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Table 2-6: Host Interface Map (Read only registers) (Continued)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RASTER_STRUCTURE2[12:0]	12h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B(4,3)	10h	VFO4-b 7	VFO4-b 6	VFO4-b 5	VFO4-b 4	VFO4-b 3	VFO4-b 2	VFO4-b 1	VFO4-b 0	VFO3-b 7	VFO3-b 6	VFO3-b 5	VFO3-b 4	VFO3-b 3	VFO3-b 2	VFO3-b 1	VFO3-b 0
VIDEO_FORMAT_OUT_A(2,1)	0Fh	VFO2-b 7	VFO2-b 6	VFO2-b 5	VFO2-b 4	VFO2-b 3	VFO2-b 2	VFO2-b 1	VFO2-b 0	VFO1-b 7	VFO1-b 6	VFO1-b 5	VFO1-b 4	VFO1-b 3	VFO1-b 2	VFO1-b 1	VFO1-b 0
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
	09h																
	08h																
	07h																
	06h																
	05h																
DATA_FORMAT	04h						AP_CRC _V	FF_CRC_ V	EDH_ DETECT	VERSIO N_352M			STD_ LOCK	DATA_ FORMA T b3	DATA_ FORMA T b2	DATA_ FORMA T b1	DATA_ FORMA T b0
EDH_FLAG_OUT	03h	Not Used	ANC-UE S	ANC-ID A	ANC-ID H	ANC-ED A	ANC-ED H	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
EDH_FLAG_IN	02h	Not Used	ANC-UE S _IN	ANC-ID A _IN	ANC-ID H _IN	ANC-ED A _IN	ANC-ED H _IN	FF-UES_I N	FF-IDA_I N	FF-IDH_I N	FF-EDA_ IN	FF-EDH_ IN	AP-UES_ IN	AP-IDA_ IN	AP-IDH_ IN	AP-EDA _IN	AP-EDH _IN
ERROR_STATUS	01h										VD_STD _ ERR	FF_CRC_ ERR	AP_CRC _ ERR	LOCK_ ERR	CCS_ER R	SAV_ER R	EAV_ER R

Table 2-6: Host Interface Map (Read only registers) (Continued)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	00h																

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).