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June 1997 Revised December 2000

# GTLP16616 17-Bit TTL/GTLP Bus Transceiver with Buffered Clock

## **General Description**

The GTLP16616 is a 17-bit registered bus transceiver that provides TTL to GTLP signal level translation. It allows for transparent, latched and clocked modes of data flow and provides a buffered GTLP (CLKOUT) clock output from the TTL CLKAB. The device provides a high speed interface between cards operating at TTL logic levels and a back-plane operating at GTLP logic levels. High speed back-plane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transceiver logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage, and temperature (PVT) compensated. Its function is similar to BTL and GTL but with different output levels and receiver threshold. GTLP output LOW level is typically less than 0.5V, the output level HIGH is 1.5V and the receiver threshold is 1.0V.

#### **Features**

- Bidirectional interface between GTLP and TTL logic levels
- Designed with edge rate control circuitry to reduce output noise on the GTLP port
- V<sub>REF</sub> pin provides external supply reference voltage for receiver threshold adjustibility
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible driver and control inputs
- Designed using Fairchild advanced CMOS technology
- Bushold data inputs on the A port eliminates the need for external pull-up resistors on unused inputs.
- Power up/down and power off high impedance for live insertion
- 5 V tolerant inputs and outputs on the LVTTL ports
- Open drain on GTLP to support wired-or connection
- Flow through pinout optimizes PCB layout
- $\hfill \blacksquare$  D-type flip-flop, latch and transparent data paths
- A Port source/sink –32 mA/+32 mA
- GTLP Buffered CLKAB signal available (CLKOUT)

## **Ordering Code:**

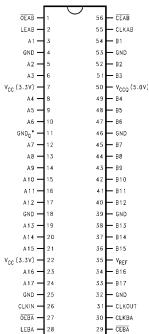
Order Number	Package Number	Package Description				
GTLP16616MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118 0.300" Wide				
GTLP16616MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide				

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

## **Pin Descriptions**

Pin Names	Description			
OEAB	A-to-B Output Enable (Active LOW)			
OEBA	B-to-A Output Enable (Active LOW)			
CEAB	A-to-B Clock Enable (Active LOW)			
CEBA	B-to-A Clock Enable (Active LOW)			
LEAB	A-to-B Latch Enable (Transparent HIGH)			
LEBA	B-to-A Latch Enable (Transparent HIGH)			
V <sub>REF</sub>	GTLP Reference Voltage			
CLKAB	A-to-B Clock			
CLKBA	B-to-A Clock			
A1-A17	A-to-B Data Inputs or B-to-A 3-STATE Outputs			
B1-B17	B-to-A Data Inputs or			
	A-to-B Open Drain Outputs			
CLKIN	B-to-A Buffered Clock Output			
CLKOUT	GTLP Buffered Clock Output of CLKAB			

# **Connection Diagram**



## **Functional Description**

The GTLP16616 is a 17 bit registered transceiver containing D-type flip-flop, latch and transparent modes of operation for the data <u>path</u> and a <u>GTLP</u> translation of the CLKAB signal (CLKOUT). Data flow in each direction is controlled by <u>the clock enables</u> (<u>CEAB</u> and <u>CEBA</u>), <u>latch enables</u> (<u>LEAB</u> and LEBA), clock (CLKAB and CLKBA) and <u>output enables</u> (<u>OEAB</u> and <u>OEBA</u>). The clock enables (<u>CEAB</u> and <u>OEBA</u>) enable all 17 bits. The output enables (<u>OEAB</u> and <u>OEBA</u>) control both the 17 bits of data and the CLKOUT/CLKIN buffered clock path.

For A-to-B data flow, when  $\overline{\text{CEAB}}$  is LOW, the device operates on the LOW-to-HIGH transition of CLKAB for the flip-flop and on the HIGH-to-LOW transition of LEAB for the latch path. That is, if  $\overline{\text{CEAB}}$  is LOW and LEAB is LOW the A data is latched regardless as to the state of CLKAB (HIGH or LOW) and if LEAB is HIGH the device is in transparent mode. When  $\overline{\text{OEAB}}$  is LOW the <u>outputs are active</u>. When  $\overline{\text{OEAB}}$  is HIGH the outputs are HIGH impedance. The data flow of B-to-A is similar except that  $\overline{\text{CEBA}}$ ,  $\overline{\text{OEBA}}$ , LEBA and CLKBA are used.

#### **Truth Table**

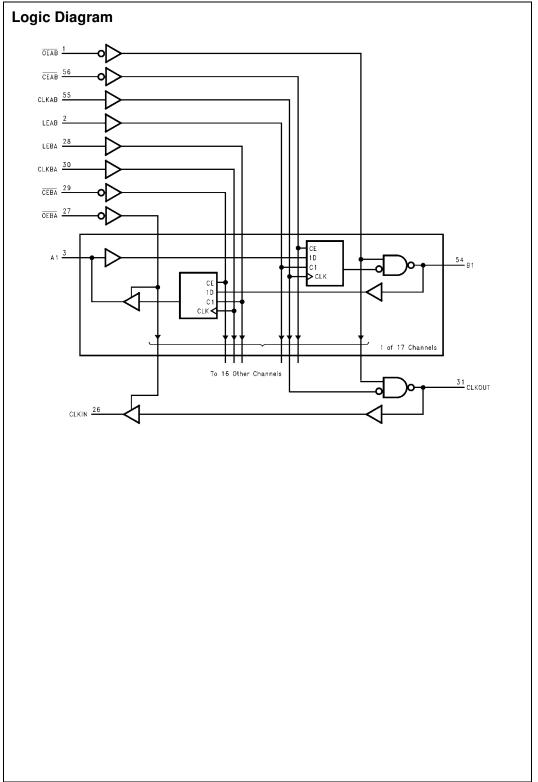
(Note 1)

Inputs				Output	Mode	
CEAB	OEAB	LEAB	CLKAB	Α	В	
Х	Н	Х	Х	Х	Z	Latched
L	L	L	Н	Χ	B <sub>0</sub> (Note 2)	storage
L	L	L	L	X	B <sub>0</sub> (Note 3)	of A data
Х	L	Н	Χ	L	L	Transparent
Х	L	Н	Χ	Н	Н	
L	L	L	1	L	L	Clocked storage
L	L	L	$\uparrow$	Н	Н	of A data
Н	L	L	Χ	Х	B <sub>0</sub> (Note 3)	Clock inhibit

 $\textbf{Note 1:} \ A-to-B \ data \ flow \ is \ shown. \ B-to-A \ data \ flow \ is \ similar \ but \ uses \ \overline{OEBA}, \ LEBA, \ CLKBA, \ and \ \overline{CEBA}.$ 

Note 2: Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH prior to LEAB going LOW.

Note 3: Output level before the indicated steady-state input conditions were established.



#### **Absolute Maximum Ratings**(Note 4) **Recommended Operating**

Conditions (Note 6)

-0.5V to +7.0V Supply Voltage (V<sub>CC</sub>) DC Input Voltage (V<sub>I</sub>) -0.5V to +7.0V

DC Output Voltage (V<sub>O</sub>)

Outputs 3-STATE -0.5V to +7.0VOutputs Active (Note 5) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Sink Current into

A Port I<sub>OL</sub> 64 mA

DC Output Source Current from

-64 mA A Port I<sub>OH</sub>

DC Output Sink Current

into B Port in the LOW State,  $\rm I_{OL}$ 80 mA DC Input Diode Current (I<sub>IK</sub>)

 $V_I < 0V$ -50 mA

DC Output Diode Current ( $I_{OK}$ )

 $V_{O} < 0V$ -50 mA  $V_{O} > V_{CC}$ +50 mA **ESD** Rating >2000V

Storage Temperature (T<sub>STG</sub>) -65°C to +150°C

Supply Voltage  $V_{\rm CC}$ 

3.15V to 3.45V  $V_{CC}$  $V_{CCQ}$ 4.75V to 5.25V Bus Termination Voltage (V<sub>TT</sub>) GTLP 1.35V to 1.65V

Input Voltage (V<sub>I</sub>)

on A Port and Control Pins 0.0V to 5.5V

HIGH Level Output Current (I<sub>OH</sub>)

A Port -32 mA

LOW Level Output Current (I<sub>OL</sub>)

A Port +32 mA B Port +34 mA -40°C to +85°C

Operating Temperature  $(T_A)$ 

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be

operated at these limits. The parametric values defined in the Electrical Characteristics tables are not quaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions

for actual device operation.

Note 5: I<sub>O</sub> Absolute Maximum Rating must be observed.

Note 6: Unused inputs must be held HIGH or LOW.

#### **DC Electrical Characteristics**

Over Recommended Operating Free-Air Temperature Range,  $V_{REF} = 1.0V$  (unless otherwise noted).

	Symbol	Test Conditi	ons	Min	Typ (Note 7)	Max	Units
V <sub>IH</sub>	B Port			V <sub>REF</sub> +0.1		$V_{TT}$	٧
	Others			2.0			V
V <sub>IL</sub>	B Port			0.0		V <sub>REF</sub> -0.1	V
	Others					0.8	V
$V_{REF}$	GTLP				1.0		V
	GTL				0.8		V
$V_{IK}$		V <sub>CC</sub> = 3.15V,	I <sub>I</sub> = -18 mA			-1.2	V
		V <sub>CCQ</sub> = 4.75V					
$V_{OH}$	A Port	V <sub>CC</sub> , V <sub>CCQ</sub> = Min to Max (Note 8)	$I_{OH} = -100 \ \mu A$	V <sub>CC</sub> -0.2			
		V <sub>CC</sub> = 3.15V	$I_{OH} = -8 \text{ mA}$	2.4			V
		V <sub>CCQ</sub> = 4.75V	$I_{OH} = -32 \text{ mA}$	2.0			
V <sub>OL</sub>	A Port	V <sub>CC</sub> , V <sub>CCQ</sub> = Min to Max (Note 8)	$I_{OL} = 100 \mu A$			0.2	
		V <sub>CC</sub> = 3.15V	$I_{OL} = 32 \text{ mA}$			0.5	V
		V <sub>CCQ</sub> = 4.75V					
	B Port	V <sub>CC</sub> = 3.15V V <sub>CCQ</sub> = 4.75V	$I_{OL} = 34 \text{ mA}$			0.65	V
I	Control Pins	V <sub>CC</sub> , V <sub>CCQ</sub> = 0 or Max	$V_I = 5.5V$ or $0V$			±10	μΑ
	A Port	V <sub>CC</sub> = 3.45V	$V_1 = 5.5V$			20	
		V <sub>CCQ</sub> = 5.25V	$V_I = V_{CC}$			1	μΑ
			$V_I = 0$			-30	
	B Port	V <sub>CC</sub> = 3.45V	$V_I = V_{CC}$			5	
		V <sub>CCQ</sub> = 5.25V	$V_I = 0$			-5	μΑ
l <sub>OFF</sub>	A Port and Control Pins	$V_{CC} = V_{CCQ} = 0$	$V_I$ or $V_O = 0$ to 4.5V			100	μΑ
I <sub>I(hold)</sub>	A Port	V <sub>CC</sub> = 3.15V,	$V_1 = 0.8V$	75			
		V <sub>CCQ</sub> = 4.75V	$V_1 = 2.0V$	-20			μΑ
l <sub>OZH</sub>	A Port	V <sub>CC</sub> = 3.45V,	$V_O = 3.45V$			1	
	B Port	V <sub>CCQ</sub> = 5.25V	V <sub>O</sub> = 1.5V			5	μΑ
l <sub>OZL</sub>	A Port	V <sub>CC</sub> = 3.45V,	V <sub>O</sub> = 0			-20	
	B Port	V <sub>CCO</sub> = 5.25V	$V_{O} = 0.65V$	1		-10	μΑ

# DC Electrical Characteristics (Continued)

Symbol		Test Condition	Test Conditions		Typ (Note 7)	Max	Units
I <sub>CCQ</sub>	A or B	V <sub>CC</sub> = 3.45V,	Outputs HIGH		30	40	
(V <sub>CCQ</sub> )	Ports	$V_{CCQ} = 5.25V$ ,	Outputs LOW		30	40	mA
		$I_O = 0$ ,					IIIA
		$V_I = V_{CCQ}$ or GND	Outputs Disabled		30	40	
I <sub>CC</sub>	A or B	$V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_{O} = 0,$	Outputs HIGH		0	1	
(V <sub>CC</sub> )	Ports		Outputs LOW		0	1	mA
		$V_I = V_{CC}$ or GND	Outputs Disabled		0	1	
$\Delta I_{CC}$	A Port and	$V_{CC} = 3.45V,$	One Input at 2.7V		0	1	
(Note 9)	Control Pins	$V_{CC} = 5.25V$ ,					mA
		A or Control Inputs at					IIIA
		V <sub>CC</sub> or GND					
C <sub>IN</sub>	Control Pins		$V_I = V_{CCQ}$ or 0		8		
C <sub>I/O</sub>	A Port		$V_I = V_{CCQ}$ or 0		9		pF
C <sub>I/O</sub>	B Port		$V_I = V_{CCQ}$ or 0		6		

Note 7: All typical values are at  $V_{CC}=3.3 V,\, V_{CCQ}=5.0 V,$  and  $T_A=25^{\circ}C.$ 

Note 8: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Note 9: This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

# **AC Operating Requirements**

Over recommended ranges of supply voltage and operating free-air temperature,  $V_{REF} = 1.0V$  (unless otherwise noted).

Symbol			Min	Max	Unit
f <sub>MAX</sub>	Maximum Clock Frequency		175		MHz
t <sub>W</sub>	Pulse Duration	LEAB or LEBA HIGH	3.0		
		CLKAB or CLKBA HIGH or LOW	3.2		ns
t <sub>S</sub>	Setup Time	A before CLKAB↑	0.5		
		B before CLKBA↑	3.1		
		A before LEAB↓	1.3		
		B before LEBA↓	3.7		ns
		CEAB before CLKAB↑	0.7		
		CEBA before CLKBA↑	1.0		
t <sub>H</sub>	Hold Time	A after CLKAB↑	1.5		
		B after CLKBA↑	0.0		
		A after LEAB↓	0.5		
		B after LEBA↓	0.0		ns
		CEAB after CLKAB↑	1.5		
		CEBA after CLKBA↑	1.7		

## **AC Electrical Characteristics**

Over recommended range of supply voltage and operating free-air temperature,  $V_{REF}=1.0V$  (unless otherwise noted).  $C_L=30$  pF for B Port and  $C_L=50$  pF for A Port.

Symbol	From	То	Min	Тур	Max	Unit
	(Input)	(Output)		(Note 10)		
PLH	Α	В	1.0	4.3	6.5	
PHL			1.0	5.0	8.2	ns
t <sub>PLH</sub>	LEAB	В	1.8	4.5	6.7	20
t <sub>PHL</sub>			1.5	5.3	8.7	ns
PLH	CLKAB	В	1.8	4.6	6.7	
PHL			1.5	5.4	8.7	ns
PLH	CLKAB	CLKOUT	3.0	6.2	10.0	
t <sub>PHL</sub>			3.0	5.7	10.0	ns
t <sub>PLH</sub>	OEAB	B or CLKOUT	1.6	4.4	6.3	ns
PHL			1.3	6.1	9.8	
SKEW	B (Note 11)	CLKOUT	0		2	ns
RISE	Transition time, B o	outputs (20% to 80%)		2.6		no
FALL	Transition time, B o	outputs (20% to 80%)		2.6		ns
PLH	В	А	2.0	5.6	8.2	no
PHL			1.4	5.0	7.2	ns
PLH	LEBA	A	2.1	4.2	6.3	
PHL			1.9	3.3	5.0	ns
PLH	CLKBA	A	2.3	4.4	6.8	ne
PHL			2.1	3.5	5.2	ns
PLH	CLKOUT	CLKIN	3.0	6.0	10.0	ne
PHL			3.0	6.4	10.0	ns
<sub>PZH</sub> , t <sub>PZL</sub>	OEBA	A or CLKIN	1.5	5.0	6.4	-
PHZ, tPLZ			1.4	3.9	8.0	ns

Note 10: All typical values are at  $V_{CC}=3.3V,\ V_{CCQ}=5.0V,\ and\ T_A=25^{\circ}C.$ 

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delays for the CLKOUT pin and any B output transition when measured with reference to CLKAB1. This guarantees the relationship between B output data and CLKOUT such that data is coincident or ahead of CLKOUT. This specification is guaranteed but not tested.

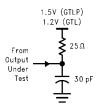
# **Test Circuits and Timing Waveforms**

#### **Test Circuit for A Outputs**

# From Output $C_L = 50 \text{ pF}$ $S_{00\Omega}$ $S_{00D}$ $S_{00D}$

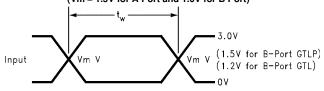
C<sub>L</sub> includes probes and jig capacitance.

#### **Test Circuit for B Outputs**

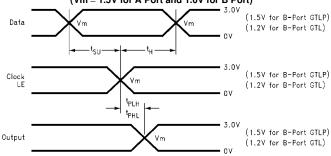


 $\mbox{C}_L$  includes probes and jig capacitance. For B Port outputs,  $\mbox{C}_L=30$  pF is used for worst case edge rate.

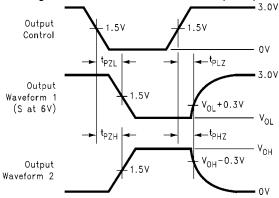
# Voltage Waveforms Pulse Duration (Vm = 1.5V for A Port and 1.0V for B Port)



# Voltage Waveforms Propagation Delay and Setup and Hold Times (Vm = 1.5V for A Port and 1.0V for B Port)



#### Voltage Waveforms Enable and Disable Times (A Port)



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. All input pulses have the following characteristics: frequency = 10 MHz,  $t_r = t_f = 2$  ns,  $Z_O = 50\Omega$ . The outputs are measured one at a time with one transition per measurement.

# Physical Dimensions inches (millimeters) unless otherwise noted 0.720 - 0.730 [18.30 - 18.54] - A -ĬŎ₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽₽ 0.398 - 0.417 [10.10 - 10.60] LEAD #1 ⊕ 0.010[0.25] C B S A S 0.291 - 0.299 [7.40 - 7.59] \_0.005 - 0.009 [0.13 - 0.22] - 0.025 [0.635] TYP 0.020 ±0.003 [0.51 ±0.08] TYP-GAUGE PLANE = 0.008 - 0.012 [0.21 - 0.30] TYP --0.010 [0.25] 0.020 - 0.040 [0.51 - 1.01] DETAIL E TYP 45° x 0.015 - 0.025 [0.39 - 0.63] 0.096 - 0.108 [2.44 - 2.74] SEATING PLANE SEE DETAIL E - D -☐ 0.004[0.10] 0.010 [0.25] MIN TYP - C -0.025 [0.635] TYP MS56A (REV E) 56-Lead Shrink Small Outline Package, JEDEC MO-118 0.300" Wide Package Number MS56A

MTD56 (REV B)

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 14.0 ± 0.1 -A-SYMM Ç (9.2 TYP) 8.1 -B-(5.6 TYP) 4.05 □ 0.2 C B A . + (0.3 TYP) ALL LEAD TIPS - (0.5 TYP) LAND PATTERN RECOMMENDATION □ 0.1 C SEE DETAIL A ALL LEAD TIPS (0.90) **ФИНЕНИЛИ ТОВЕТИТЕ В В 1.1** МАХ - 0.5 TYP 0.17 - 0.27 TYP └ 0.10 ± 0.05 TYP | Φ | 0.13 M | A | B S | C S GAGE PLANE <sub>□</sub>0.25 SEATING PLANE 0.60 +0.15

56-Lead Thin Shrink Small Outline Package, JEDEC MO-153, 6.1mm Wide Package Number MTD56

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