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FAIRCHILD SEMICONDUCTOR™

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GTLP16T1655
16-Bit LVTTL/GTLP Universal Bus Transceiver with High Drive GTLP and Individual Byte Controls

General Description

The GTLP16T1655 is a 16-bit universal bus transceiver that provides LVTTL to GTLP signal level translation. It allows for transparent, latched and clocked modes of data transfer. The device provides a high speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP logic levels. High speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage, and temperature (PVT) compensated. Its function is similar to BTL and GTL but with different output levels and receiver threshold. GTLP output LOW level is typically less than 0.5V, the output level HIGH is 1.5V and the receiver threshold is 1.0V.

Features

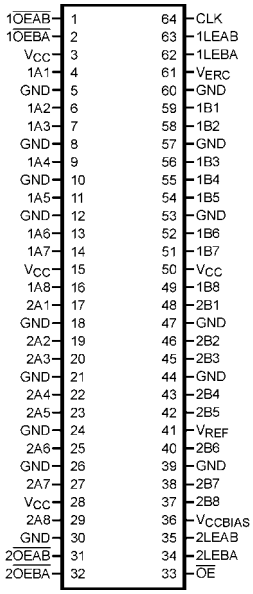
- Bidirectional interface between GTLP and LVTTL logic levels
- Variable edge rate control pin to select desired edge rate on the GTLP backplane (V_{ERC})
- V_{REF} pin provides external supply reference voltage for receiver threshold adjustibility
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible driver and control inputs
- Designed using Fairchild advanced BiCMOS technology
- Bushold data inputs on A port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down and power off high impedance for live insertion
- Open drain on GTLP to support wired-or connection
- Flow through pinout optimizes PCB layout
- D-type flip-flop, latch and transparent data paths
- A Port source/sink –24mA/+24mA
- B Port sink +100mA
- Partitioned as two 8-bit transceivers with individual latch timing and output control but with a common clock
- External pin to pre-condition I/O capacitance to high state (V_{CCBIAS})

Ordering Code:

Order Number	Package Number	Package Description
GTLP16T1655MTD	MTD64	64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
$1\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$2\overline{OEAB}$	Byte 1 and Byte 2
$1\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$2\overline{OEBA}$	Byte 1 and Byte 2
$\overline{OE}$	Disables all I/O ports simultaneously
1LEAB	A-to-B Latch Enable (Transparent HIGH)
2LEAB	Byte 1 and Byte 2
1LEBA	B-to-A Latch Enable (Transparent HIGH)
2LEBA	Byte 1 and Byte 2
V_{REF}	GTLP Reference Voltage
CLK	A-to-B and B-to-A Clock
1A1-1A8	A Port I/O Byte 1 and Byte 2
2A1-2A8	
1B1-1B8	B Port I/O Byte 1 and Byte 2
2B1-2B8	

Truth Tables

(Note 1)

Inputs				Output	Mode
$\overline{OEAB}$	LEAB	CLK	A	B	
H	X	X	X	Z	High Impedance
L	H	X	L	L	Transparent
L	H	X	H	H	Transparent
L	L	↑	L	L	Registered
L	L	↑	H	H	Registered
L	L	H	X	B_0 (Note 2)	Previous State
L	L	L	X	B_0 (Note 3)	Previous State

Inputs			Outputs	
$\overline{OE}$	$\overline{OEAB}$ (Note 4)	$\overline{OEBA}$ (Note 4)	A Port	B Port
L	L	L	Active	Active
L	L	H	Z	Active
L	H	L	Active	Z
L	H	H	Z	Z
H	X	X	Z	Z

Inputs	Output Edge
V_{ERC}	B Port
V_{CC}	Slow
GND	Fast

Note 1: A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLK.

Note 2: Output level before the indicated steady state input conditions were established, provided CLK was HIGH prior to LEAB going LOW.

Note 3: Output level before the indicated steady state input conditions were established.

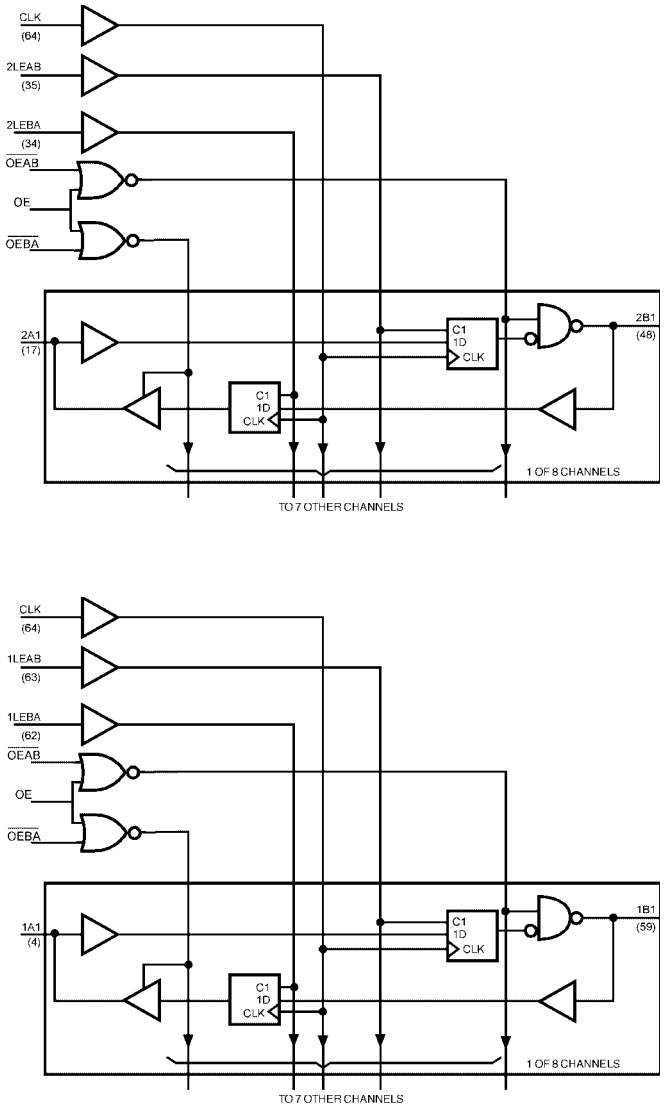
Note 4: $\overline{OEAB}$ and $\overline{OEBA}$ are byte-wide enables. Each is proceeded by a number indicating the byte controlled.

Functional Description

The GTLP16T1655 is a high drive (100 mA) 16-bit universal bus transceiver containing D-type flip-flop, latch and transparent modes of operation for the data path. The device is uniquely partitioned as two 8-bit transceivers with individual latch timing and output control signals but with a common clock pin (CLK) for both transceiver words. Data flow for each word is determined by the respective latch enables (xLEAB and xLEBA), output enables (x$\overline{\text{OEAB}}$ and x$\overline{\text{OEBA}}$) and clock (CLK). The output enables (1$\overline{\text{OEAB}}$, 1$\overline{\text{OEBA}}$, and 2$\overline{\text{OEAB}}$ and 2$\overline{\text{OEBA}}$) control Byte1 and Byte2 data for the A to B and B to A directions respectively.

For A-to-B data flow, the devices operate in the transparent mode when LEAB is HIGH. When LEAB transitions LOW, the A data is latched independent of CLK HIGH or LOW. If LEAB is LOW the A data is registered on the CLK LOW-to-HIGH transition. When $\overline{\text{OEAB}}$ is LOW the outputs are active. With $\overline{\text{OEAB}}$ HIGH the outputs are HIGH impedance. Data flow for the B-to-A direction is identical but uses $\overline{\text{OEBA}}$, LEBA and CLK. Note that CLK is common to both directions and both 8-bit words. $\overline{\text{OE}}$ is also common and is used to disable all I/O ports simultaneously.

Logic Diagrams



Absolute Maximum Ratings(Note 5)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 6)	−0.5V to + 4.6V
DC Output Sink Current into	
A Port I_{OL}	48 mA
DC Output Source Current from	
A Port I_{OH}	−48 mA
DC Output Sink Current	
into B Port in the LOW State,	200 mA
I_{OL} (Note 7)	
DC Input Diode Current (I_{IK})	
$V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
$V_O > V_{CC}$	+50 mA
ESD Rating	>2000V
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage V_{CC}	3.0V to 3.6V
Bus Termination Voltage (V_{TT})	
GTLP	1.35V to 1.65V
GTL	1.14V to 1.26V
V_{REF}	
GTLP	0.87V to 1.1V
GTL	0.74V to 0.87V
Input Voltage (V_I)	
on A Port and Control Pins	0.0V to V_{CC}
on B Port	0.0V to V_{tt}
HIGH Level Output Current (I_{OH})	
A Port	−24 mA
LOW Level Output Current (I_{OL})	
A Port	+24mA
B Port	+100 mA
Operating Temperature (T_A)	−40°C to +85°C

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: V_{TT} and R_{term} can be adjusted to accommodate backplane impedances other than 50Ω, within the boundaries of not exceeding the DC Absolute I_{OL} ratings (200 mA). Similarly V_{REF} can be adjusted to compensate for changes in V_{TT}.

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (unless otherwise noted).

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
V_{IH}	B Port			V_{REF} +0.05		V_{TT}	V
	Others			2.0			V
V_{IL}	B Port			0.0		V_{REF} −0.05	V
	Others					0.8	V
V_{REF}	GTLP			0.74	1.0	1.1	V
V_{IK}		V_{CC} = 3.0V	I_I = −18 mA			−1.2	V
V_{OH}	A Port	V_{CC} = Min to Max (Note 9)	I_{OH} = −100 µA	V_{CC} −0.2			V
		V_{CC} = 3.0V	I_{OH} = −12 mA	2.4			
			I_{OH} = −24 mA	2.2			
V_{OL}	A Port	V_{CC} = Min to Max (Note 9)	I_{OL} = 100 µA			0.20	V
		V_{CC} = 3.0V	I_{OL} = 12 mA			0.40	
			I_{OL} = 24 mA			0.50	
	B Port	V_{CC} = 3.0V	I_{OL} = 40 mA			0.20	V
			I_{OL} = 80 mA			0.40	
			I_{OL} = 100 mA			0.50	
I_I	A Port	V_{CC} = 3.6V	$V_I = V_{CC}$ or 0V			±10	µA
	Control Pins	V_{CC} = 3.6V	$V_I = V_{CC}$ or 0V			±10	µA
	B Port	V_{CC} = 3.6V	$V_I = V_{TT}$ or GND			±10	µA
I_{OFF}	Except V_{ERC}	V_{CC} = 0	V_I or V_O = 0 to V_{CC}			100	µA
$I_{I(hold)}$	A Port	V_{CC} = 3.0V	V_I = 0.8V	75			µA
			V_I = 2.0V	−75			
		V_{CC} = 3.6V	V_I = 0 to V_{CC}			±500	

DC Electrical Characteristics (Continued)

Symbol		Test Conditions		Min	Typ (Note 8)	Max	Units
I_{OZH}	A Port	V_{CC} = 3.6V	$V_O = V_{CC}$			10	µA
	B Port		V_O = 1.5V			10	
I_{OZL}	A Port	V_{CC} = 3.6V	V_O = 0V			−10	µA
	B Port		V_O = 0.4V			−10	
I_{OZPU} (Note 10)	A Port	V_{CC} = 0 to 1.5V, $\overline{OE}$ = 0 or V_{CC}	V_O = 0.5 to 3V			±50	µA
I_{OZPD} (Note 10)	A Port	V_{CC} = 1.5 to 0V, $\overline{OE}$ = 0 or V_{CC}	V_O = 0.5 to 3V			±50	µA
I_{CC} (v_{cc})	A or B Ports	V_{CC} = 3.6	Outputs HIGH			55	mA
		I_O = 0	Outputs LOW			55	
		$V_I = V_{CC}$ or GND	Outputs Disabled			55	
ΔI_{CC} (Note 11)	A Port and Control Pins	V_{CC} = 3.6V, A or Control Inputs at V_{CC} or GND	One Input at V_{CC}–0.6		0	1	mA
C_i	Control Pins		$V_I = V_{CC}$ or 0		5.8	7.0	pF
	A Port		$V_I = V_{CC}$ or 0		8.0	9.5	
	B Port		$V_I = V_{CC}$ or 0		8.3	9.9	

Note 8: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

Note 9: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Note 10: This is specified by characterization but not tested.

Note 11: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Live Insertion Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (unless otherwise noted).

Parameter		Test Conditions		Min	Typ	Max	Units
I_{CC}	B Port	V_{CC} = 0 to 3V	V_O = 0 to 1.2V			5	mA
(V_{CC}BIAS)		V_{CC} = 3.0 to 3.6V	V_I (V_{CC}BIAS) = 3 to 3.6V			10	µA
V_O	B Port	V_{CC} = 0 V_I (V_{CC}BIAS) = 3.3v			1.1		V
I_O	B Port	V_{CC} = 0 V_I (V_{CC}BIAS) = 3 to 3.6V V_O = 0.4		−1			µA
		V_{CC} = 0 to 3.6V $\overline{OE}$ = 3.3V				100	
		V_{CC} = 0 to 1.5V $\overline{OE}$ = 0 to 3.3V				100	

AC Operating Requirements (GTLP)

Over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5V and V_{ref} = 1.0V (unless otherwise noted).

Parameter			Min	Max	Unit
f_{MAX}	Maximum Clock Frequency		160		MHz
t_{WIDTH}	Pulse Duration	LE HIGH	3.0		ns
		CLK HIGH or LOW	3.0		
t_{SU}	Setup Time	Data before CLK↑	2.5		ns
		Data before LE↓ (CLK = X)	2.5		
t_{HOLD}	Hold Time	Data after CLK↑	0.5		ns
		Data after LE↓ (CLK = X)	0.5		

B to A AC Electrical Characteristics (GTLP)

Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 1.0V, V_{TT} = 1.5V, V_{ERC} = V_{CC} or GND (unless otherwise noted). C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Parameter	From (Input)	To (Output)	Min	Typ (Note 12)	Max	Unit
f_{MAX}			160			MHz
t_{PLH}	B	A	1.0		4.7	ns
t_{PHL}			1.5		4.8	
t_{PLH}	LEAB	A	1.2		4.0	ns
t_{PHL}			1.2		3.8	
t_{PLH}	CLK	A	1.2		4.0	ns
t_{PHL}			1.2		4.0	
$t_{PLZ/HZ}$	$\overline{OE}$	A	1.4		4.5	ns
$t_{PZH/ZL}$			1.0		4.0	
$t_{PLZ/HZ}$	$\overline{OEBA}$	A	1.2		4.9	ns
$t_{PZH/ZL}$			1.0		4.0	

Note 12: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

A to B AC Electrical Characteristics (GTLP)

Over recommended range of supply voltage and operating free air temperature, V = 1.0V, V_{TT} = 1.5V (unless otherwise noted).
C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Type (Note 13)	Max	Units
f_{MAX}			160			MHz
t_{PLH}	A	B	2.6		5.7	ns
t_{PHL}	$V_{ERC} = V_{CC}$		0.8		4.5	
t_{PLH}	A	B	2.0		4.9	ns
t_{PHL}	V_{ERC} = GND		0.7		4.0	
t_{PLH}	LEAB	B	2.6		5.7	ns
t_{PHL}	$V_{ERC} = V_{CC}$		0.8		4.0	
t_{PLH}	LEAB	B	2.2		4.9	ns
t_{PHL}	V_{ERC} = GND		0.7		4.0	
t_{PLH}	CLK	B	2.8		5.7	ns
t_{PHL}	$V_{ERC} = V_{CC}$		1.0		4.0	
t_{PLH}	CLK	B	2.3		5.0	ns
t_{PHL}	V_{ERC} = GND		0.8		4.0	
t_{PLH}	$\overline{OE}$	B	2.7		5.8	ns
t_{PHL}	$V_{ERC} = V_{CC}$		0.6		4.0	
t_{PLH}	$\overline{OE}$	B	2.1		4.9	ns
t_{PHL}	V_{ERC} = GND		1.0		4.0	
t_{PLH}	$\overline{OEAB}$	B	2.6		5.8	ns
t_{PHL}	$V_{ERC} = V_{CC}$		0.6		4.0	
t_{PLH}	$\overline{OEAB}$	B	2.0		4.9	ns
t_{PHL}	V_{ERC} = GND		0.6		3.5	
$t_{FALL/RISE}$ $V_{ERC} = V_{CC}$	Transition Time, B outputs (0.6V to 1.3V)		0.7/0.7	2.0/2.5		ns
$t_{FALL/RISE}$ V_{ERC} = GND	Transition Time, B outputs (0.6V to 1.3V)		0.7/0.7	1.5/2.0		ns

Note 13: All Typical values are at V_{CC} = 3.3V and T_A = 25°C

Extended Electrical Characteristics (GTLP)

Over recommended ranges of supply voltage and operating free-air temperature V_{REF} = 1.0V (unless otherwise noted).
C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 14)	Max	Unit
t_{OSLH} (Note 15)	A	B		0.4	1.0	ns
t_{OSHL} (Note 15)				0.4	1.0	ns
$t_{PV(HL)}$ (Note 16) (Note 17)	A	B			1.5	ns
t_{OSLH} (Note 15)	CLKAB	B		0.3	0.9	ns
t_{OSHL} (Note 15)				0.3	0.6	ns
$t_{PV(HL)}$ (Note 16)(Note 17)	CLKAB	B			1.2	ns
t_{OSLH} (Note 15)	B	A		0.3	1.0	ns
t_{OSHL} (Note 15)				0.3	1.0	ns
t_{OST} (Note 15)	B	A		0.6	1.5	ns
t_{PV} (Note 16)	B	A			1.6	ns
t_{OSLH}(Note 15)	CLKAB	A		0.3	0.6	ns
t_{OSHL} (Note 15)				0.3	0.6	ns
t_{OST}(Note 15)	CLKAB	A		0.5	1.0	ns
t_{PV} (Note 16)	CLKAB	A			1.1	ns

Note 14: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

Note 15: t_{OSHL}/t_{OSLH} and t_{OST}—Output to output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs within the same packaged device. The specifications are given for specific worst case V_{CC} and temperature and apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

Note 16: t_{PV}—Part to part skew is defined as the absolute value of the difference between the actual propagation delay for all outputs from device to device. The parameter is specified for a specific worst case V_{CC} and temperature. This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

Note 17: Due to the open drain structure on GTLP outputs, t_{OST} and $t_{PV(LH)}$ in the A-to-B direction are not specified. Skew on these paths is dependent on the V_{TT} and R_T values on the backplane.

AC Operating Requirements (GTL)

Over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2V and V_{ref} = 0.8V (unless otherwise noted).

Parameter			Min	Max	Units
f_{MAX}	Maximum Clock Frequency		160		MHz
t_{WIDTH}	Pulse Duration	LE HIGH	3.0		ns
		CLK HIGH or LOW	3.0		ns
t_{SU}	Setup Time	Data before CLK↑	2.5		ns
		Data before LE↓ (CLK = X)	2.5		
t_{HOLD}	Hold Time	Data after CLK↑	0.5		ns
		Data after LE↓ (CLK =X)	0.5		

B to A AC Electrical Characteristics (GTL)

Over recommended range of supply voltage and operating free air temperature, V_{ref} = 0.8V, V_{TT} = 1.2V, V_{ERC} = V_{CC} or GND (unless otherwise noted). C_L = 30pF for B Port and C_L = 50 pF for A Port.

Parameter	From (Input)	To (Output)	Min	Typ (Note 18)	Max	Units
f_{MAX}			160			MHz
t_{PLH}	B	A	1.0		4.7	ns
t_{PHL}			1.2		4.8	
t_{PLH}	LEBA	A	1.0		4.4	ns
t_{PHL}			1.1		4.0	
t_{PLH}	CLK	A	1.0		4.2	ns
t_{PHL}			1.1		4.1	
$t_{PLZ/HZ}$	$\overline{OE}$	A	1.5		4.6	ns
$t_{PZH/ZL}$			1.2		4.2	
$t_{PLZ/HZ}$	$\overline{OEBA}$	A	1.2		4.9	ns
$t_{PZH/ZL}$			1.0		4.0	

Note 18: All Typical values are at V_{CC} = 3.3V and T_A = 25°C.

A to B AC Electrical Characteristics (GTL)

Over recommended range of supply voltage and operating free air temperature, V_{REF} = 0.8V, V_{TT} = 1.2V (unless otherwise noted). C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 19)	Max	Units
f_{MAX}			160			MHz
t_{PLH}	A	B	2.2		5.7	ns
t_{PHL}	$V_{ERC} = V_{CC}$		1.0		4.7	
t_{PLH}	A	B	1.5		4.8	ns
t_{PHL}	V_{ERC} = GND		0.9		4.0	
t_{PLH}	LEAB	B	2.2		5.7	ns
t_{PHL}	$V_{ERC} = V_{CC}$		1.0		4.1	
t_{PLH}	LEAB	B	1.7		5.0	ns
t_{PHL}	V_{ERC} = GND		0.9		4.4	
t_{PLH}	CLK	B	2.8		5.8	ns
t_{PHL}	$V_{ERC} = V_{CC}$		1.0		4.3	
t_{PLH}	CLK	B	2.3		5.0	ns
t_{PHL}	V_{ERC} = GND		1.0		4.3	
t_{PLH}	$\overline{OE}$	B	2.5		5.8	ns
t_{PHL}	$V_{ERC} = V_{CC}$		0.8		4.3	
t_{PLH}	$\overline{OE}$	B	1.7		4.9	ns
t_{PHL}	V_{ERC} = GND		0.9		4.3	
t_{PLH}	$\overline{OEAB}$	B	2.2		5.8	ns
t_{PHL}	$V_{ERC} = V_{CC}$		0.8		4.3	
t_{PLH}	$\overline{OEAB}$	B	1.7		4.9	ns
t_{PHL}	V_{ERC} = GND		0.9		3.8	
$t_{FALL/RISE}$ $V_{ERC} = V_{CC}$	Transition Time, B outputs (0.6V to 1.3V)		0.7/0.7	2.0/2.5		ns
$t_{FALL/RISE}$ $V_{ERC} = V_{CC}$	Transition Time, B outputs (0.6V to 1.3V)		0.7/0.7	1.5/2.0		ns

Note 19: All Typical values are at V_{CC} = 3.3V and T_A = 25°C.

Extended Electrical Characteristics (GTL)

Over recommended ranges of supply voltage and operating free-air temperature V_{REF} = 0.8V (unless otherwise noted).
C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 20)	Max	Unit
t_{OSLH} (Note 21)	A	B		0.4	1.0	ns
t_{OSHL} (Note 21)				0.4	1.0	ns
$t_{PV(HL)}$ (Note 22) (Note 23)	A	B			1.5	ns
t_{OSLH} (Note 21)	CLKAB	B		0.3	0.9	ns
t_{OSHL} (Note 21)				0.3	0.6	ns
$t_{PV(HL)}$ (Note 22)(Note 23)	CLKAB	B			1.2	ns
t_{OSLH} (Note 21)	B	A		0.3	1.0	ns
t_{OSHL} (Note 21)				0.3	1.0	ns
t_{OST} (Note 21)	B	A		0.6	1.5	ns
t_{PV} (Note 22)	B	A			1.6	ns
t_{OSLH}(Note 21)	CLKAB	A		0.3	0.6	ns
t_{OSHL} (Note 21)				0.3	0.6	ns
t_{OST}(Note 21)	CLKAB	A		0.5	1.0	ns
t_{PV} (Note 22)	CLKAB	A			1.1	ns

Note 20: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

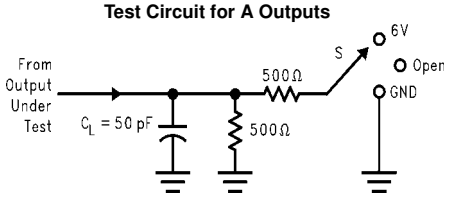
Note 21: t_{OSHL}/t_{OSLH} and t_{OST}—Output to output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs within the same packaged device. The specifications are given for specific worst case V_{CC} and temperature and apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTL outputs could vary on the backplane due to the loading and impedance seen by the device.

Note 22: t_{PV}—Part to part skew is defined as the absolute value of the difference between the actual propagation delay for all outputs from device to device. The parameter is specified for a specific worst case V_{CC} and temperature. This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTL outputs could vary on the backplane due to the loading and impedance seen by the device.

Note 23: Due to the open drain structure on GTL outputs, t_{OST} and $t_{PV(LH)}$ in the A-to-B direction are not specified. Skew on these paths is dependent on the V_{TT} and R_T values on the backplane.

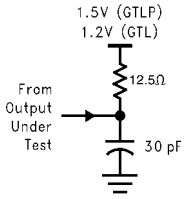
Test Circuits and Timing Waveforms

Test Circuit for A Outputs



Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

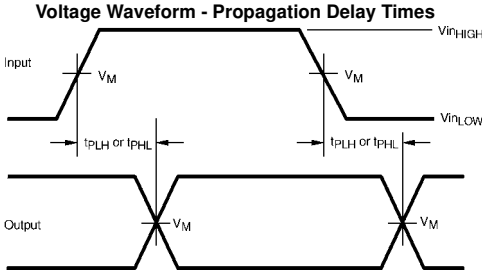
Test Circuit for B Outputs



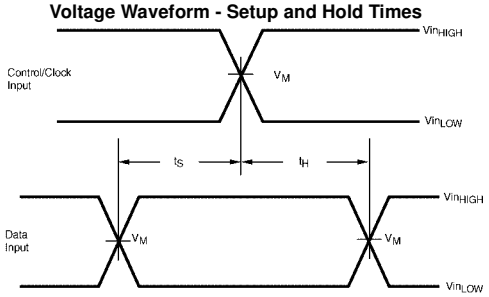
Note A: C_L includes probes and Jig capacitance.

Note B: For B Port, C_L = 30 pF is used fort worst case.

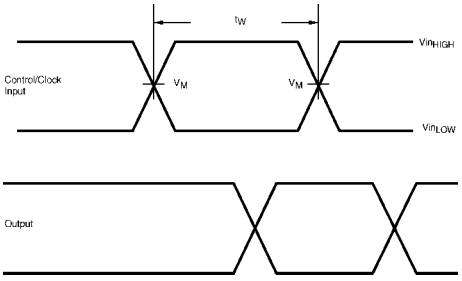
Voltage Waveform - Propagation Delay Times



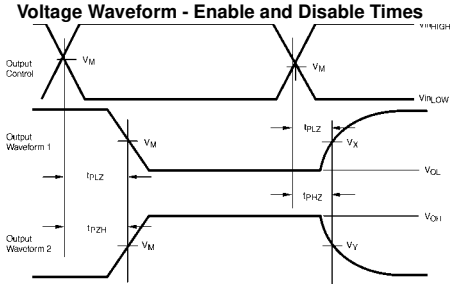
Voltage Waveform - Setup and Hold Times



Voltage Waveform - Pulse Width



Voltage Waveform - Enable and Disable Times



Output Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the control output

Output Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the control output

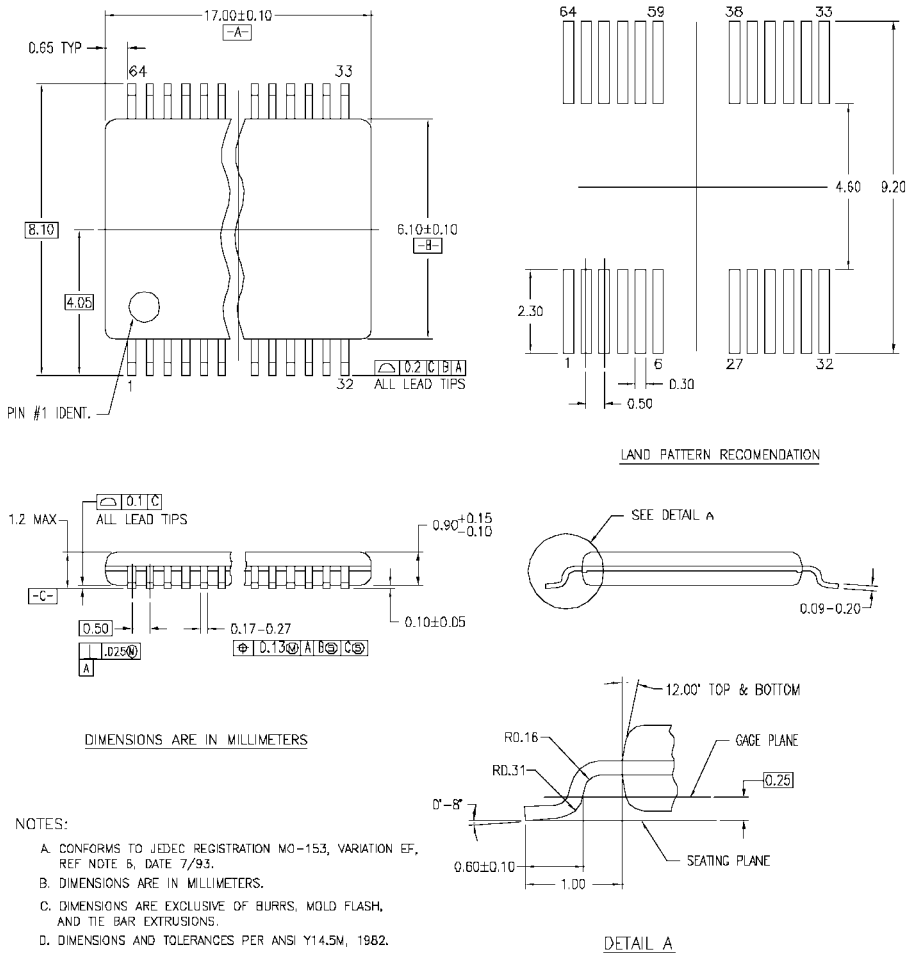
Input and Measure Conditions

	A or LVTTL Pins	B or GTLP Pins
V_{inHIGH}	3.0	1.5
V_{inLOW}	0.0	0.0
V_M	1.5	1.0
V_X	V_{OL} + 0.3V	N/A
V_Y	V_{OH} − 0.3V	N/A

All input pulses have the following characteristics: Frequency = 10MHz, $t_{RISE} = t_{FALL}$ = 2 ns, Z_O = 50Ω

The outputs are measured one at a time with one transition per measurement

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION EF, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD64REVB

64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD64

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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