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GV7600

Aviia™ Transmitter

Key Features

- Serial digital video transmitter for standard and high definition component video:
  - SD 525i and 625i
  - HD 720p 24, 25, 30, 50 and 60
  - HD 1080i 50, 60
  - HD 1080p 24, 25, 30, 50 and 60
- Supports 8-bit, 10-bit or 12-bit component digital video:
  - RGB or YCbCr 4:4:4 sampled
  - YCbCr 4:2:2 or 4:2:0 sampled
- Single 75Ω coaxial cable driver output
- Integrated audio embedder for the carriage of up to 8 channels of 48kHz digital audio
- Asynchronous Serial Interface (ASI) for transmission of IEC 13818-1 compliant transport streams
- Ancillary (ANC) data insertion
- User selectable processing features, including:
  - Timing Reference Signal (TRS) insertion
  - Programmable ANC data insertion
  - Illegal video code word re-mapping
- 4-wire Gennum Serial Peripheral Interface (GSPI) for external host command and control
- Dedicated JTAG test interface
- 1.2V core and 3.3V analog voltage power supplies
- 1.8V or 3.3V selectable digital I/O power supply
- Small footprint 100-BGA (11mm x 11mm)
- Low power operation, typically 400mW
- Pb-free and RoHS compliant

Applications

- Industrial & professional cameras
- Digital video recorders (DVR)
- Video servers
- Video mixers and switchers
- Camcorders

Description

The GV7600 is a serial digital video transmitter for standard and high definition component video. With integrated cable driving technology, the GV7600 is capable of transmitting digital video at 270Mb/s, 1.485Gb/s and 2.97Gb/s over 75Ω coaxial cable. The device provides a complete transmit solution for the transmission of both interlaced and progressive component digital video, up to 1920 x 1080, in coaxial cable-based video systems.

Using the GV7600 with the complete Aviia transmitter reference design, it is possible to implement an all-digital, bi-directional multimedia interface over coax. This interface allows both DC power and a bi-directional, half-duplex, auxiliary data interface, up to 1Mb/s, to be carried over the same single, robust and cost effective coaxial cable as the high-speed serial digital video.

The GV7600 includes a broad range of user-selectable processing features, such as Timing Reference Signal (TRS) insertion, illegal code word re-mapping, and ancillary data packet insertion. The content of ancillary data packets can be programmed via the host interface. Device configuration and status reporting is accomplished via the Gennum Serial Peripheral Interface (GSPI). Alternatively, many processing features and operational modes can be configured directly through external pin settings.

The device supports both 8-bit, 10-bit and 12-bit video data input, for RGB or YCbCr 4:4:4, and YCbCr 4:2:2 or 4:2:0. A configurable 20-bit wide parallel digital video input bus is provided, with associated pixel clock and timing signal inputs. The GV7600 supports direct interfacing of ITU-R BT.656 SD formats, and HD formats conforming to ITU-R BT.709 and BT.1120-6 for 1125-line formats, and SMPTE 296M for 750-line formats. The device may also be configured to accepts CEA-861 timing.

The GV7600 audio embedding function allows the carriage of up to 8 channels of serial digital audio within the ancillary data space of the video data stream. The input audio signal formats supported by the device include AES/EBU for professional applications, S/PDIF, and I^2S. 16-bit, 20-bit and 24-bit audio formats are supported at

48kHz synchronous-to-video for SD video formats and 48kHz synchronous or asynchronous for HD formats. Additional audio processing features include: individual channel enabling, audio group selection, group replacement, channel swapping and audio channel status insertion.

The GV7600 supports an Asynchronous Serial Interface (ASI), to carry compressed audio and video transport streams, conforming to IEC 13818-1, at 270Mb/s. Transport stream data is input to the device at a synchronous 27MHz clock rate. The device will automatically 8b/10b encode the data, prior to serialization.

Packaged in a space saving 100-BGA, the GV7600 is ideal for designs where high-density component placement is required. Typically requiring only 400mW power, the device can be used as a high bandwidth alternative to analog composite or component video interfaces, providing a high quality, all-digital, long reach video transmit solution.

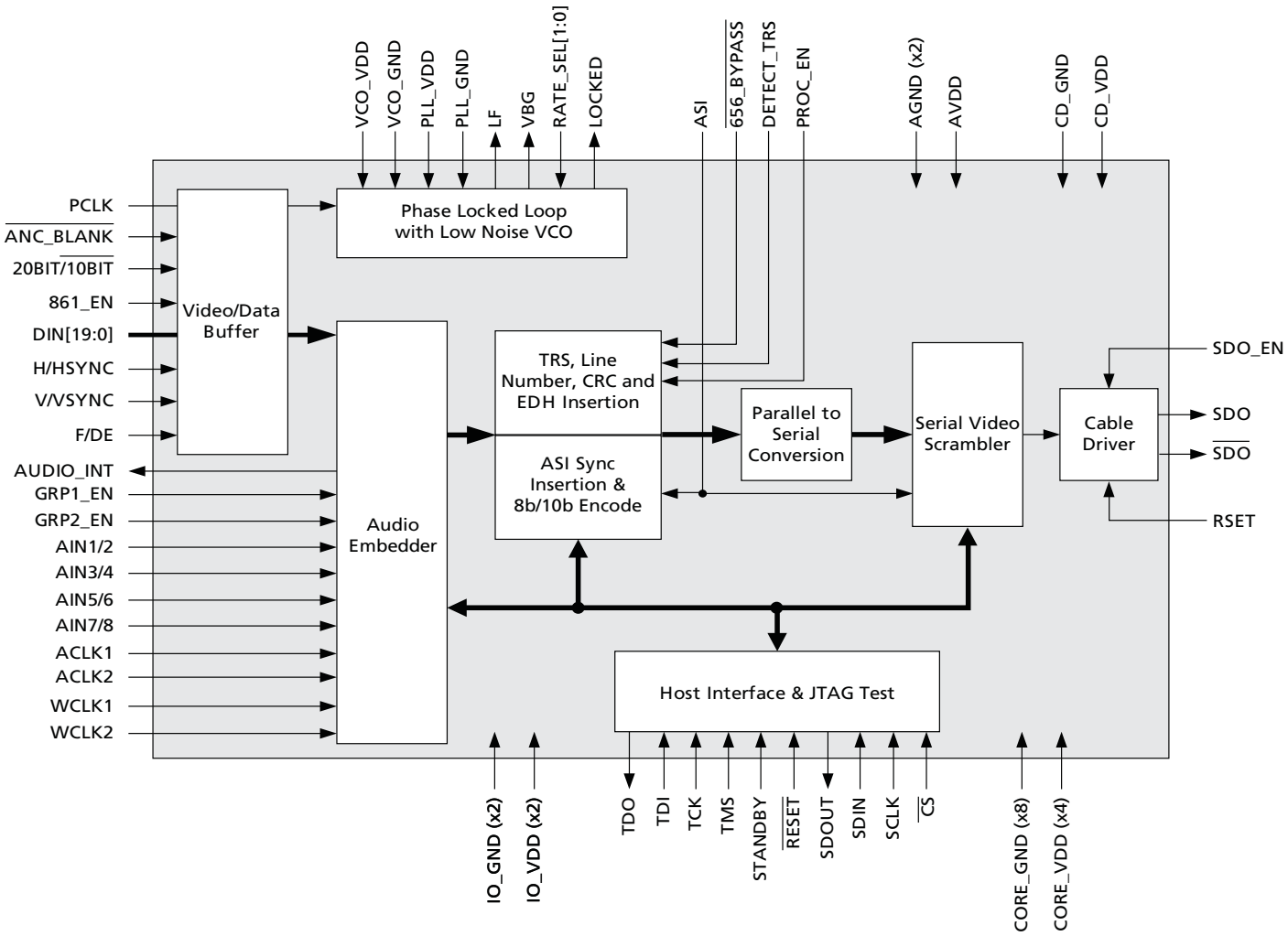

Figure A: GV7600 Functional Block Diagram

Revision History

Version	ECR	Date	Changes and / or Modifications
8	019059	April 2014	Updated Figure 6-1: GV7600 Package Dimensions
7	153723	March 2010	Changes to addresses 040h -> 13Fh in Table 4-29: Video Core Configuration and Status Registers.
6	153582	February 2010	Added analog input absolute maximum ratings to Table 2-1: Absolute Maximum Ratings.
5	152573	September 2009	Changed Reset Pulse Width from 10ms to 1ms.
4	152157	June 2009	Changed Figure 4-54 and 6.3 Marking Diagram.
3	151832	May 2009	Re-ordered the DIN[19:10] & DIN[9:0] in Table 1-1 to reflect the pin names. Added Device Latency in Table 2-4. Changed description in Section 4.7.2. Changed Figure 4-47. Changed descriptions to address 40Bh in Table 4-30 & address 80Ah in Table 4-31.
2	151644	April 2009	Changed 4.8.1 Ancillary Data Insertion Operating Modes and their registers.
1	151321	February 2009	Altered Parallel Video Data Inputs DIN[9:0] & DIN[9:0] section. Changed table in Full HD Input Formats section. Added Aviia 20-bit Mapping Structure for 1280x720 100/120Hz Progressive 4:2:2 ($Y'C'_BC'_R$) 8/10-bit Signals. Added section: Video Format & Bandwidth Requirements. Changed/Added to H:V:F Timing diagrams. Added GSPI timing delay values. Added Index.
0	150962	December 2008	New document.

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	DIN17	DIN18	F/DE	H/ HSYNC	CORE_ VDD	PLL_ VDD	LF	VBG	RSV	AVDD
B	DIN15	DIN16	DIN19	PCLK	CORE_ GND	PLL_ VDD	VCO_ VDD	VCO_ GND	AGND	AGND
C	DIN13	DIN14	DIN12	V/ VSYNC	CORE_ GND	PLL_ GND	PLL_ GND	PLL_ GND	CD_ GND	SDO
D	DIN11	DIN10	STAND BY	SDO_ EN	RSV	RSV	RSV	RSV	CD_ GND	$\overline{\text{SDO}}$
E	CORE_ VDD	CORE_ GND	RATE_ SEL0	RATE_ SEL1	CORE_ GND	CORE_ GND	TDI	TMS	CD_ GND	CD_ VDD
F	DIN9	DIN8	DETECT _TRS	RSV	CORE_ GND	CORE_ GND	RSV	TDO	CD_ GND	RSET
G	IO_VDD	IO_GND	861_EN	$\overline{\text{20BIT}}$/ 10BIT	ASI	$\overline{\text{656\_BYPASS}}$	PROC _EN	$\overline{\text{RESET}}$	CORE_ GND	CORE_ VDD
H	DIN7	DIN6	$\overline{\text{ANC\_BLANK}}$	LOCKED	GRP2_ EN	GRP1_ EN	AUDIO _INT	RSV	IO_ GND	IO_ VDD
J	DIN5	DIN4	DIN1	AIN5/6	WCLK2	AIN1/2	WCLK1	TCK	SDOUT	SCLK
K	DIN3	DIN2	DIN0	AIN7/8	ACLK2	AIN3/4	ACLK1	CORE_ VDD	$\overline{\text{CS}}$	SDIN

Figure 1-1: GV7600 Pin Assignment

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description	
B3, A2, A1, B2, B1, C2, C1, C3, D1, D2	DIN[19:10]		Input	PARALLEL DATA BUS Signal levels are LVCMOS / LVTTL compatible.	
				20-bit mode 20BIT/$\overline{10BIT}$ = HIGH	Data Stream 1/Luma data input in video mode ($\overline{656\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{656\_BYPASS}$ = LOW)
				10-bit mode 20BIT/$\overline{10BIT}$ = LOW	Multiplexed Data Stream 1/Luma and Data Stream 2/Chroma data input in video mode ($\overline{656\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{656\_BYPASS}$ = LOW) Transport stream data input in ASI mode ($\overline{656\_BYPASS}$ = LOW) (ASI = HIGH)
A3	F/DE	Synchronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. 861_EN = LOW: Used to indicate the ODD / EVEN field of the video signal when DETECT_TRS is set LOW. The device sets the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH (PROC_EN must also be HIGH). The F signal should be set HIGH for the entire period of field 2 and should be set LOW for all lines in field 1 and for all lines in progressive scan systems. The F signal is ignored when DETECT_TRS = HIGH. 861_EN = HIGH: The DE signal is used to indicate the active video period when DETECT_TRS is LOW. DE is HIGH for active data and LOW for blanking. See Section 4.3.1 and Section 4.3.2 for timing details. The DE signal is ignored when DETECT_TRS = HIGH.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A4	H/HSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. 861_EN is LOW: The H signal is used to indicate the portion of the video line containing active video data, when DETECT_TRS is set LOW. Active Line Blanking The H signal should be LOW for the active portion of the video line. The signal goes LOW at the first active pixel of the line, and then goes HIGH after the last active pixel of the line. The H signal should be set HIGH for the entire horizontal blanking period, including both EAV and SAV TRS words, and LOW otherwise. TRS Based Blanking (H_CONFIG = 1_h) The H signal should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise. 861_EN = HIGH: The HSYNC signal indicates horizontal timing. See Section 4.3.1. When DETECT_TRS is HIGH, this pin is ignored at all times. If DETECT_TRS is set HIGH and 861_EN is set HIGH, the DETECT_TRS feature takes priority.
A5, E1, G10, K8	CORE_VDD		Input Power	Power supply connection for digital core logic. Connect to 1.2V DC digital.
A6, B6	PLL_VDD		Input Power	Power supply pin for PLL. Connect to 1.2V DC analog.
A7	LF		Analog Output	Loop Filter component connection.
A8	VBG		Output	Bandgap voltage filter connection.
A9, D6, D7, D8, F4	RSV		–	These pins are reserved and should be left unconnected.
A10	AVDD		Input Power	VDD for sensitive analog circuitry. Connect to 3.3VDC analog.
B4	PCLK		Input	PARALLEL DATA BUS CLOCK. Signal levels are LVCMOS / LVTTL compatible. Full HD 20-bit mode: PCLK @ 148.5MHz Full HD 10-bit mode DDR: PCLK @ 148.5MHz HD 20-bit mode: PCLK @ 74.25MHz HD 10-bit mode: PCLK @ 148.5MHz SD 20-bit mode: PCLK @ 13.5MHz SD 10-bit mode: PCLK @ 27MHz ASI mode: PCLK @ 27MHz

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
B5, C5, E2, E5, E6, F5, F6, G9	CORE_GND		Input Power	GND connection for digital logic. Connect to digital GND.
B7	VCO_VDD		Input Power	Power pin for VCO. Connect to 1.2V DC analog followed by an RC filter. VCO_VDD is nominally 0.7V.
B8	VCO_GND		Input Power	Ground connection for VCO. Connect to analog GND.
B9, B10	AGND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
C4	V/VSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. 861_EN = LOW: The V signal is used to indicate the portion of the video field/frame that is used for vertical blanking, when DETECT_TRS is set LOW. The V signal should be set HIGH for the entire vertical blanking period and should be set LOW for all lines outside of the vertical blanking interval. The V signal is ignored when DETECT_TRS = HIGH. 861_EN = HIGH: The VSYNC signal indicates vertical timing. See 4.9.2 Ancillary Data Blanking for timing details. The VSYNC signal is ignored when DETECT_TRS = HIGH.
C6, C7, C8	PLL_GND		Input Power	Ground connection for PLL. Connect to analog GND.
C9, D9, E9, F9	CD_GND		Input Power	Ground connection for the serial digital cable driver. Connect to analog GND.
C10, D10	SDO, $\overline{\text{SDO}}$		Output	Serial Data Output Signal. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485 /1.001Gb/s or 270Mb/s. The slew rate of the output is automatically controlled according to the setting of the RATE_SEL0 and RATE_SEL1 pins.
D3	STANDBY		Input	Power Down input. HIGH to power down device.
D4	SDO_EN		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to enable or disable the serial digital output stage. When SDO_EN is LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When SDO_EN is HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled.
D5, F7, H8	RSV		–	These pins are reserved and should be connected to CORE_GND.

Table 1-1: Pin Descriptions (Continued)

<table>
<tr><th>Pin Number</th><th>Name</th><th>Timing</th><th>Type</th><th>Description</th></tr>
<tr><td>E3, E4</td><td>RATE_SEL0,
RATE_SEL1</td><td></td><td>Input</td><td>CONTROL SIGNAL INPUT.
Signal levels are LVCMOS/LVTTL compatible.
Used to configure the operating data rate.
<table><tr><th>RATE_SEL0</th><th>RATE_SEL1</th><th>Data Rate</th></tr><tr><td>0</td><td>0</td><td>1.485 or 1.485/1.001Gb/s</td></tr><tr><td>0</td><td>1</td><td>2.97 or 2.97/1.001Gb/s</td></tr><tr><td>1</td><td>X</td><td>270Mb/s</td></tr></table></td></tr>
<tr><td>E7</td><td>TDI</td><td></td><td>Input</td><td>COMMUNICATION SIGNAL INPUT.
Signal levels are LVCMOS/LVTTL compatible.
Dedicated JTAG pin.
Test data in.
This pin is used to shift JTAG test data into the device.</td></tr>
<tr><td>E8</td><td>TMS</td><td></td><td>Input</td><td>COMMUNICATION SIGNAL INPUT.
Signal levels are LVCMOS/LVTTL compatible.
Dedicated JTAG pin.
Test mode start.
This pin is JTAG Test Mode Start. It is used to control the operation of the JTAG test.</td></tr>
<tr><td>E10</td><td>CD_VDD</td><td></td><td>Input Power</td><td>Power for the serial digital cable driver. Connect to 3.3V DC analog.</td></tr>
<tr><td>F1, F2, H1, H2, J1, J2, K1, K2, J3, K3</td><td>DIN[9:0]</td><td></td><td>Input</td><td>PARALLEL DATA BUS.
Signal levels are LVCMOS / LVTTL compatible.
<table><tr><td>20-bit mode
20BIT/$\overline{10BIT}$ = HIGH</td><td>DS2/Chroma data input in video mode
$\overline{656\_BYPASS}$ = HIGH
ASI = LOW
Data input in data through mode
$\overline{656\_BYPASS}$ = LOW
ASI = LOW
Not Used in ASI mode
$\overline{656\_BYPASS}$ = LOW
ASI = HIGH</td></tr><tr><td>10-bit mode
20BIT/$\overline{10BIT}$ = LOW</td><td>High impedance.</td></tr></table></td></tr>
<tr><td>F3</td><td>DETECT_TRS</td><td></td><td>Input</td><td>CONTROL SIGNAL INPUT.
Signal levels are LVCMOS / LVTTL compatible.
Used to select external HVF timing mode or TRS extraction timing mode.
When DETECT_TRS is LOW, the device extracts all internal timing from the supplied H:V:F or CEA-861 timing signals, dependent on the status of the 861_EN pin.
When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.</td></tr>
</table>

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
F8	TDO		Output	COMMUNICATION SIGNAL OUTPUT. Signal levels are LVCMOS/LVTTL compatible. Dedicated JTAG pin. JTAG Test Data Output. This pin is used to shift results from the device.
F10	RSET		Input	An external 1% resistor connected to this input is used to set the SDO/$\overline{\text{SDO}}$ output signal amplitude.
G1, H10	IO_VDD		Input Power	Power connection for digital I/O. Connect to 3.3V or 1.8V DC digital.
G2, H9	IO_GND		Input Power	Ground connection for digital I/O. Connect to digital GND.
G3	861_EN		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to select external CEA-861 timing mode. When DETECT_TRS is LOW and 861_EN is LOW, the device extracts all internal timing from the supplied H:V:F timing signals. When DETECT_TRS is LOW and 861_EN is HIGH, the device extracts all internal timing from the supplied HSYNC, VSYNC, DE timing signals. When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.
G4	20BIT/$\overline{\text{10BIT}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to select the input bus width.
G5	ASI		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable the ASI data transmission. When ASI is set HIGH and $\overline{\text{656\_BYPASS}}$ is set LOW, the device carries out ASI word alignment, I/O processing and transmission. When $\overline{\text{656\_BYPASS}}$ and ASI are both set LOW, the device operates in data-through mode.
G6	$\overline{\text{656\_BYPASS}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to enable / disable all forms of encoding / decoding, scrambling and EDH insertion. When set LOW, the device operates in data through mode (ASI= LOW), or in ASI mode (ASI = HIGH). No video data scrambling takes place and none of the I/O processing features of the device are available when $\overline{\text{656\_BYPASS}}$ is set LOW. When set HIGH, the device carries out video data scrambling and I/O processing.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G7	PROC_EN		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the I/O processing features. When PROC_EN is HIGH, the I/O processing features of the device are enabled. When PROC_EN is LOW, the I/O processing features of the device are disabled. Only applicable in video mode.
G8	$\overline{\text{RESET}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings.
H3	$\overline{\text{ANC\_BLANK}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. When $\overline{\text{ANC\_BLANK}}$ is LOW, the Luma and Chroma input data is set to the appropriate blanking levels during the H and V blanking intervals. When $\overline{\text{ANC\_BLANK}}$ is HIGH, the Luma and Chroma data pass through the device unaltered. Only applicable in video mode.
H4	LOCKED		Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. PLL lock indication. HIGH indicates PLL is locked. LOW indicates PLL is not locked.
H5	GRP2_EN		Input	Enable Input for audio channels 5-8. Set HIGH to enable.
H6	GRP1_EN		Input	Enable Input for audio channels 1-4. Set HIGH to enable.
H7	AUDIO_INT		Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. Summary Interrupt from Audio Processing. This signal is set HIGH by the device to indicate a problem with the audio processing, which requires the Host processor to interrogate the interrupt status registers. IO_VDD = 3.3V Drive Strength = 8mA IO_VDD = 1.8V Drive Strength = 4mA **Note**: By default, out of reset, the AUDIO_INT pin outputs the HD_AUDIO_CLOCK, rather than the audio interrupt signal. In order to output the interrupt flags from the audio core as intended, the user must write 0001h to register 0232h.
J4	AIN5/6		Input	Serial Audio Input; Channels 5 and 6.
J5	WCLK2		Input	48kHz Word clock for Channels 5-8.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
J6	AIN1/2		Input	Serial Audio Input; Channels 1 and 2.
J7	WCLK1		Input	48kHz Word clock for Channels 1-4.
J8	TCK		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. JTAG Serial Data Clock Signal. This pin is the JTAG clock.
J9	SDOUT		Output	COMMUNICATION SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. Serial Data Output. This pin operates as the host interface serial output, used to read status and configuration information from the internal registers of the device. IO_VDD = 3.3V Drive Strength = 12mA IO_VDD = 1.8V Drive Strength = 4mA
J10	SCLK		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Serial data clock signal. SCLK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. **Note**: If the host interface is not being used, tie this pin HIGH.
K4	AIN7/8		Input	Serial Audio Input; Channels 7 and 8.
K5	ACLK2		Input	64 x WCLK for Channels 5-8.
K6	AIN3/4		Input	Serial Audio Input; Channels 3 and 4.
K7	ACLK1		Input	64 x WCLK for Channels 1-4.
K9	$\overline{CS}$		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Chip select. $\overline{CS}$ operates as the host interface Chip Select, and is active LOW.
K10	SDIN		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Serial data in. This pin is used to write address and configuration data words into the device.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +3.6V
Supply Voltage, Analog 1.2V (PLL_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (CD_VDD, AVDD)	-0.3V to +3.6V
Input Voltage Range (RSET)	-0.3V to (CD_VDD + 0.3)V
Input Voltage Range (VBG)	-0.3V to (AVDD + 0.3)V
Input Voltage Range (LF)	-0.3V to (PLL_VDD + 0.3)V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Ambient Operating Temperature (T_A)	$-40°C \leq T_A \leq 95°C$
Storage Temperature (T_{STG})	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

Notes:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–

Table 2-2: Recommended Operating Conditions (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	AVDD	–	3.13	3.3	3.47	V	–
Supply Voltage, CD	CD_VDD	–	3.13	3.3	3.47	V	–

Notes:

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10-bit Full HD	–	135	200	mA	–
		20-bit Full HD	–	135	200	mA	–
		10/20-bit HD	–	100	160	mA	–
		10/20-bit SD	–	75	120	mA	–
		ASI	–	75	120	mA	–
+1.8V Supply Current	I_{1V8}	10-bit Full HD	–	15	30	mA	–
		20-bit Full HD	–	15	32	mA	–
		10/20-bit HD	–	15	32	mA	–
		10/20-bit SD	–	3	10	mA	–
		ASI	–	3	10	mA	–
+3.3V Supply Current	I_{3V3}	10-bit Full HD	–	90	110	mA	–
		20-bit Full HD	–	90	110	mA	–
		10/20-bit HD	–	90	110	mA	–
		10/20-bit SD	–	70	90	mA	–
		ASI	–	70	90	mA	–
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10-bit Full HD	–	400	560	mW	–
		20-bit Full HD	–	400	560	mW	–
		10/20-bit HD	–	350	510	mW	–
		10/20-bit SD	–	300	450	mW	–
		ASI	–	300	450	mW	–
		Reset	–	200	–	mW	–
		Standby	–	110	150	mW	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10-bit Full HD	–	430	600	mW	–
		20-bit Full HD	–	450	610	mW	–
		10/20-bit HD	–	420	550	mW	–
		10/20-bit SD	–	320	450	mW	–
		ASI	–	320	450	mW	–
		Reset	–	230	–	mW	–
		Standby	–	110	150	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_GND - 0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD + 0.3	V	–
Output Logic LOW	V_{OL}	IOL=5mA, 1.8V operation	–	–	0.2	V	–
		IOL=8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOL=5mA, 1.8V operation	1.4	–	–	V	–
		IOL=8mA, 3.3V operation	2.4	–	–	V	–
Serial Output							
Serial Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET = 750Ω SD and HD mode	–	CD_VDD - $\Delta V_{SDO}/2$	–	V	–

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Reset Pulse Width	t_{reset}	–	1	–	–	ms	–
Device Latency							
Full HD Bypass Mode		PCLK = 148.5MHz	–	54	–	PCLK	–
Full HD Video Mode		PCLK = 148.5MHz (no audio)	–	95	–	PCLK	–
Full HD Video Mode		PCLK = 148.5MHz (with audio)	–	1106	–	PCLK	–
HD Bypass Mode		PCLK = 74.25MHz	–	54	–	PCLK	–
HD Video Mode		PCLK = 74.25MHz (no audio)	–	95	–	PCLK	–
HD Video Mode		PCLK = 74.25MHz (with audio)	–	1106	–	PCLK	–
SD Bypass Mode		PCLK = 27MHz	–	54	–	PCLK	–
SD Video Mode		PCLK = 27MHz (no audio)	–	112			
SD Video Mode		PCLK = 27MHz (with audio)	–	638	–	PCLK	–
ASI Mode		PCLK = 27MHz	–	52	–	PCLK	–
Parallel Input							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Input Data Setup Time	t_{su}	50% levels; 3.3V or 1.8V operation	1.2	–	–	ns	1
Input Data Hold Time	t_{ih}		0.8	–	–	ns	1
Serial Audio Data Input							
Input Data Set-up Time	t_{su}	50% levels; 3.3V or 1.8V operation	74	–	–	ns	–
Input Data Hold Time	t_{ih}		74	–	–	ns	–
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	–	2.97	–	Gb/s	–
		–	–	2.97/1.001	–	Gb/s	–
		–	–	1.485	–	Gb/s	–
		–	–	1.485/1.001	–	Gb/s	–
		–	–	270	–	Mb/s	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Output Swing	V_{SDD}	RSET = 750Ω 75Ω load	750	800	850	mVp-p	2
Serial Output Rise/Fall Time 20% ~ 80%	trf_{SDO}	HD mode	–	120	135	ps	–
	trf_{SDO}	SD mode	400	660	800	ps	–
Mismatch in rise/fall time	$\Delta t_r, \Delta t_f$	–	–	–	35	ps	–
Duty Cycle Distortion	–	–	–	–	5	%	2
Overshoot	–	HD mode	–	5	10	%	2
	–	SD mode	–	3	8	%	2
Output Return Loss	ORL	1.485GHz - 2.97GHz	–	-12	–	dB	3
		5MHz - 1.485GHz	–	-18	–	dB	3
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and Colour Bars HD signal	–	40	68	ps	4, 5
	t_{OJ}	Pseudorandom and Colour Bars SD signal	–	50	95	ps	4, 5
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and Colour Bars SD signal	–	200	400	ps	6
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	80	MHz	–
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	–
GSPI Input Data Setup Time	–		1.5	–	–	ns	–
GSPI Input Data Hold Time	–		1.5	–	–	ns	–
GSPI Output Data Hold Time	–	15pF load	1.5	–	–	ns	–
$\overline{CS}$ low before SCLK rising edge	t_0	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	7
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	t_4	50% levels 3.3V or 1.8V operation	PCLK (MHz) / ns: unlocked 445; 13.5 74.2; 27.0 37.1; 74.25 13.5; 148.5 6.7	–	–	ns	7

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min		Typ	Max	Units	Notes
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	t_5	50% levels 3.3V or 1.8V operation	PCLK (MHz)	ns	–	–	ns	7
			unlocked	1187				
			13.5	297				
			27.0	148.4				
			74.25	53.9				
			148.5	27				
$\overline{CS}$ high after SCLK rising edge	t_7	50% levels 3.3V or 1.8V operation	PCLK (MHz)	ns	–	–	ns	7
			unlocked	445				
			13.5	74.2				
			27.0	37.1				
			74.25	13.5				
			148.5	6.7				

Notes:

1. Input setup and hold time is dependent on the rise and fall time on the parallel input. Parallel clock and data with rise time or fall time greater than 500ps require larger setup and hold times.
2. Single Ended into 75Ω external load.
3. ORL depends on board design.
4. Alignment Jitter = measured from 100kHz to serial data rate/10.
5. This is the maximum jitter for a BER 10^{-12}. The equivalent jitter value as per RP184 is 40ps max.
6. Alignment Jitter = measured from 1kHz to 27MHz.
7. For GSPI timing parameters, refer to Figure 4-52 and Figure 4-53 in Section 4.14.3, as appropriate.

3. Input/Output Circuits

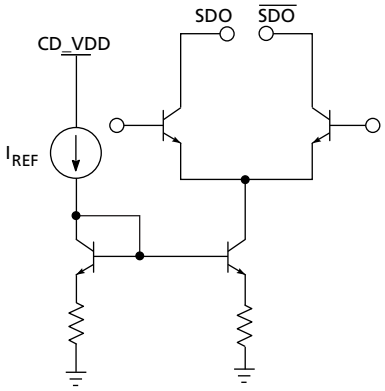

Figure 3-1: Differential Output Stage (SDO/SDO)

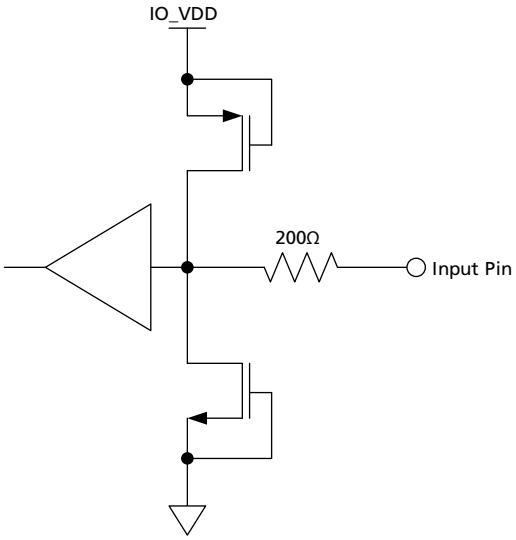

Figure 3-2: Digital Input Pin (20BIT/10BIT, ANC_BLANK, DETECT_TRS, ASI, RATE_SEL0, 656_BYPASS, RATE_SEL1, 861_EN, F/DE, H/HSYNC, PCLK, V/VSYNC)

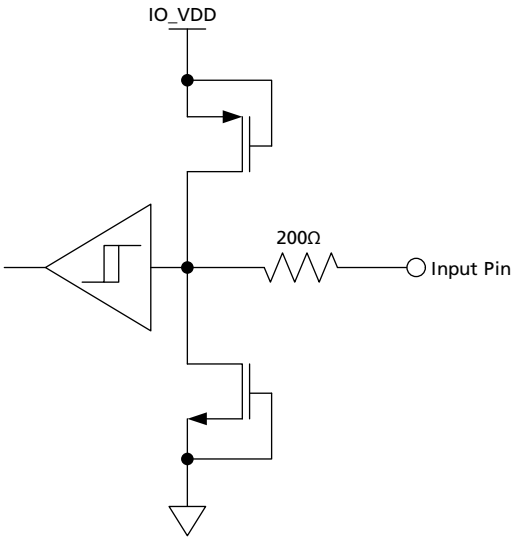

Figure 3-3: Digital Input Pin with Schmitt Trigger ($\overline{\text{RESET}}$)

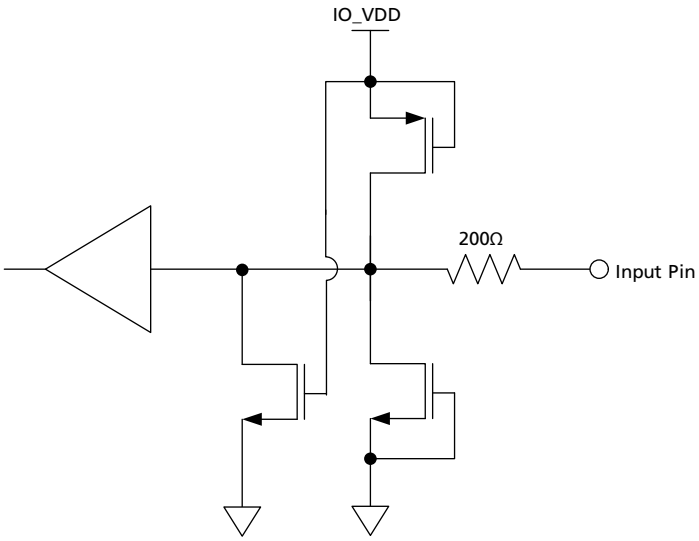

Figure 3-4: Digital Input Pin with weak pull-down - maximum pull-down current <110mA (STANDBY, SCLK, SDIN, TCK, TDI)

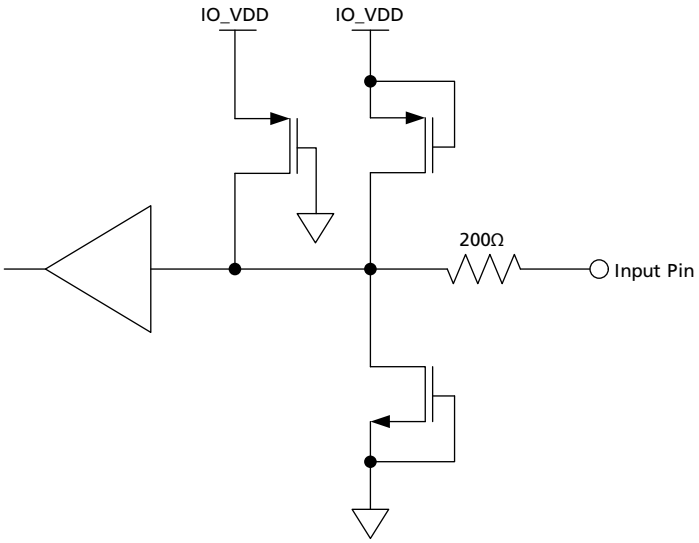

Figure 3-5: Digital Input Pin with weak pull-up - maximum pull-up current <110mA (ACLK1, ACLK2, AIN7/8, AIN5/6, AIN3/4, AIN1/2, $\overline{CS}$, GRP1_EN, GRP2_EN, PROC_EN, SDO_EN, TMS, WCLK1, WCLK2)

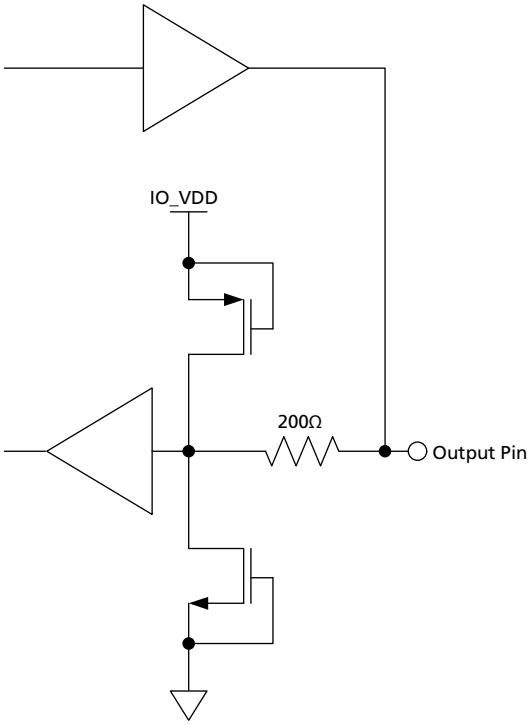

Figure 3-6: Bidirectional Digital Input/Output Pin with programmable drive strength.

These pins in Figure 3-6 are configured to input at all times except in test mode. (DIN0, DIN2, DIN3, DIN4, DIN5, DIN6, DIN7, DIN8, DIN9, DIN10, DIN11, DIN12, DIN13, DIN14, DIN15, DIN16, DIN17, DIN18, DIN19, DIN1)