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Key Features

- Serial digital video receiver for standard and high definition component video:
 - SD 525i and 625i
 - HD 720p 24, 25, 30, 50 and 60
 - HD 1080i 50, 60
 - HD 1080p 24, 25, 30, 50 and 60
- Supports 8-bit, 10-bit or 12-bit component digital video:
 - RGB or YCbCr 4:4:4 sampled
 - YCbCr 4:2:2 or 4:2:0 sampled
- Integrated cable equalizer for long reach cable performance
 - 230m typical HD performance over high-quality 75Ω coaxial cable (Belden 1694A or equivalent)
 - 160m typical HD performance over RG59 or equivalent 75Ω coaxial cable
- Serial digital loop-through output
- Integrated audio de-embedder for the extraction of up to 8 channels of 48kHz digital audio
- Supports IEC 13818-1 compliant transport streams over the Asynchronous Serial Interface (ASI)
- Automatic selection between SD/HD component video and ASI input data
- Ancillary (ANC) data detection and extraction
- User selectable processing features, including:
 - Timing Reference Signal (TRS) error detection and correction
 - ANC data checksum error detection and correction
 - Programmable ANC data detection
 - Line number and CRC error detection and correction
 - Illegal video code word re-mapping
- 4-wire Gennum Serial Peripheral Interface (GSPI) for external host command and control
- JTAG test interface
- 1.2V core and 3.3V analog voltage power supplies
- 1.8V or 3.3V selectable digital I/O power supply
- Small footprint 100-BGA (11mm x 11mm)
- Low power operation, typically 570mW at HD
- Pb-free and RoHS compliant

Applications

- Digital video recorders (DVR)
- Video servers
- Video mixers and switchers
- Image capture devices
- Video framegrabbers
- Camcorders
- Video monitors & displays

Description

The GV7601 is a serial digital video receiver for standard and high definition component video, operating at 270Mb/s, 1.485Gb/s and 2.97Gb/s data rates. With integrated cable equalizer technology, the GV7601 is capable of receiving digital video over 75Ω coaxial cable at lengths up to 460m for standard definition video, and up to 230m for high definition. This provides a complete receive solution for the transmission of both interlaced and progressive component digital video, up to 1920 x 1080, in coaxial cable-based video systems.

Using the GV7601 with the complete Aviia™ receiver reference design, it is possible to implement an all-digital, bi-directional multimedia interface over coax. This interface allows both DC power and a bi-directional, half-duplex, auxiliary data interface to be carried over the same single, robust and cost effective coaxial cable as the high-speed serial digital video. The GV7601 also provides a re-timed serial digital output for video loop-through applications.

The GV7601 includes a broad range of user-selectable processing features, such as Timing Reference Signal (TRS) error detection and extraction, illegal code word re-mapping, and ancillary data packet extraction. The content of ancillary data packets, embedded by an Aviia transmitter, can be extracted and retrieved via the host interface. Device configuration and status reporting is accomplished via the Gennum Serial Peripheral Interface (GSPI). Alternatively, many processing features and

operational modes can be configured directly through external pin settings.

The device can output both 8-bit, 10-bit and 12-bit video data, for RGB or YCbCr 4:4:4, and YCbCr 4:2:2 or 4:2:0. A configurable 20-bit wide parallel digital video output bus is provided, with associated pixel clock and timing signal outputs. The GV7601 supports ITU-R BT.656 SD formats, and HD formats conforming to ITU-R BT.709 and BT.1120-6 for 1125-line formats, and SMPTE 296M for 750-line formats. The device may also be configured to output CEA-861 timing.

The GV7601 audio de-embedding function allows the up to 8 channels of serial digital audio within the ancillary data space of the video data stream to be extracted. The audio output signal formats supported by the device include AES/EBU for professional applications, S/PDIF, and I²S. 16-bit, 20-bit and 24-bit audio formats are supported at 48kHz synchronous-to-video for SD video formats and

48kHz synchronous or asynchronous for HD formats. Additional audio processing features include: individual channel extraction, audio group selection, group replacement, channel swapping and audio channel status extraction.

The GV7601 also supports an Asynchronous Serial Interface (ASI) 270Mb/s input, carrying compressed audio and video transport streams, conforming to IEC 13818-1. Transport stream data is output from the device at a synchronous 27MHz clock rate. The device will automatically deserialize and 8b/10b decode the data.

Packaged in a space saving 100-BGA, the GV7601 is ideal for designs where high-density component placement is required. Typically requiring only 570mW power, the device can be used as a high bandwidth alternative to analog composite or component video interfaces, providing a high quality, all-digital, long reach video receive solution.

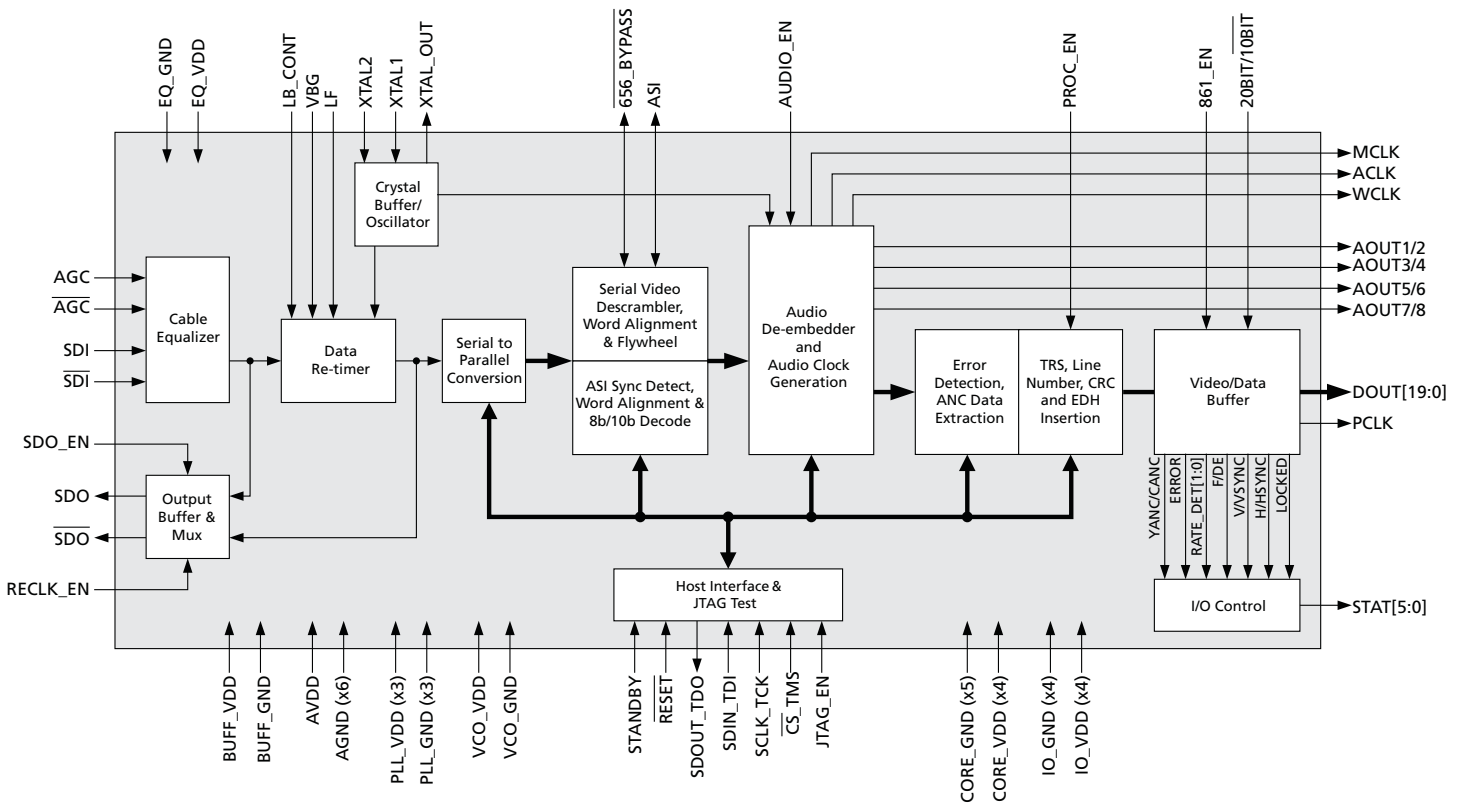


Figure A: GV7601 Block Diagram

Revision History

Version	ECR	Date	Changes and / or Modifications
7	019059	April 2014	Updated Figure 6-1: GV7601 Package Dimensions .
6	158071	May 2012	Changed VIL and VIH (Min and Max) in Table 2-3: DC Electrical Characteristics .
5	153582	February 2010	Added analog input absolute maximum ratings to Table 2-1: Absolute Maximum Ratings . Updated device latency values in Table 2-4: AC Electrical Characteristics .
4	152345	August 2009	Modified Key Features , Description , Table 2-3 , Table 2-4 and Table 4-1 .
3	152159	June 2009	Modified Section 4.11.1.1 , Section 4.12 , Section 4.17.4 , Section 4.19 , and Table 4-33 . Added Figure 4-64 . Changed 6.3 Marking Diagram .
2	151833	May 2009	Re-ordered the DOUT[19:10] & DOUT[9:0] in Table 1-1 to reflect the pin names. Changed Figure 4-41 .
1	151651	April 2009	Changed DOUT[18_10] and DOUT[9:0] pin descriptions. Changed 4.16.8 Ancillary Data Extraction and its registers.
0	151484	February 2009	New document.

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	AVDD	PLL_VDD	RSV	VCO_GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	AGND	PLL_VDD	PLL_VDD	STAT4	STAT5	$\overline{\text{RESET}}$	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	AGND	AGND	PLL_GND	CORE_GND	CORE_VDD	RSV	JTAG_EN	IO_GND	IO_VDD
E	EQ_VDD	EQ_GND	AGND	PLL_GND	CORE_GND	CORE_VDD	SDOUT_TDO	SDIN_TDI	DOUT10	DOUT11
F	AGC	RSV	AGND	PLL_GND	CORE_GND	CORE_VDD	$\overline{\text{CS}}$ _TMS	SCLK_TCK	DOUT8	DOUT9
G	$\overline{\text{AGC}}$	AGND	RECLK_EN	CORE_GND	CORE_GND	CORE_VDD	$\overline{\text{656}}$ _BYPASS	ASI	IO_GND	IO_VDD
H	BUFF_VDD	BUFF_GND	AUDIO_EN	WCLK	861_EN	XTAL_OUT	20BIT/10BIT	PROC_EN	DOUT6	DOUT7
J	SDO	SDO_EN	AOUT1/2	ACLK	AOUT5/6	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STANDBY	AOUT3/4	MCLK	AOUT7/8	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
A1	VBG	Analog Input	Band Gap voltage filter connection.
A2	LF	Analog Input	Loop Filter component connection.
A3	LB_CONT	Analog Input	Connection for loop bandwidth control resistor.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description																												
A4	VCO_VDD	Input Power	POWER pin for the VCO. Connect to 1.2V DC analog through an RC filter (see 5. References & Relevant Standards). VCO_VDD is nominally 0.7V (Do not connect directly to 0.7V).																												
A5, A6, B5, B6, C5, C6	STAT[0:5]	Output	<p>MULTI-FUNCTIONAL OUTPUT PORT. Signal levels are LVCMOS/LVTTL compatible. Each of the STAT[5:0] pins can be configured individually to output one of the following signals:</p> <table border="1"> <thead> <tr> <th>Signal</th> <th>Default</th> </tr> </thead> <tbody> <tr> <td>H/HSYNC</td> <td>STAT0</td> </tr> <tr> <td>V/VSYNC</td> <td>STAT1</td> </tr> <tr> <td>F/DE</td> <td>STAT2</td> </tr> <tr> <td>LOCKED</td> <td>STAT3</td> </tr> <tr> <td>Y/1ANC</td> <td>STAT4</td> </tr> <tr> <td>C/2ANC</td> <td>–</td> </tr> <tr> <td>$\overline{\text{DATA_ERROR}}$</td> <td>STAT5</td> </tr> <tr> <td>$\overline{\text{VIDEO_ERROR}}$</td> <td>–</td> </tr> <tr> <td>$\overline{\text{AUDIO_ERROR}}$</td> <td>–</td> </tr> <tr> <td>EDH_DETECTED</td> <td>–</td> </tr> <tr> <td>CARRIER_DETECT</td> <td>–</td> </tr> <tr> <td>RATE_DETO</td> <td>–</td> </tr> <tr> <td>RATE_DET1</td> <td>–</td> </tr> </tbody> </table>	Signal	Default	H/HSYNC	STAT0	V/VSYNC	STAT1	F/DE	STAT2	LOCKED	STAT3	Y/1ANC	STAT4	C/2ANC	–	$\overline{\text{DATA_ERROR}}$	STAT5	$\overline{\text{VIDEO_ERROR}}$	–	$\overline{\text{AUDIO_ERROR}}$	–	EDH_DETECTED	–	CARRIER_DETECT	–	RATE_DETO	–	RATE_DET1	–
Signal	Default																														
H/HSYNC	STAT0																														
V/VSYNC	STAT1																														
F/DE	STAT2																														
LOCKED	STAT3																														
Y/1ANC	STAT4																														
C/2ANC	–																														
$\overline{\text{DATA_ERROR}}$	STAT5																														
$\overline{\text{VIDEO_ERROR}}$	–																														
$\overline{\text{AUDIO_ERROR}}$	–																														
EDH_DETECTED	–																														
CARRIER_DETECT	–																														
RATE_DETO	–																														
RATE_DET1	–																														
A7, D10, G10, K7	IO_VDD	Input Power	POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.																												
A8	PCLK	Output	<p>PARALLEL DATA BUS CLOCK - Signal levels are LVCMOS/LVTTL compatible.</p> <table border="1"> <tbody> <tr> <td>Full HD 10-bit or 20-bit mode</td> <td>PCLK @ 148.5 or 148.5/1.001MHz</td> </tr> <tr> <td>HD 10-bit mode</td> <td>PCLK @ 148.5 or 148.5/1.001MHz</td> </tr> <tr> <td>HD 20-bit mode</td> <td>PCLK @ 74.25 or 74.25/1.001MHz</td> </tr> <tr> <td>SD 10-bit mode</td> <td>PCLK @ 27MHz</td> </tr> <tr> <td>SD 20-bit mode</td> <td>PCLK @ 13.5MHz</td> </tr> </tbody> </table>	Full HD 10-bit or 20-bit mode	PCLK @ 148.5 or 148.5/1.001MHz	HD 10-bit mode	PCLK @ 148.5 or 148.5/1.001MHz	HD 20-bit mode	PCLK @ 74.25 or 74.25/1.001MHz	SD 10-bit mode	PCLK @ 27MHz	SD 20-bit mode	PCLK @ 13.5MHz																		
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SD 10-bit mode	PCLK @ 27MHz																														
SD 20-bit mode	PCLK @ 13.5MHz																														

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
			PARALLEL DATA BUS - Signal levels are LVCMOS/LVTTL compatible.
			<p>Video mode $(\overline{656_BYPASS} = \text{HIGH and ASI} = \text{LOW})$: Luma data output for SD and HD data rates; Data Stream 1 for Full HD at 148.5MHz</p> <p>20-bit mode $20\text{BIT}/\overline{10\text{BIT}} = \text{HIGH}$</p> <p>ASI mode $(\overline{656_BYPASS} = \text{LOW and ASI} = \text{HIGH})$: Not defined</p> <p>Data-Through mode $(\overline{656_BYPASS} = \text{LOW and ASI} = \text{LOW})$: Data output</p>
B8, A9, A10, B9, B10,C9, C10, C8, E10, E9	DOUT[19:10]	Output	<p>Video mode $(\overline{656_BYPASS} = \text{HIGH and ASI} = \text{LOW})$: Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1/2 for Full HD at 148.5MHz</p> <p>10-bit mode $20\text{BIT}/\overline{10\text{BIT}} = \text{LOW}$</p> <p>ASI mode $(\overline{656_BYPASS} = \text{LOW and ASI} = \text{HIGH})$: 8b/10b decoded transport stream data</p> <p>Data-Through mode $(\overline{656_BYPASS} = \text{LOW and ASI} = \text{LOW})$: Data output</p>
			<p>Video mode $(\overline{656_BYPASS} = \text{HIGH and ASI} = \text{LOW})$: Luma data output for SD and HD data rates; Data Stream 1 for Full HD at 148.5MHz (20-bit mode)</p>
			<p>ASI mode $(\overline{656_BYPASS} = \text{LOW and ASI} = \text{HIGH})$: Transport stream output</p>
			<p>Data-Through mode $(\overline{656_BYPASS} = \text{LOW and ASI} = \text{LOW})$: Data output</p>
B1	AVDD	Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.
B2, C3, C4	PLL_VDD	Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.
B3, F2	RSV		These pins must be left unconnected.
B4	VCO_GND	Input Power	GND pin for the VCO. Connect to analog GND.
B7, D9, G9, J7	IO_GND	Input Power	GND connection for digital I/O. Connect to digital GND.
C1, D1	SDI, $\overline{\text{SDI}}$	Analog Input	Serial Digital Differential Input.
C2, D2, D3, E3, F3, G2	AGND	Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
C7	$\overline{\text{RESET}}$	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible.</p> <p>Used to reset the internal operating conditions to default settings and to reset the JTAG sequence.</p> <p>Normal mode (JTAG_EN = LOW): When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance. When HIGH, normal operation of the device resumes.</p> <p>JTAG test mode (JTAG_EN = HIGH): When LOW, all functional blocks are set to default and the JTAG test sequence is reset. When HIGH, normal operation of the JTAG test sequence resumes.</p>
D4, E4, F4	PLL_GND	Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G4, G5	CORE_GND	Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD	Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	RSV	Input	Connect to core ground.
D8	JTAG_EN	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible.</p> <p>Used to select JTAG test mode or host interface mode.</p> <p>When JTAG_EN is HIGH, the host interface port is configured for JTAG test. When JTAG_EN is LOW, normal operation of the host interface port resumes.</p>
E1	EQ_VDD	Input Power	POWER pin for SDI input. Connect to 3.3V DC analog.
E2	EQ_GND	Input Power	GND pin for SDI input. Connect to analog GND.
E7	SDOUT_TDO	Output	<p>COMMUNICATION SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible.</p> <p>GSPI serial data output/test data out.</p> <p>In JTAG mode (JTAG_EN = HIGH), this pin is used to shift test results from the device.</p> <p>In host interface mode, this pin is used to read status and configuration data from the device.</p>
E8	SDIN_TDI	Input	<p>COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible.</p> <p>GSPI serial data in/test data in.</p> <p>In JTAG mode (JTAG_EN = HIGH), this pin is used to shift test data into the device.</p> <p>In host interface mode, this pin is used to write address and configuration data words into the device.</p>
F1, G1	AGC, $\overline{\text{AGC}}$		Automatic Gain Control. Attach the AGC capacitor across these pins.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description				
F7	$\overline{CS_TMS}$	Input	<p>COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip select / test mode start.</p> <p>In JTAG mode (JTAG_EN = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test.</p> <p>In host interface mode (JTAG_EN = LOW), this pin operates as the host interface chip select and is active LOW.</p>				
F8	SCLK_TCK	Input	<p>COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial data clock signal.</p> <p>In JTAG mode (JTAG_EN = HIGH), this pin is the JTAG clock.</p> <p>In host interface mode (JTAG_EN = LOW), this pin is the host interface serial bit clock.</p> <p>All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.</p>				
F10, F9, H10, H9, J10, J9, K10, K9, J8, K8	DOUT[9:0]	Output	<p>PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible.</p> <hr/> <table border="0"> <tr> <td>20-bit mode 20BIT/$\overline{10BIT}$ = HIGH</td> <td> <p>Video mode ($\overline{656_BYPASS}$ = HIGH and ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for Full HD at 148.5MHz</p> <p>ASI mode ($\overline{656_BYPASS}$ = LOW and ASI = HIGH): Not defined</p> <p>Data-Through mode ($\overline{656_BYPASS}$ = LOW and ASI = LOW): Data output</p> </td> </tr> <tr> <td>10-bit mode 20BIT/$\overline{10BIT}$ = LOW</td> <td>Forced LOW</td> </tr> </table>	20-bit mode 20BIT/ $\overline{10BIT}$ = HIGH	<p>Video mode ($\overline{656_BYPASS}$ = HIGH and ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for Full HD at 148.5MHz</p> <p>ASI mode ($\overline{656_BYPASS}$ = LOW and ASI = HIGH): Not defined</p> <p>Data-Through mode ($\overline{656_BYPASS}$ = LOW and ASI = LOW): Data output</p>	10-bit mode 20BIT/ $\overline{10BIT}$ = LOW	Forced LOW
20-bit mode 20BIT/ $\overline{10BIT}$ = HIGH	<p>Video mode ($\overline{656_BYPASS}$ = HIGH and ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for Full HD at 148.5MHz</p> <p>ASI mode ($\overline{656_BYPASS}$ = LOW and ASI = HIGH): Not defined</p> <p>Data-Through mode ($\overline{656_BYPASS}$ = LOW and ASI = LOW): Data output</p>						
10-bit mode 20BIT/ $\overline{10BIT}$ = LOW	Forced LOW						
G3	RECLK_EN	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible.</p> <p>When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.</p>				

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
G7	$\overline{656_BYPASS}$	Input/Output	<p>CONTROL SIGNAL INPUT/OUTPUT Signal levels are LVCMOS/LVTTL compatible. Indicates the presence or valid video data. When the AUTO/\overline{MAN} bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{656_BYPASS}$ is HIGH when the device locks to a ITU-R BT.656 or BT.1120 compliant input. $\overline{656_BYPASS}$ is LOW under all other conditions. When the AUTO/\overline{MAN} bit in the host interface register is LOW, this pin is an INPUT. No video data descrambling takes place, and none of the video processing features of the device are available when $\overline{656_BYPASS}$ is set LOW. When $\overline{656_BYPASS}$ is set HIGH, the device carries out descrambling and video processing. When $\overline{656_BYPASS}$ and ASI are both set LOW, the device operates in Data-Through mode.</p>
G8	ASI	Input/Output	<p>CONTROL SIGNAL INPUT Signal Levels are LVCMOS/LVTTL compatible. Used to enable/disable ASI data extraction in manual mode. When the AUTO/\overline{MAN} bit in the host interface is LOW, this pin is an input, and when the ASI pin is set HIGH the device carries out ASI data extraction and processing. The $\overline{656_BYPASS}$ pin must be set LOW. When $\overline{656_BYPASS}$ and ASI are both set LOW, the device operates in Data-Through mode. When the AUTO/\overline{MAN} bit in the host interface is HIGH (Default), ASI input is not supported.</p>
H1	BUFF_VDD	Input Power	POWER pin for the serial digital output 50 Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND	Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H3	AUDIO_EN	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Enables or disables audio extraction.</p>
H4	WCLK	Output	48kHz word clock for Audio.
H5	861_EN	Input	<p>CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select CEA-861 timing mode. When 861_EN is HIGH, the device outputs CEA-861 timing signals (HSYNC/VSNC/DE) instead of H:V:F digital timing signals.</p>
H6	XTAL_OUT	Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.
H7	20BIT/ $\overline{10BIT}$	Input	<p>CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to select the output bus width. HIGH = 20-bit LOW = 10-bit</p>

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
H8	PROC_EN	Input	CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to enable or disable audio and video processing features. When PROC_EN is HIGH, the audio and video processing features of the device are enabled. When PROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.
J1, K1	SDO, $\overline{\text{SDO}}$	Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable the serial digital output stage. When SDO_EN is LOW, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH. When SDO_EN is HIGH, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are enabled.
J3	AOUT1/2	Output	Serial Audio Output; Channels 1 and 2.
J4	ACLK	Output	64fs sample clock for audio.
J5	AOUT5/6	Output	Serial Audio Output; Channels 5 and 6.
J6, K6	XTAL2, XTAL1	Analog Input	Input connection for 27MHz crystal.
K2	STANDBY	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH.
K3	AOUT3/4	Output	Serial Audio Output; Channels 3 and 4.
K4	MCLK	Output	Oversampled master clock for audio (128fs, 256fs, 512fs selectable).
K5	AOUT7/8	Output	Serial Audio Output; Channels 7 and 8.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (EQ_VDD, BUFF_VDD, AVDD)	-0.3V to +4.0V
Input Voltage Range (SDI, $\overline{\text{SDI}}$, LB_CONT)	-0.3V to (EQ_VDD + 0.3)V
Input Voltage Range (VBG)	-0.3V to (AVDD + 0.3)V
Input Voltage Range (LF)	-0.3V to (PLL_VDD + 0.3)V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Ambient Operating Temperature (T_A)	-40°C to 95°C
Storage Temperature (T_{STG})	-40°C to 125°C
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

Note:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–

Table 2-2: Recommended Operating Conditions (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	AVDD	–	3.13	3.3	3.47	V	2
Supply Voltage, Serial Digital Input	EQ_VDD	–	3.13	3.3	3.47	V	–
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	2

Notes:

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor.
2. The 3.3V supplies must track the 3.3V supply of an external cable driver.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10-bit Full HD	–	220	265	mA	–
		20-bit Full HD	–	210	265	mA	–
		10/20-bit HD	–	170	220	mA	–
		10/20-bit SD	–	140	185	mA	–
		ASI	–	130	170	mA	–
+1.8V Supply Current	I_{1V8}	10-bit Full HD	–	37	45	mA	–
		20-bit Full HD	–	16	20	mA	–
		10/20-bit HD	–	15	21	mA	–
		10/20-bit SD	–	4	7	mA	–
		ASI	–	4	6	mA	–
+3.3V Supply Current	I_{3V3}	10-bit Full HD	–	150	180	mA	–
		20-bit Full HD	–	115	130	mA	–
		10/20-bit HD	–	110	135	mA	–
		10/20-bit SD	–	90	100	mA	–
		ASI	–	90	95	mA	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Total Device Power (IO_VDD = 1.8V)	P _{1D8}	10-bit Full HD	–	560	680	mW	–
		20-bit Full HD	–	525	640	mW	–
		10/20-bit HD	–	480	590	mW	–
		10/20-bit SD	–	420	520	mW	–
		ASI	–	410	500	mW	–
		Reset	–	390	–	mW	–
		Standby	–	23	45	mW	–
Total Device Power (IO_VDD = 3.3V)	P _{3D3}	10-bit Full HD	–	750	930	mW	–
		20-bit Full HD	–	620	760	mW	–
		10/20-bit HD	–	570	830	mW	–
		10/20-bit SD	–	460	560	mW	–
		ASI	–	440	540	mW	–
		Reset	–	410	–	mW	–
		Standby	–	23	45	mW	–
Digital I/O							
Input Logic LOW	V _{IL}	3.3V or 1.8V operation	IO_GND - 0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V _{IH}	3.3V or 1.8V operation	0.7 x IO_GND	–	IO_VDD + 0.3	V	–
Output Logic LOW	V _{OL}	I _{OL} = 5mA, 1.8V operation	–	–	0.2	V	–
		I _{OL} = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V _{OH}	I _{OH} = 5mA, 1.8V operation	1.4	–	–	V	–
		I _{OH} = 8mA, 3.3V operation	2.4	–	–	V	–
Output Drive Strength	–	–	–	–	–	–	1
Serial Input							
Serial Input Common Mode Voltage	–	75Ω load	–	2.2	–	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD - (0.6 / 2)	BUFF_VDD - (0.45 / 2)	BUFF_VDD - (0.35 / 2)	V	–

Notes:

1. The output drive strength of the digital outputs can be programmed through the host interface. Please see [Table 4-33: Video Core Configuration and Status Registers](#), register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Reset Pulse Width	t_{reset}	–	1	–	–	ms	–
Device Latency							
Full HD (Audio Enabled)	–	PCLK = 148.5MHz	79	–	83	PCLK	1
HD (Audio Enabled)	–	PCLK = 74.25MHz	79	–	83	PCLK	1
SD (Audio Enabled)	–	PCLK = 27MHz	50	–	59	PCLK	1
Full HD (Audio Disabled)	–	PCLK = 148.5MHz	44	–	48	PCLK	2
HD (Audio Disabled)	–	PCLK = 74.25MHz	44	–	48	PCLK	2
SD (Audio Disabled)	–	PCLK = 27MHz	44	–	53	PCLK	2
ASI Mode	–	PCLK = 27MHz	12	–	16	PCLK	3
Parallel Output							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
Output Data Hold Time (1.8V)	t_{oh}	SPI	1.5	-	-	ns	4	
		Full HD 10-bit	Audio Outputs	1.5	-	-	ns	4
			Video Data Bus	0.4	-	-	ns	4
			STAT Pins	0.45	-	-	ns	4
		Full HD 20-bit	Video Data Bus	1.0	-	-	ns	4
			STAT Pins	1.0	-	-	ns	4
		HD 10-bit	Video Data Bus	1.0	-	-	ns	4
			STAT Pins	1.0	-	-	ns	4
		HD 20-bit	Video Data Bus	1.0	-	-	ns	4
			STAT Pins	1.0	-	-	ns	4
		SD 10-bit	Video Data Bus	19.4	-	-	ns	4
			STAT Pins	19.4	-	-	ns	4
		SD 20-bit	Video Data Bus	38.0	-	-	ns	4
			STAT Pins	38.0	-	-	ns	4

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
Output Data Hold Time (3.3V)	t_{oh}	SPI	1.5	-	-	ns	5	
		Full HD 10-bit	Audio Outputs	1.5	-	-	ns	5
			Video Data Bus	0.45	-	-	ns	5
			STAT Pins	0.45	-	-	ns	5
		Full HD 20-bit	Video Data Bus	1.0	-	-	ns	5
			STAT Pins	1.0	-	-	ns	5
		HD 10-bit	Video Data Bus	1.0	-	-	ns	5
			STAT Pins	1.0	-	-	ns	5
		HD 20-bit	Video Data Bus	1.0	-	-	ns	5
			STAT Pins	1.0	-	-	ns	5
		SD 10-bit	Video Data Bus	19.4	-	-	ns	5
			STAT Pins	19.4	-	-	ns	5
		SD 20-bit	Video Data Bus	38.0	-	-	ns	5
			STAT Pins	38.0	-	-	ns	5

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
Output Data Delay Time (1.8V)	t_{od}	SPI	-	-	14.0	ns	6	
		Full HD 10-bit	Audio Outputs	-	-	7.0	ns	6
			Video Data Bus	-	-	1.8	ns	6
			STAT Pins	-	-	2.5	ns	6
			Full HD 20-bit	Video Data Bus	-	-	3.7	ns
		STAT Pins		-	-	4.4	ns	6
		HD 10-bit	Video Data Bus	-	-	3.7	ns	6
			STAT Pins	-	-	4.4	ns	6
		HD 20-bit	Video Data Bus	-	-	3.7	ns	6
			STAT Pins	-	-	4.4	ns	6
		SD 10-bit	Video Data Bus	-	-	22.2	ns	6
			STAT Pins	-	-	22.2	ns	6
		SD 20-bit	Video Data Bus	-	-	41.0	ns	6
			STAT Pins	-	-	41.0	ns	6

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
Output Data Delay Time (3.3V)	t_{od}	SPI	-	-	14.0	ns	7	
		Full HD 10-bit	Audio Outputs	-	-	7.0	ns	7
			Video Data Bus	-	-	1.9	ns	7
			STAT Pins	-	-	2.2	ns	7
		Full HD 20-bit	Video Data Bus	-	-	3.7	ns	7
			STAT Pins	-	-	4.1	ns	7
		HD 10-bit	Video Data Bus	-	-	3.7	ns	7
			STAT Pins	-	-	4.1	ns	7
		HD 20-bit	Video Data Bus	-	-	3.7	ns	7
			STAT Pins	-	-	4.1	ns	7
		SD 10-bit	Video Data Bus	-	-	22.2	ns	7
			STAT Pins	-	-	22.2	ns	7
		SD 20-bit	Video Data Bus	-	-	41.0	ns	7
			STAT Pins	-	-	41.0	ns	7

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes			
Output Data Rise/Fall Time (1.8V)	t_r/t_f	Full HD 10-bit 6pF load	Video Data Bus	0.4	-	-	ns	4		
			STAT Pins	0.3	-	-	ns	4		
			Audio Outputs	0.6	-	-	ns	4		
		All other modes 6pF load	Video Data Bus	0.4	-	-	ns	4		
			STAT Pins	0.4	-	-	ns	4		
			Audio Outputs	0.6	-	-	ns	4		
		Full HD 10-bit 15pF load	Video Data Bus	-	-	-	1.5	ns	6	
			STAT Pins	-	-	-	1.1	ns	6	
			Audio Outputs	-	-	-	2.3	ns	6	
			All other modes 15pF load	Video Data Bus	-	-	-	1.5	ns	6
				STAT Pins	-	-	-	1.4	ns	6
				Audio Outputs	-	-	-	2.3	ns	6
Output Data Rise/Fall Time (3.3V)	t_r/t_f	Full HD 10-bit 6pF load	Video Data Bus	0.5	-	-	ns	5		
			STAT Pins	0.4	-	-	ns	5		
			Audio Outputs	0.6	-	-	ns	5		
		All other modes 6pF load	Video Data Bus	0.5	-	-	ns	5		
			STAT Pins	0.4	-	-	ns	5		
			Audio Outputs	0.6	-	-	ns	5		

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
Output Data Rise/Fall Time (3.3V)	t_r/t_f	Video Data Bus	-	-	1.6	ns	7	
		Full HD 10-bit 15pF load	-	-	1.5	ns	7	
		STAT Pins	-	-	1.5	ns	7	
		Audio Outputs	-	-	2.2	ns	7	
		All other modes 15pF load	-	-	1.6	ns	7	
		STAT Pins	-	-	1.4	ns	7	
		Audio Outputs	-	-	2.2	ns	7	
Serial Digital Input								
Serial Input Data Rate	DR_{SDI}	-	0.27	-	2.97	Gb/s	-	
Serial Input Swing	ΔV_{SDI}	TA=25°C, differential, 270Mb/s & 1.485Gb/s	720	800	950	mV _{p-p}	9	
		TA=25°C, differential, 2.97Gb/s	720	800	880	mV _{p-p}	9	
Achievable Cable Length	-	Full HD	Belden 1694A cable	-	150	-	m	-
			Belden RG59 cable	-	100	-	m	-
		HD	Belden 1694A cable	-	230	-	m	-
			Belden RG59 cable	-	160	-	m	-
		SD	Belden 1694A cable	-	460	-	m	-
			Belden RG59 cable	-	330	-	m	-
Input Return Loss	-	single-ended	15	21	-	dB	10	
Input Resistance	-	single-ended	-	1.52	-	k Ω	-	