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GV7605

Aviia™ Receiver

Key Features

- Serial digital video receiver for standard and high definition component video:
  - SD 525i and 625i
  - HD 720p 24, 25, 30, 50 and 60
  - HD 1080i 50, 60
  - HD 1080p 24, 25, 30, 50 and 60
- Supports 8-bit, 10-bit or 12-bit component digital video:
  - RGB or YCbCr 4:4:4 sampled
  - YCbCr 4:2:2 or 4:2:0 sampled
- Long reach cable performance when combined with the GV8501 cable equalizer
  - 140m typical HD performance over high quality 75Ω coaxial cable
- Serial digital loop-though output
- Integrated audio de-embedder for the extraction of up to 8 channels of 48kHz digital audio
- Supports IEC 13818-1 compliant transport streams over the Asynchronous Serial Interface (ASI)
- Automatic selection between SD/HD component video and ASI input data
- Ancillary (ANC) data detection and extraction
- User selectable processing features, including:
  - Timing Reference Signal (TRS) error detection and correction
  - ANC data checksum error detection and correction
  - Programmable ANC data detection
  - Line number and CRC error detection and correction
  - Illegal video code word re-mapping
- 4-wire Gennum Serial Peripheral Interface (GSPI) for external host command and control
- JTAG test interface
- 1.2V core and 3.3V analog voltage power supplies
- 1.8V or 3.3V selectable digital I/O power supply
- Small footprint 100-BGA (11mm x 11mm)
- Low power operation, typically 405mW
- Pb-free and RoHS compliant

Applications

- Digital Video Recorders (DVR)
- Video servers
- Video mixers and switchers
- Image capture devices
- Video framegrabbers
- Camcorders
- Video monitors & displays

Description

The GV7605 is a serial digital video receiver for standard and high definition component video, operating at 270Mb/s, 1.485Gb/s and 2.97Gb/s data rates. When combined with the GV8501 cable equalizer, the GV7605 is capable of receiving digital video over 75Ω coaxial cable at lengths up to 300m. This provides a complete receive solution for the transmission of both interlaced and progressive component digital video, up to 1920 x 1080, in coaxial cable-based video systems.

Using the GV7605 with the complete Aviia receiver reference design, it is possible to implement an all-digital, bi-directional multimedia interface over coax. This interface allows both DC power and a bi-directional, half-duplex, auxiliary data interface, up to 1Mb/s, to be carried over the same single, robust and cost effective coaxial cable as the high-speed serial digital video. The GV7605 also provides a re-timed serial digital output for video loop-through applications.

The GV7605 includes a broad range of user-selectable processing features, such as Timing Reference Signal (TRS) error detection and extraction, illegal code word re-mapping, and ancillary data packet extraction. The content of ancillary data packets, embedded by a Aviia transmitter, can be extracted and retrieved via the host interface. Device configuration and status reporting is

accomplished via the Gennum Serial Peripheral Interface (GSPI). Alternatively, many processing features and operational modes can be configured directly through external pin settings.

The device can output 8-bit, 10-bit and 12-bit video data, for RGB or YCbCr 4:4:4, and YCbCr 4:2:2 or 4:2:0. A configurable 20-bit wide parallel digital video output bus is provided, with associated pixel clock and timing signal outputs. The GV7605 supports ITU-R BT.656 SD formats, and HD formats conforming to ITU-R BT.709 and BT.1120-6 for 1125-line formats, and SMPTE 296M for 750-line formats. The device may also be configured to output CEA-861 timing.

The GV7605 audio de-embedding function allows the up to 8 channels of serial digital audio within the ancillary data space of the video data stream to be extracted. The audio output signal formats supported by the device include AES/EBU for professional applications, S/PDIF, and I^2S. 16-bit, 20-bit and 24-bit audio formats are supported at 48kHz synchronous-to-video for SD video formats and 48kHz synchronous or asynchronous for HD formats. Additional audio processing features include: individual channel extraction, audio group selection, group replacement, channel swapping and audio channel status extraction.

The GV7605 supports an Asynchronous Serial Interface (ASI) 270Mb/s input, carrying compressed audio and video transport streams, conforming to IEC 13818-1. Transport stream data is output from the device at a synchronous 27MHz clock rate. The device will automatically deserialize and 8b/10b decode the data.

Packaged in a space saving 100-BGA, the GV7605 is ideal for designs where high-density component placement is required. Typically requiring only 405mW power, the device can be used as a high bandwidth alternative to analog composite or component video interfaces, providing a high quality, all-digital, long reach video receive solution.

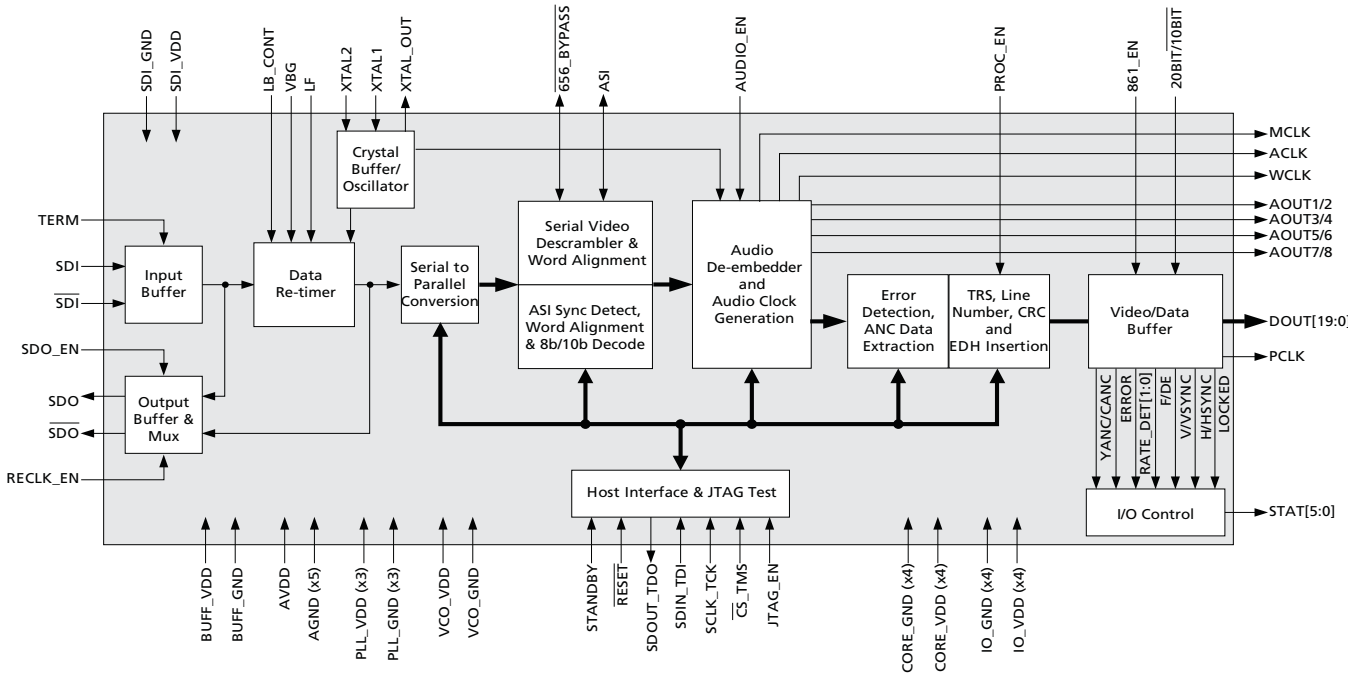

Figure A: GV7605 Functional Block Diagram

Revision History

Version	ECR	Date	Changes and / or Modifications
8	019059	April 2014	Updated Figure 6-1: GV7605 Package Dimensions
7	153582	February 2010	Added analog input absolute maximum ratings to Table 2-1: Absolute Maximum Ratings. Updated device latency values in Table 2-4: AC Electrical Characteristics.
6	152574	September 2009	Updates.
5	152158	June 2009	Modified Section 4.11.1.1, Section 4.12, Section 4.17.4, Section 4.19, and Table 4-34. Added Figure 4-64. Changed 6.3 Marking Diagram.
4	151834	May 2009	Re-ordered the DOUT[19:10] & DOUT[9:0] in Table 1-1 to reflect the pin names. Changed Figure 4-41.
3	151652	April 2009	Changed 4.16.8 Ancillary Data Extraction and its registers.
2	151552	March 2009	Changed DOUT[18_10] and DOUT[9:0] pin descriptions.
1	151322	February 2009	Changed block diagram. Changed $\overline{656}$_BYPASS pin description. Changed/Added H:V:F Timing diagrams. Added GSPI timing delays values. Added Index.
0	150966	December 2008	New document.

Contents

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_ CONT	VCO_ VDD	STAT0	STAT1	IO_ VDD	PCLK	DOUT18	DOUT17
B	AVDD	PLL_ VDD	RSV	VCO_ GND	STAT2	STAT3	IO_ GND	DOUT19	DOUT16	DOUT15
C	SDI	AGND	PLL_ VDD	PLL_ VDD	STAT4	STAT5	$\overline{\text{RESET}}$	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	AGND	AGND	PLL_ GND	CORE_ GND	CORE_ VDD	RSV	JTAG _EN	IO_ GND	IO_ VDD
E	SDI_ VDD	SDI_ GND	AGND	PLL_ GND	CORE_ GND	CORE_ VDD	SDOUT _TDO	SDIN _TDI	DOUT10	DOUT11
F	TERM	RSV	AGND	PLL_ GND	CORE_ GND	CORE_ VDD	$\overline{\text{CS}}$_ TMS	SCLK _TCK	DOUT8	DOUT9
G	RSV	RSV	RECLK _EN	RSV	CORE_ GND	CORE_ VDD	$\overline{656}$_ $\overline{\text{BYPASS}}$	ASI	IO_ GND	IO_ VDD
H	BUFF _VDD	BUFF _GND	AUDIO _EN	WCLK	861_EN	XTAL _OUT	20BIT/ $\overline{\text{10BIT}}$	PROC _EN	DOUT6	DOUT7
J	SDO	SDO _EN	AOUT 1/2	ACLK	AOUT 5/6	XTAL2	IO_ GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STAND BY	AOUT 3/4	MCLK	AOUT 7/8	XTAL1	IO_ VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
A1	VBG	Analog Input	Band Gap voltage filter connection.
A2	LF	Analog Input	Loop Filter component connection.
A3	LB_CONT	Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD	Input Power	POWER pin for the VCO. Connect to 1.2V DC analog through an RC filter (see 5. References & Relevant Standards). VCO_VDD is nominally 0.7V (Do not connect directly to 0.7V).

Table 1-1: Pin Descriptions (Continued)

<table>
<tr><th>Pin Number</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A5, A6, B5, B6, C5, C6</td><td>STAT[0:5]</td><td>Output</td><td>MULTI-FUNCTIONAL OUTPUT PORT.
Signal levels are LVCMOS/LVTTL compatible.
Each of the STAT[5:0] pins can be configured individually to output one of the following signals:
Signal — Default
H/HSYNC — STAT0
V/VSYNC — STAT1
F/DE — STAT2
LOCKED — STAT3
Y/1ANC — STAT4
C/2ANC — –
DATA_ERROR — STAT5
VIDEO_ERROR — –
AUDIO_ERROR — –
EDH_DETECTED — –
CARRIER_DETECT — –
RATE_DET0 — –
RATE_DET1 — –</td></tr>
<tr><td>A7, D10, G10, K7</td><td>IO_VDD</td><td>Input Power</td><td>POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.</td></tr>
<tr><td>A8</td><td>PCLK</td><td>Output</td><td>PARALLEL DATA BUS CLOCK
Signal levels are LVCMOS/LVTTL compatible.
Full HD 10-bit or 20-bit mode — PCLK @ 148.5 or 148.5/1.001MHz
HD 10-bit mode — PCLK @ 148.5 or 148.5/1.001MHz
HD 20-bit mode — PCLK @ 74.25 or 74.25/1.001MHz
SD 10-bit mode — PCLK @ 27MHz
SD 20-bit mode — PCLK @ 13.5MHz</td></tr>
</table>

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description	
B8, A9, A10, B9, B10,C9, C10, C8, E10, E9	DOUT[19:10]	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible.	
			20-bit mode 20BIT/$\overline{10BIT}$ = HIGH	Video mode ($\overline{656\_BYPASS}$ = HIGH and ASI = LOW): Luma data output for SD and HD data rates; Data Stream 1 for Full HD at 148.5MHz ASI mode ($\overline{656\_BYPASS}$ = LOW and ASI = HIGH): Not defined Data-Through mode ($\overline{656\_BYPASS}$ = LOW and ASI = LOW): Data output
			10-bit mode 20BIT/$\overline{10BIT}$ = LOW	Video mode ($\overline{656\_BYPASS}$ = HIGH and ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1/2 for Full HD at 148.5MHz ASI mode ($\overline{656\_BYPASS}$ = LOW and ASI = HIGH): 8b/10b decoded transport stream data Data-Through mode ($\overline{656\_BYPASS}$ = LOW and ASI = LOW): Data output
			Video mode ($\overline{656\_BYPASS}$ = HIGH and ASI = LOW)	Luma data output for SD and HD data rates; Data Stream 1 for Full HD at 148.5MHz (20-bit mode)
			ASI mode ($\overline{656\_BYPASS}$ = LOW and ASI = HIGH)	Transport stream output
			Data-Through mode ($\overline{656\_BYPASS}$ = LOW and ASI = LOW)	Data output
B1	AVDD	Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.	
B2, C3, C4	PLL_VDD	Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.	
B3, F2, G1, G2, G4	RSV		These pins must be left unconnected.	
B4	VCO_GND	Input Power	GND pin for the VCO. Connect to analog GND.	
B7, D9, G9, J7	IO_GND	Input Power	GND connection for digital I/O. Connect to digital GND.	
C1, D1	SDI, $\overline{SDI}$	Analog Input	Serial Digital Differential Input.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
C2, D2, D3, E3, F3	AGND	Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
C7	$\overline{\text{RESET}}$	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG_EN = LOW): When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG_EN = HIGH): When LOW, all functional blocks are set to default and the JTAG test sequence is reset. When HIGH, normal operation of the JTAG test sequence resumes.
D4, E4, F4	PLL_GND	Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G5	CORE_GND	Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD	Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	RSV	Input	Connect to core ground.
D8	JTAG_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG test mode or host interface mode. When JTAG_EN is HIGH, the host interface port is configured for JTAG test. When JTAG_EN is LOW, normal operation of the host interface port resumes.
E1	SDI_VDD	Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	SDI_GND	Input Power	GND pin for SDI buffer. Connect to analog GND.
E7	SDOUT_TDO	Output	COMMUNICATION SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. GSPI serial data output/test data out. In JTAG mode (JTAG_EN = HIGH), this pin is used to shift test results from the device. In host interface mode, this pin is used to read status and configuration data from the device.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description	
E8	SDIN_TDI	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. GSPI serial data in/test data in. In JTAG mode (JTAG_EN = HIGH), this pin is used to shift test data into the device. In host interface mode, this pin is used to write address and configuration data words into the device.	
F1	TERM	Analog Input	Decoupling for internal SDI termination resistors.	
F7	$\overline{CS}$_TMS	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip select / test mode start. In JTAG mode (JTAG_EN = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test. In host interface mode (JTAG_EN = LOW), this pin operates as the host interface chip select and is active LOW.	
F8	SCLK_TCK	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial data clock signal. In JTAG mode (JTAG_EN = HIGH), this pin is the JTAG clock. In host interface mode (JTAG_EN = LOW), this pin is the host interface serial bit clock. All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.	
F10, F9, H10, H9, J10, J9, K10, K9, J8, K8	DOUT[9:0]	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible.	
			20-bit mode 20BIT/$\overline{10BIT}$ = HIGH	Video mode ($\overline{656\_BYPASS}$ = HIGH and ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for Full HD at 148.5MHz ASI mode ($\overline{656\_BYPASS}$ = LOW and ASI = HIGH): Not defined Data-Through mode ($\overline{656\_BYPASS}$ = LOW and ASI = LOW): Data output
			10-bit mode 20BIT/$\overline{10BIT}$ = LOW	Forced LOW
G3	RECLK_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
G7	$\overline{656\_BYPASS}$	Input/Output	CONTROL SIGNAL INPUT/OUTPUT Signal levels are LVCMOS/LVTTL compatible. Indicates the presence or valid video data. When the AUTO/$\overline{MAN}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{656\_BYPASS}$ is HIGH when the device locks to a ITU-R BT.656 or BT.1120 compliant input. $\overline{656\_BYPASS}$ is LOW under all other conditions. When the AUTO/$\overline{MAN}$ bit in the host interface register is LOW, this pin is an INPUT. No video data descrambling takes place, and none of the video processing features of the device are available when $\overline{656\_BYPASS}$ is set LOW. When $\overline{656\_BYPASS}$ is set HIGH, the device carries out descrambling and video processing. When $\overline{656\_BYPASS}$ and ASI are both set LOW, the device operates in Data-Through mode.
G8	ASI	Input/Output	CONTROL SIGNAL INPUT Signal Levels are LVCMOS/LVTTL compatible. Used to enable/disable ASI data extraction in manual mode. When the AUTO/$\overline{MAN}$ bit in the host interface is LOW, this pin is an input, and when the ASI pin is set HIGH the device carries out ASI data extraction and processing. The $\overline{656\_BYPASS}$ pin must be set LOW. When $\overline{656\_BYPASS}$ and ASI are both set LOW, the device operates in Data-Through mode. When the AUTO/$\overline{MAN}$ bit in the host interface is HIGH (Default), ASI input is not supported.
H1	BUFF_VDD	Input Power	POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND	Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H3	AUDIO_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Enables or disables audio extraction.
H4	WCLK	Output	48kHz word clock for Audio.
H5	861_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select CEA-861 timing mode. When 861_EN is HIGH, the device outputs CEA-861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.
H6	XTAL_OUT	Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
H7	20BIT/$\overline{10BIT}$	Input	CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to select the output bus width. HIGH = 20-bit LOW = 10-bit
H8	PROC_EN	Input	CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to enable or disable audio and video processing features. When PROC_EN is HIGH, the audio and video processing features of the device are enabled. When PROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.
J1, K1	SDO, $\overline{SDO}$	Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable the serial digital output stage. When SDO_EN is LOW, the serial digital output signals, SDO and $\overline{SDO}$, are both pulled HIGH. When SDO_EN is HIGH, the serial digital output signals, SDO and $\overline{SDO}$, are enabled.
J3	AOUT1/2	Output	Serial Audio Output; Channels 1 and 2.
J4	ACLK	Output	64fs sample clock for audio.
J5	AOUT5/6	Output	Serial Audio Output; Channels 5 and 6.
J6, K6	XTAL2, XTAL1	Analog Input	Input connection for 27MHz crystal.
K2	STANDBY	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and $\overline{SDO}$, are both pulled HIGH.
K3	AOUT3/4	Output	Serial Audio Output; Channels 3 and 4.
K4	MCLK	Output	Oversampled master clock for audio (128fs, 256fs, 512fs selectable).
K5	AOUT7/8	Output	Serial Audio Output; Channels 7 and 8.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (SDI_VDD, BUFF_VDD, AVDD)	-0.3V to +4.0V
Input Voltage Range (SDI, $\overline{SDI}$, TERM, LB_CONT)	-0.3V to (SDI_VDD + 0.3)V
Input Voltage Range (VBG)	-0.3V to (AVDD + 0.3)V
Input Voltage Range (LF)	-0.3V to (PLL_VDD + 0.3)V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Ambient Operating Temperature (T_A)	$-40°C \leq T_A \leq 95°C$
Storage Temperature (T_{STG})	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

Note:

1. Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–

Table 2-2: Recommended Operating Conditions (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	AVDD	–	3.13	3.3	3.47	V	2
Supply Voltage, Serial Digital Input	SDI_VDD	–	3.13	3.3	3.47	V	2
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	2

Notes:

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor.
2. The 3.3V supplies must track the 3.3V supply of an external EQ and external CD.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10-bit Full HD	–	220	265	mA	–
		20-bit Full HD	–	215	265	mA	–
		10/20-bit HD	–	175	215	mA	–
		10/20-bit SD	–	145	180	mA	–
		ASI	–	135	165	mA	–
+1.8V Supply Current	I_{1V8}	10-bit Full HD	–	32	34	mA	–
		20-bit Full HD	–	32	34	mA	–
		10/20-bit HD	–	20	21	mA	–
		10/20-bit SD	–	6	7	mA	–
		ASI	–	6	7	mA	–
+3.3V Supply Current	I_{3V3}	10-bit Full HD	–	95	105	mA	–
		20-bit Full HD	–	95	105	mA	–
		10/20-bit HD	–	65	75	mA	–
		10/20-bit SD	–	35	45	mA	–
		ASI	–	35	45	mA	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10-bit Full HD	–	380	470	mW	–
		20-bit Full HD	–	350	435	mW	–
		10/20-bit HD	–	300	360	mW	–
		10/20-bit SD	–	235	305	mW	–
		ASI	–	235	305	mW	–
		Reset	–	200	–	mW	–
		Standby	–	16	44	mW	–
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10-bit Full HD	–	580	700	mW	–
		20-bit Full HD	–	580	695	mW	–
		10/20-bit HD	–	430	530	mW	–
		10/20-bit SD	–	290	370	mW	–
		ASI	–	290	370	mW	–
		Reset	–	220	–	mW	–
		Standby	–	16	44	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VDD + 0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_GND - 0.3	V	–
Output Logic LOW	V_{OL}	I_{OL} = 5mA, 1.8V operation	–	–	0.2	V	–
		I_{OL} = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	I_{OH} = 5mA, 1.8V operation	1.4	–	–	V	–
		I_{OH} = 8mA, 3.3V operation	2.4	–	–	V	–
Output Drive Strength	–	–	–	–	–	–	1
Serial Input							
Serial Input Common Mode Voltage	–	75Ω load	–	(SDI_VDD) x 5 / 6	–	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD - (0.6 / 2)	BUFF_VDD - (0.45 / 2)	BUFF_VDD - (0.35 / 2)	V	–

Note:

1. The output drive strength of the digital outputs can be programmed through the host interface. Please see Table 4-34: Video Core Configuration and Status Registers, register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Reset Pulse Width	t_{reset}	–	1	–	–	ms	–
Device Latency							
Full HD (Audio Enabled)	–	PCLK = 148.5MHz	79	–	83	PCLK	1
HD (Audio Enabled)	–	PCLK = 74.25MHz	79	–	83	PCLK	1
SD (Audio Enabled)	–	PCLK = 27MHz	50	–	59	PCLK	1
Full HD (Audio Disabled)	–	PCLK = 148.5MHz	44	–	48	PCLK	2
HD (Audio Disabled)	–	PCLK = 74.25MHz	44	–	48	PCLK	2
SD (Audio Disabled)	–	PCLK = 27MHz	44	–	53	PCLK	2
ASI Mode	–	PCLK = 27MHz	12	–	16	PCLK	3
Parallel Output							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Hold Time (1.8V)	t_{oh}	Full HD 10-bit	SPI	1.5	–	–	ns	4
			Audio Outputs	1.5	–	–	ns	4
			Video Data Bus	0.4	–	–	ns	4
			STAT Pins	0.45	–	–	ns	4
		Full HD 20-bit	Video Data Bus	1.0	–	–	ns	4
			STAT Pins	1.0	–	–	ns	4
		HD 10-bit	Video Data Bus	1.0	–	–	ns	4
			STAT Pins	1.0	–	–	ns	4
		HD 20-bit	Video Data Bus	1.0	–	–	ns	4
			STAT Pins	1.0	–	–	ns	4
		SD 10-bit	Video Data Bus	19.4	–	–	ns	4
			STAT Pins	19.4	–	–	ns	4
		SD 20-bit	Video Data Bus	38.0	–	–	ns	4
			STAT Pins	38.0	–	–	ns	4

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Hold Time (3.3V)	t_{oh}	Full HD 10-bit	SPI	1.5	–	–	ns	5
			Audio Outputs	1.5	–	–	ns	5
			Video Data Bus	0.45	–	–	ns	5
			STAT Pins	0.45	–	–	ns	5
		Full HD 20-bit	Video Data Bus	1.0	–	–	ns	5
			STAT Pins	1.0	–	–	ns	5
		HD 10-bit	Video Data Bus	1.0	–	–	ns	5
			STAT Pins	1.0	–	–	ns	5
		HD 20-bit	Video Data Bus	1.0	–	–	ns	5
			STAT Pins	1.0	–	–	ns	5
		SD 10-bit	Video Data Bus	19.4	–	–	ns	5
			STAT Pins	19.4	–	–	ns	5
		SD 20-bit	Video Data Bus	38.0	–	–	ns	5
			STAT Pins	38.0	–	–	ns	5

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Delay Time (1.8V)	t_{od}	Full HD 10-bit	SPI	–	–	14.0	ns	6
			Audio Outputs	–	–	7.0	ns	6
			Video Data Bus	–	–	1.8	ns	6
			STAT Pins	–	–	2.5	ns	6
		Full HD 20-bit	Video Data Bus	–	–	3.7	ns	6
			STAT Pins	–	–	4.4	ns	6
		HD 10-bit	Video Data Bus	–	–	3.7	ns	6
			STAT Pins	–	–	4.4	ns	6
		HD 20-bit	Video Data Bus	–	–	3.7	ns	6
			STAT Pins	–	–	4.4	ns	6
		SD 10-bit	Video Data Bus	–	–	22.2	ns	6
			STAT Pins	–	–	22.2	ns	6
		SD 20-bit	Video Data Bus	–	–	41.0	ns	6
			STAT Pins	–	–	41.0	ns	6

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Delay Time (3.3V)	t_{od}	Full HD 10-bit	SPI	–	–	14.0	ns	7
			Audio Outputs	–	–	7.0	ns	7
			Video Data Bus	–	–	1.9	ns	7
			STAT Pins	–	–	2.2	ns	7
		Full HD 20-bit	Video Data Bus	–	–	3.7	ns	7
			STAT Pins	–	–	4.1	ns	7
		HD 10-bit	Video Data Bus	–	–	3.7	ns	7
			STAT Pins	–	–	4.1	ns	7
		HD 20-bit	Video Data Bus	–	–	3.7	ns	7
			STAT Pins	–	–	4.1	ns	7
		SD 10-bit	Video Data Bus	–	–	22.2	ns	7
			STAT Pins	–	–	22.2	ns	7
		SD 20-bit	Video Data Bus	–	–	41.0	ns	7
			STAT Pins	–	–	41.0	ns	7

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Rise/Fall Time (1.8V)	t_r/t_f	Full HD 10-bit 6pF load	Video Data Bus	0.4	–	–	ns	4
			STAT Pins	0.3	–	–	ns	4
			Audio Outputs	0.6	–	–	ns	4
		All other modes 6pF load	Video Data Bus	0.4	–	–	ns	4
			STAT Pins	0.4	–	–	ns	4
			Audio Outputs	0.6	–	–	ns	4
		Full HD 10-bit 15pF load	Video Data Bus	–	–	1.5	ns	6
			STAT Pins	–	–	1.1	ns	6
			Audio Outputs	–	–	2.3	ns	6
		All other modes 15pF load	Video Data Bus	–	–	1.5	ns	6
			STAT Pins	–	–	1.4	ns	6
			Audio Outputs	–	–	2.3	ns	6
Output Data Rise/Fall Time (3.3V)	t_r/t_f	Full HD 10-bit 6pF load	Video Data Bus	0.5	–	–	ns	5
			STAT Pins	0.4	–	–	ns	5
			Audio Outputs	0.6	–	–	ns	5
		All other modes 6pF load	Video Data Bus	0.5	–	–	ns	5
			STAT Pins	0.4	–	–	ns	5
			Audio Outputs	0.6	–	–	ns	5

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Rise/Fall Time (3.3V)	t_r/t_f	Full HD 10-bit 15pF load	Video Data Bus	–	–	1.6	ns	7
			STAT Pins	–	–	1.5	ns	7
			Audio Outputs	–	–	2.2	ns	7
		All other modes 15pF load	Video Data Bus	–	–	1.6	ns	7
			STAT Pins	–	–	1.4	ns	7
			Audio Outputs	–	–	2.2	ns	7
Serial Digital Input								
Serial Input Data Rate	DR_{SDI}	–		0.27	–	2.97	Gb/s	–
Serial Input Swing	ΔV_{SDI}	Differential with 100Ω load		500	800	1100	mVp-p	–
Serial Input Jitter Tolerance	IJT	Nominal loop bandwidth	Square wave mod.	0.7	0.8	–	UI	–
Serial Digital Output								
Serial Output Data Rate	DR_{SDO}	–		0.27	–	2.97	Gb/s	–
Serial Output Swing	ΔV_{SDO}	Differential with 100Ω load		350	–	600	mVp-p	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	–		–	–	180	ps	–
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	–		–	–	180	ps	–
Serial Output Intrinsic Jitter	t_{OJ}	Full HD colour bar signal		–	–	100	ps	–
		HD colour bar signal		–	–	100	ps	–
		SD colour bar signal		–	–	400	ps	–
Serial Output Duty Cycle Distortion	DCD_{SDD}	Full HD		–	10	–	ps	–
		HD		–	10	–	ps	–
		SD		–	20	–	ps	–
Synchronous lock time	–	–		–	–	25	µs	–
Asynchronous lock time	–	–		100	–	825	µs	–