Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

GV7700

HD-VLC™ Transmitter

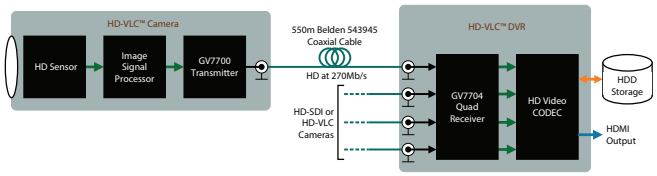
Key Features

- Serial digital video transmitter for HD and 3G video surveillance and HDcctv applications
- Quad rate operation: 270Mb/s, 540Mb/s, 1.485Gb/s, and 2.97Gb/s
- Supports HDcctv 1.0, HD-SDI (ST 292), 3G-SDI (ST 424), and SD-SDI (ST 259)[1]
- Integrated High Definition Visually Lossless CODEC (HD-VLC™) for extended cable reach:
  - HD over 550m of Belden 543945 CCTV coax at 270Mb/s
  - Full HD over 300m of Belden 543945 CCTV coax at 540Mb/s
  - HD over 150m of Cat-5e/6 UTP cable at 270Mb/s
- Configurable 50/75Ω cable driver output, for both coaxial and twisted pair cable transmission
- Integrated audio embedder with support for up to 4 channels of I^2S serial digital audio at 32kHz, 44.1kHz and 48kHz sample rates
- Downstream ancillary data insertion
- Supports both 720p and 1080p HD formats:
  - Full HD: 1080p50/59.94/60fps
  - HD: 1080p25/29.97/30fps
  - HD: 720p25/29.97/30/50/59.94/60fps
- Support for both 8/10-bit and 16/20-bit BT.1120 compliant video interfaces, with embedded TRS or external HVF timing
- 4-wire Gennum Serial Peripheral Interface (GSPI 2.0) for external host command and control
- Dedicated JTAG test interface
- 1.8V core power supply and 1.8V or 3.3V digital I/O supply
- Small-footprint 84-pin dual-row QFN (7mm x 7mm)
- Low power operation, typically 180mW
- Wide operating temperature range: -20°C to + 85°C
- Pb-free and RoHS compliant

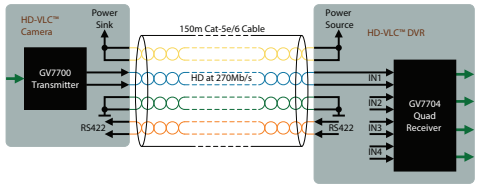
Applications

- HD/3G security cameras
- Industrial cameras
- HD-SDI, 3G-SDI, and HDcctv peripherals
- Media converters
- Video multiplexers

Coaxial Cable Application



UTP Cable Application



Description

The GV7700 is a serial digital video transmitter for High Definition component video. With integrated cable driving technology, the GV7700 is capable of transmitting compressed video at 270Mb/s or 540Mb/s, or uncompressed video at 1.485Gb/s or 2.97Gb/s, over 75Ω coaxial cable, or differentially over 100Ω twisted pair cable.

The GV7700 integrates the High Definition Visually Lossless CODEC (HD-VLC™) technology, which has been developed specifically to reduce the transmission data rate of HD video over both coaxial and unshielded twisted pair (UTP) cable. This is achieved by encoding the HD video, normally transmitted at a serial data rate of 1.485Gb/s, to the same rate as Standard Definition (SD) video, at 270Mb/s serial data rate.

At 270Mb/s, the effect of cable loss is greatly reduced, resulting in much longer cable transmission. For 75Ω coaxial cable, HD-VLC allows a 1.485Gb/s HD signal to be transmitted up to 3x the normal reach. In typical video over coaxial installations, when paired with Semtech's GV7704 HD-VLC receiver, cable distances over 550m are possible.

Similarly, a 2.97Gb/s 3G signal can be transmitted at 540Mb/s using HD-VLC.

The GV7700 can also be configured to transmit HD and 3G video over UTP cable, such as Cat-5e and Cat-6 cable, when HD-VLC encoded at 270Mb/s and 540Mb/s, respectively.

The device supports both 8-bit and 10-bit per pixel YCbCr 4:2:2 BT.1120 component digital video. A configurable 20-bit or 10-bit wide parallel digital video input bus is provided, with associated pixel clock and timing signal inputs. The GV7700 supports direct interfacing of HD video formats conforming to ITU-R BT.709 and BT.1120-6 for 1125-line formats, and SMPTE ST 296 for 750-line formats.

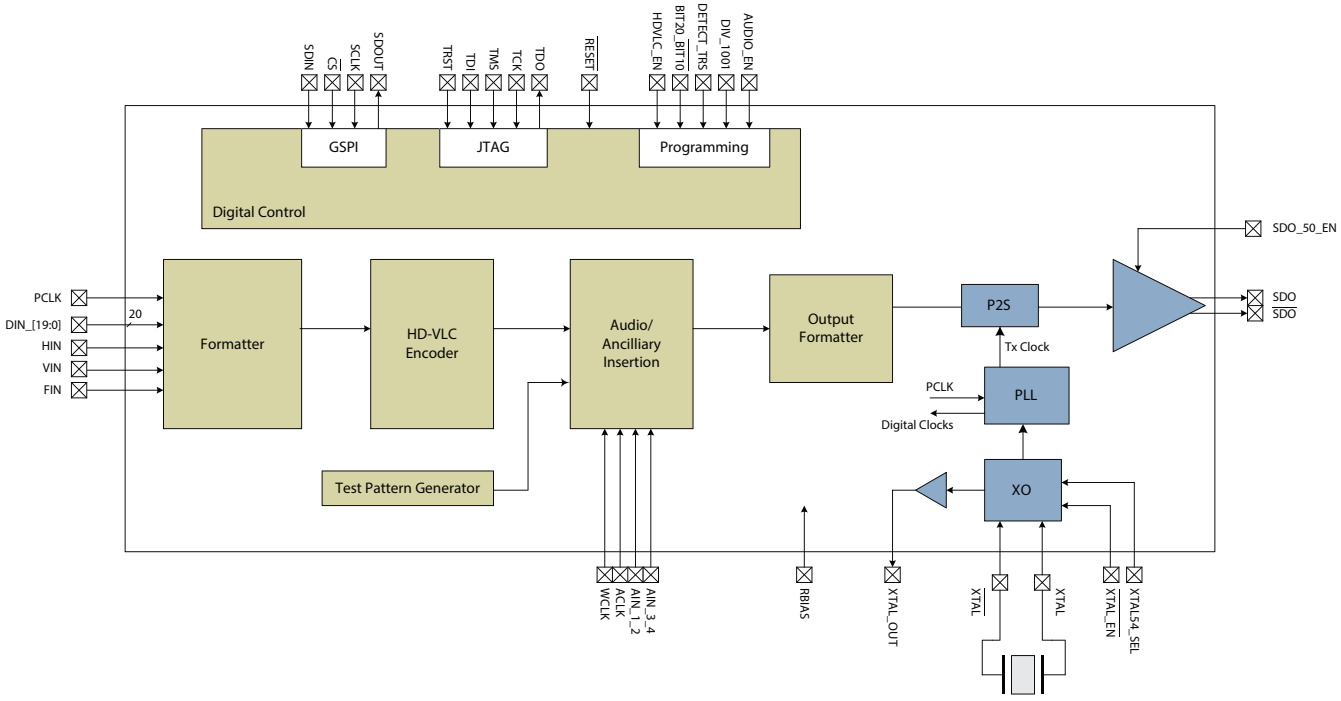
The GV7700 features an audio embedding core, which supports up to 4 channels of I^2S serial digital audio within the ancillary data space of the video data stream. The audio embedding core supports 32kHz, 44.1kHz, and 48kHz sample rates.

The GV7700 supports the insertion of ancillary data into the horizontal blanking of the video data stream. User data can be programmed via the GSPI, allowing downstream communication from the video source to sink device. The ancillary data packing format is compliant with HDcctv 2.0 communications protocol.

Packaged in a space-saving 84-pin dual-row QFN, the GV7700 is ideal for single PCB security cameras, where high-density component placement is required. Typically requiring only 180mW of power, the device does not require any special heat sinking or air flow, reducing the over-cost of HD security camera designs.

[1] *Frame structure with encoded HD only. Does not support SD/D1 video.*

Functional Block Diagram



GV7700 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Description
8	029991	—	March 2016	Addition of Figure 3-3: XTAL_N, XTAL_P, XTAL_EN. Updates to values in Table 4-6: Cable Reach for Various Cable Types (In Meters).
7	029012	—	December 2015	Updated values in Table 2-3: AC Electrical Characteristics.
6	028866	—	December 2015	Updated to Final Data Sheet from Preliminary Data Sheet.
5	027517	—	September 2015	Removed Proprietary and Confidential from footer. Updated Table 1-1, Table 2-3, Section 4.4, Section 4.11, Section 4.14, Figure 4-18, and Figure 6-1. Added Figure 6-2.
4	027026	—	July 2015	Updated cable reach values. Updated Table 2-2 and Table 2-3.
3	025836	—	May 2015	Updated to Preliminary Data Sheet from Draft Data Sheet
2	025126	—	April 2015	Updated GV7700 Functional Block Diagram, Figure 1-1, Figure 6-1. Updated Table 2-2 and Table 2-3. Various updates throughout document.
1	024223	—	February 2015	Updated Table 1-1, Table 2-2, Section 4.1
0	020611	—	August 2014	New Document

Contents

1. Pin Out

1.1 GV7700 Pin Assignment

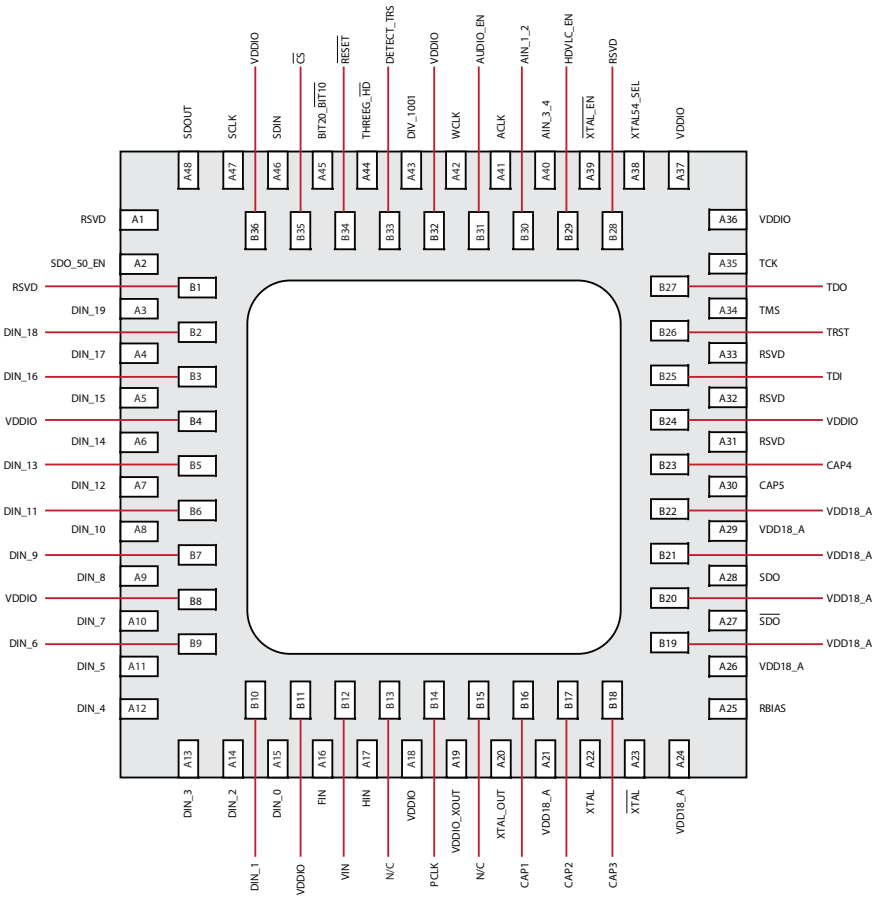


Figure 1-1: GV7700 Pin Out

1.2 Pin Descriptions

Table 1-1: GV7700 Pin Descriptions

Pin Number	Name	Type	Description
A1	RSVD	—	Connect to ground.
A2	SDO_50_EN	Input	HIGH = device outputs a 100Ω differential signal. LOW = device outputs a 75Ω single-ended output signal, with both complementary outputs ON by default. Each output can be manually disabled via GSPI. Schmitt Trigger Input with Pull-Down.
B1	RSVD	—	Connect to ground.
A3, B2, A4, B3, A5, A6, B5, A7, B6, A8	DIN_[19:10]	Input	Parallel data bus inputs [19:10]. If BIT20_$\overline{\text{BIT10}}$ = HIGH, the input data format must be word aligned, demultiplexed Luma and Chroma data. DIN_[19:10] are the input pins for Luma data. If BIT20_$\overline{\text{BIT10}}$ = LOW, the multiplexed Luma and Chroma data is presented on these pins.
B7, A9, A10, B9, A11 A12, A13, A14, B10, A15	DIN_[9:0]	Input	Parallel data bus inputs [9:0]. If BIT20_$\overline{\text{BIT10}}$ = HIGH, the input data format must be word aligned, demultiplexed Luma and Chroma data. DIN_[9:0] are the input pins for Chroma data. If BIT20_$\overline{\text{BIT10}}$ = LOW, these pins are unused and should be tied to ground.
B4, B8, B11, A18, B24, A36, A37, B32, B36	VDDIO	Power	Connect to 1.8V or 3.3V.
A16	FIN	Input	Field identification. Used in interlaced mode.
B12	VIN	Input	Vertical blanking.
A17	HIN	Input	Horizontal blanking.
B13	N/C	—	Do not connect.
B14	PCLK	Input	148.5MHz/74.25MHz input clock representing the time allocated to one 10 or 20-bit pixel.
A19	VDDIO_XOUT	Power	Connect to 1.8V or 3.3V[1].
B15	N/C	—	Do not connect.
A20	XTAL_OUT	Analog Output	Output capable of driving ISP clock input.
A21, A24, A26, B19, B20, B21, A29, B22	VDD18_A	Power	Connect to 1.8V.
B16	CAP1	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.

Table 1-1: GV7700 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
B17	CAP2	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.
A22	XTAL	Analog Input/Output	Pin to external 27MHz or 54MHz crystal. When not using a crystal reference ($\overline{\text{XTAL\_EN}}$ = HIGH), connect XTAL to ground.
B18	CAP3	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.
A23	$\overline{\text{XTAL}}$	Analog Input/Output	Pin to external 27MHz or 54MHz crystal. When not using a crystal reference ($\overline{\text{XTAL\_EN}}$ = HIGH), $\overline{\text{XTAL}}$ can be left floating.
A25	RBIAS	Analog Input/Output	External 11kΩ resistor for bias reference. Connect the resistor to ground.
A27, A28	$\overline{\text{SDO}}$, SDO	Analog High-Speed Output	Serial differential output signal. Single-ended operation at data rates of 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s, 540Mb/s, or 270Mb/s.
B23	CAP4	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.
A30	CAP5	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.
A31	RSVD	—	Connect to ground.
A32	RSVD	—	This pin must be set HIGH.
B25	TDI	Input	Dedicated JTAG pin – Test data input. This pin is used to shift JTAG test data into the device. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin may be left floating.
A33	RSVD	—	Connect to ground.
B26	TRST	Input	Dedicated JTAG pin – Test Reset. When set LOW, the JTAG logic will be reset. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin must be pulled LOW.
A34	TMS	Input	Dedicated JTAG pin – Test Mode Select. This pin is used to control the operation of the JTAG test. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin may be left floating.
B27	TDO	Output	Dedicated JTAG pin – Test data output. This pin is used to shift results from the device.

Table 1-1: GV7700 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
A35	TCK	Input	Dedicated JTAG pin – Serial data clock signal. This pin is the JTAG clock. Schmitt Trigger Input. If JTAG is not used this pin must be pulled LOW.
A38	XTAL54_SEL	Input	HIGH = for use with a 54MHz crystal. LOW = for use with a 27MHz crystal (default). Schmitt Trigger Input with Pull-Down.
B28	RSVD	—	Connect to ground
A39	$\overline{\text{XTAL\_EN}}$	Input	HIGH = when using the PCLK input as a frequency reference. LOW = when using an external XTAL as a frequency reference. Schmitt Trigger Input with Pull-Down.
B29	HDVLC_EN	Input	HIGH = Enables HD-VLC compression for extended cable reach. LOW = Disables HD-VLC compression.
A40	AIN_3_4	Input	I^2S Serial Audio Input; Channels 3 and 4. Schmitt Trigger Input.
B30	AIN_1_2	Input	I^2S Serial Audio Input; Channels 1 and 2. Schmitt Trigger Input.
A41	ACLK	Input	Serial Audio Input bit clock. Serial bit clock for audio data from pins AIN_1_2 and AIN_3_4. Schmitt Trigger Input.
B31	AUDIO_EN	Input	HIGH = Enables the device to support the insertion of 4 audio channels. LOW = Disables device audio support.
A42	WCLK	Input	Serial Audio Left/Right Clock. Word rate clock for the audio data from pins AIN_1_2 and AIN_3_4. Supports sampling frequencies of 32KHz, 44.1kHz, and 48kHz. Schmitt Trigger Input.
A43	DIV_1001	Input	HIGH = Enable device support for when the incoming frame rate is 60/1.001 or 30/1.001 frames per second. LOW = When the incoming frame rate is 60, 50, 30, or 25 frames per second.
A44	THREEG_$\overline{\text{HD}}$	Input	HIGH = 3G video input. LOW = HD video input.
B33	DETECT_TRS	Input	Control Signal Input. Used to select external HVF timing mode or TRS extraction timing mode. LOW = the device extracts all internal timing from the supplied H:V:F. HIGH = the device extracts all internal timing from TRS signals embedded in the supplied video stream.

Table 1-1: GV7700 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
B34	$\overline{\text{RESET}}$	Input	Digital active-low reset input. Used to reset the internal operating conditions to default settings. Minimum reset duration of 10ms. See Section 4.14. Device configuration pins should be set prior to device reset. Schmitt Trigger Input.
A45	BIT20_$\overline{\text{BIT10}}$	Input	HIGH = Selects 20-bit wide input interface. LOW = Selects 10-bit wide input interface.
B35	$\overline{\text{CS}}$	Input	Chip select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Active-low input.
A46	SDIN	Input	Serial data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port.
A47	SCLK	Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port.
A48	SDOUT	Output	Serial data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port.
—	Center Pad	Power	Common analog and digital ground connection, and main thermal path for device.

Notes:

1. Serial output jitter increases by 10ps at 3.3V.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage, Digital I/O (VDDIO)	-0.5V to +3.6V
Supply Voltage, Analog (VDD18_A)	-0.5V to +2.5V
DC Input Voltage, V_{IN} (except I/O pins)	-0.5V to (VDDIO + 0.5V)
DC Output Voltage, V_{OUT} (except I/O pins)	-0.5V to (VDDIO + 0.5V)
Input ESD Voltage (HBM)	2.5kV
Input ESD Voltage (CDM)	1kV
Storage Temperature Range (T_S)	-50°C to 125°C
Operating Temperature Range (T_A)	-40°C to 85°C
Solder Reflow Temperature (4s)	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC and DC Electrical Characteristics is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

VDD18_A = 1.8V±5% and TA = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, Digital I/O	VDDIO	1.8V mode	1.71	1.8	1.89	V	—
		3.3V mode	3.13	3.3	3.47	V	—
Supply Voltage, Analog	VDD18_A		1.71	1.8	1.89	V	—
Supply Current, Digital I/O	I_{DDIO}	1.8V mode	—	0.25	0.5	mA	—
		3.3V mode	—	3.5	4.75	mA	—
Supply Current, Analog	I_{DD18_A}		—	100	115	mA	1

Table 2-2: DC Electrical Characteristics (Continued)

VDD18_A = 1.8V±5% and TA = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Total Power Consumption	P_{total}	HD mode	—	140	170	mW	2
		3G mode	—	160	180	mW	2
		270 mode	—	180	215	mW	2
		540 mode	—	240	275	mW	2
External RBIAS Resistor			10.89	11	11.1	kΩ	—
Power Supply Noise Mask		0Hz–1.5GHz	—	—	20	mV_{pp}	3
Digital Logic Input	V_{IL}	Input LOW	-0.3	—	0.63	V	—
	V_{IH}	Input HIGH	1.17	—	3.465	V	—
Digital Logic Output	V_{OL}	Output LOW	—	—	0.45	V	—
	V_{OH}	Output HIGH	1.35	—	—	V	—

Notes:

1. SD mode.
2. Max = 85°C, VDD18_A = 1.89V.
3. Using recommended power supply decoupling. See Figure 6-1: GV7700 Typical Application Circuit.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VDD18_A = 1.8V±5% and TA = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Conditions							
Input PCLK clock frequency		10-bit mode	—	148.5	—	MHz	1
		20-bit mode	—	74.25	—	MHz	1, 3
PCLK Duty Cycle	DC_{PCLK}		40	—	60	%	—
Input Data Setup Time	t_{SU}		1.2	—	—	ns	—
Input Data Hold Time	t_{HOLD}		0.8	—	—	ns	—
Output Driver							
Impedance		75Ω single-ended	66	75	84	Ω	—
		100Ω differential	88	100	112	Ω	—

Table 2-3: AC Electrical Characteristics (Continued)

VDD18_A = 1.8V±5% and TA = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Return loss		1MHz - 5MHz	—	—	17.9	dB	—
		5MHz - 1.485GHz	—	—	6.7	dB	—
		1.485GHz - 2.25GHz	—	—	4	dB	—
Amplitude		75Ω single-ended	0.36	0.8	0.9	V_{pp}	—
		100Ω differential	0.36	0.8	0.9	V_{ppd}	—
Rise/Fall Time		100Ω differential 20% - 80%	—	85	95	ps	—
		75Ω single-ended 20% - 80%	—	102	150	ps	—
Rise/Fall Time Mismatch		20% - 80%	—	—	50	ps	—
Overshoot			—	—	10	%	—
Output Total Jitter		Data rate = 270Mb/s	—	0.021	—	UI_{pp}	2
		Data rate = 540Mb/s	—	0.04	—	UI_{pp}	2
		Data rate = 1.485Gb/s	—	0.115	—	UI_{pp}	2
		Data rate = 2.97Gb/s	—	0.2	—	UI_{pp}	2
De-emphasis		Post-Cursor	0	1	—	dB	—
Crystal Oscillator							
External Crystal Reference Frequency			—	27 or 54	—	MHz	—
Load Capacitance			8	—	9	pF	—
Start-up time			—	100	—	ms	—
Accuracy			—	±20	±100	ppm	—
GSPI Digital Control							
GSPI Read/Write Clock Frequency			—	—	40	MHz	—
Reset Time			10	—	—	ms	—
Register Access Time			—	—	300	ns	—

Notes:

1. If DIV_1001 = HIGH, divide the listed PCLK frequency by 1.001.
2. Jitter performance is only guaranteed when using a crystal (27/54MHz) as the clock reference for the device. Jitter performance is not guaranteed when using the PCLK clock generated by the ISP as the reference for the device.
3. In 3G 20-bit mode, the PCLK is 148.5MHz.

3. Input/Output Circuits

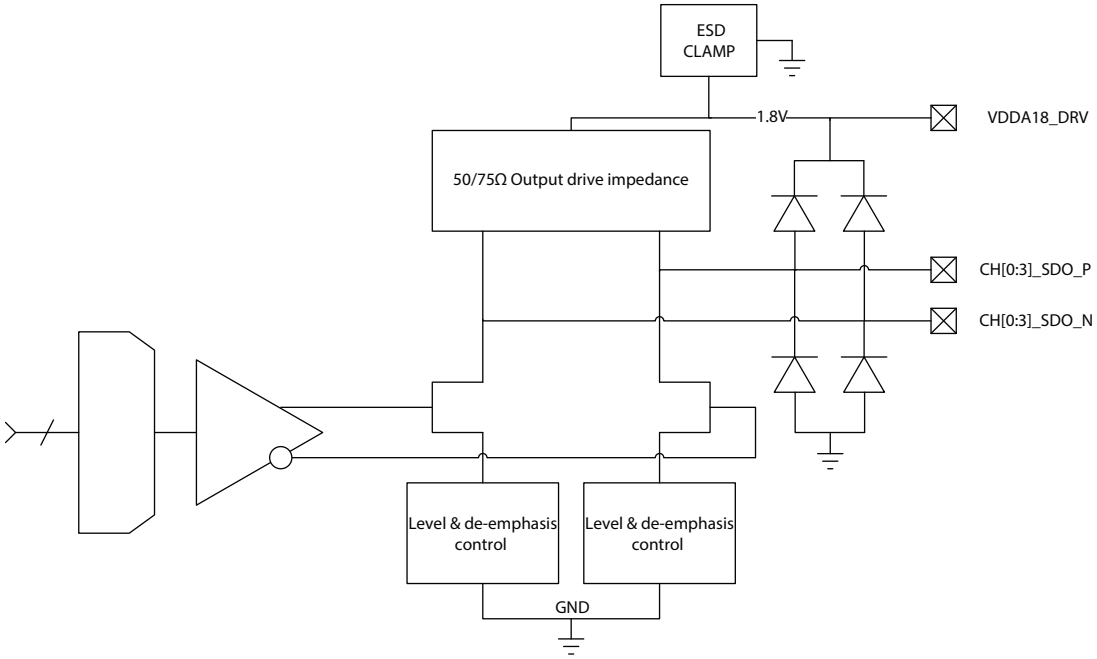


Figure 3-1: Serial Output Driver

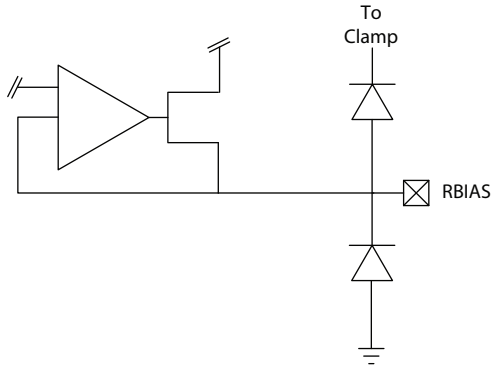


Figure 3-2: RBIAS

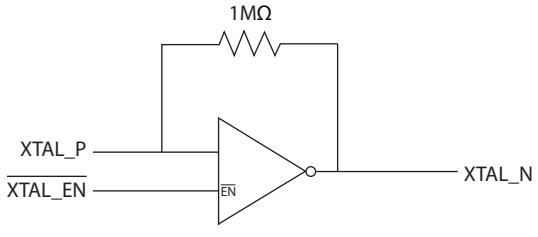


Figure 3-3: XTAL_N, XTAL_P, $\overline{\text{XTAL\_EN}}$

4. Detailed Description

4.1 Functional Overview

The GV7700 is a low cost, dual-rate HDcctv transmitter with integrated HD-VLC encoding. With integrated cable driving technology, the GV7700 is capable of transmitting compressed video at 270Mb/s or 540Mb/s, or uncompressed video at 1.485Gb/s or 2.97Gb/s, over 75Ω coaxial cable. Compressed signals can also be transmitted differentially over 100Ω twisted pair cable.

The High Definition Visually Lossless CODEC (HD-VLC™) technology is integrated in order to reduce the transmission data rate of HD video over both coaxial and unshielded twisted pair (UTP) cable. This is achieved by encoding the HD-SDI video, normally transmitted at a serial data rate of 1.485Gb/s, to the same rate as Standard Definition (SD-SDI) video, at 270Mb/s serial data rate. This provides extended cable reach for HD video up to 550m over Belden 543945 CCTV coax or 150m over Cat-5e/6 UTP cable. Similarly, 3G-SDI normally transmitted at 2.97Gb/s can be encoded down to 540Mb/s.

The GV7700 features an audio embedding core, which supports up to 4 channels of I^2S serial digital audio within the ancillary data space of the video data stream. The audio embedding core supports 32kHz, 44.1kHz, and 48kHz sample rates.

The device allows for both 8-bit and 10-bit per pixel YCbCr 4:2:2 BT.1120 component digital video. A configurable 20-bit wide parallel digital video input bus is provided, with associated pixel clock and H/V/F timing signal inputs.

The GV7700 supports the insertion of ancillary data into the horizontal blanking of the video data stream. User data can be programmed via the GSPI, allowing downstream communication from the video source to sink device. The ancillary data packing format is compliant with HDcctv 2.0 communications protocol.

The device includes a 4-wire Gennum Serial Peripheral Interface (GSPI 2.0) for external host command and control. All read or write access to the GV7700 is initiated and terminated by the application host processor. The host interface is provided to allow optional configuration of some of the functions and operating modes of the GV7700.

It is recommended to use the integrated low-noise crystal oscillator and an external crystal as the primary reference clock for the GV7700. This configuration will yield the optimal jitter performance. Degraded performance will likely occur when using a PCLK input from the ISP which typically has much more jitter. A derived clock must be used as the clock reference by the Image Signal Processing (ISP) IC to avoid any frequency mismatch. In this case, connect the GV7700's XTAL_OUT pin to the ISP's reference frequency input. Crystal values of 27MHz or 54MHz may be used, depending on the ISP requirement. XTAL54_SEL must be HIGH when using a 54MHz crystal and LOW when using a 27MHz crystal.

Jitter performance is only guaranteed when using a crystal (27/54MHz) as the clock reference for the device. Jitter performance is not guaranteed when using the PCLK clock generated by the ISP as the reference for the device.

4.2 Parallel Video Data Inputs DIN_[19:0]

Data signal inputs enter the device on the rising edge of PCLK, as shown in Figure 4-1.

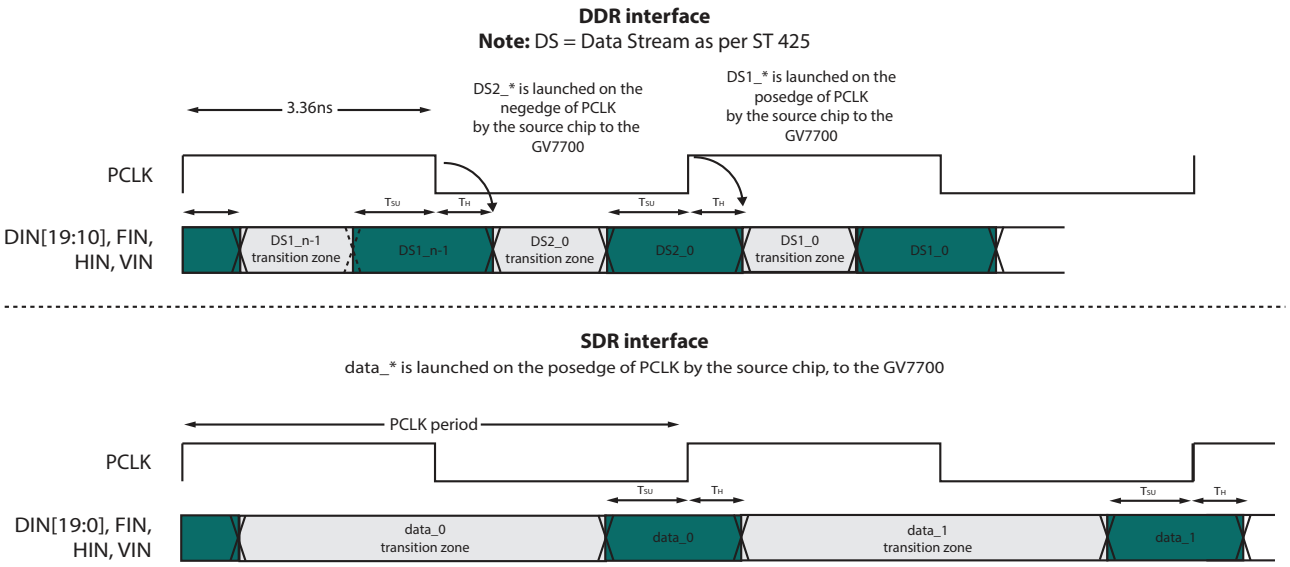


Figure 4-1: GV7700 Video Interface Timing Diagram

Table 4-1: GV7700 Parallel Input AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data set-up time	T_{SU}	50% levels; 1.8V operation	1.2	—	—	ns
Input data hold time	T_H		0.8	—	—	ns

The GV7700 is a high performance serial digital video and audio transmitter. Source series termination resistors should be used to minimize reflections on the parallel video data inputs, PCLK, audio inputs, and H, V, F timing input signals. This will ensure that signals are received correctly by the GV7700. Resistors must be placed at the signal source away from the GV7700 inputs.

4.2.1 Parallel Input In Video Mode

Data must be presented to the input bus in either multiplexed or demultiplexed form, depending on the setting of the BIT20_$\overline{\text{BIT10}}$ pin.

When operating in 20-bit mode (BIT20_$\overline{\text{BIT10}}$ = HIGH), the input data format must be word aligned, demultiplexed Luma and Chroma data. The Luma (Y) data must be presented on the DIN[19:10] pins, and the Chroma (Cb/Cr) data must be presented on the DIN[9:0] pins.

When operating in 10-bit mode (BIT20_$\overline{\text{BIT10}}$ = LOW), the input data format must be word aligned, multiplexed Luma and Chroma data. In this mode, the data must be presented on the DIN[19:10] pins. The DIN[9:0] inputs are ignored and should be tied to ground.

When operating in 10-bit mode (BIT20_BIT10 = LOW) with 3G video (THREEG_$\overline{HD}$ = HIGH), the PCLK input is DDR 148.5MHz.

4.2.1.1 High Definition Video Input Formats

ITU-R BT.1120 describes the serial and parallel format for 1080-line interlaced and progressive digital video. The field/frame blanking period (V), the line blanking period (H), and the field identification (F), are embedded as digital timing codes (TRS) within the video. Data is transmitted over two 10-bit buses, one for Luma (Y') and one for colour difference ($C'_BC'_R$), operating at a clock rate of 74.25MHz or 74.25/1.001MHz.

The following figures show horizontal and vertical timing for 1080-line interlaced systems.

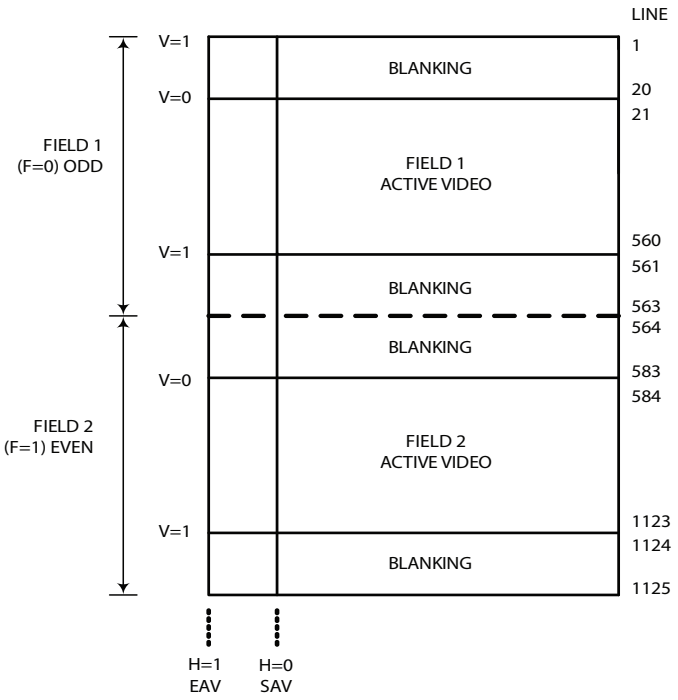


Figure 4-2: Field Timing Relationship for 1080-line Interlaced Systems

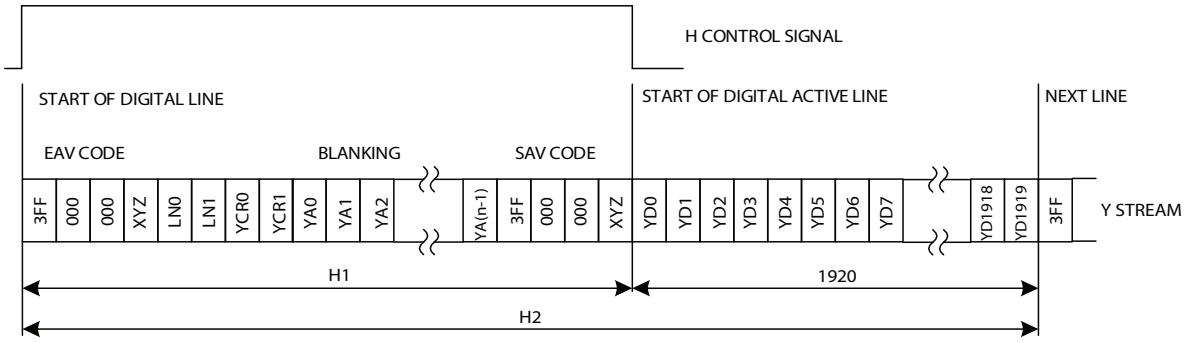


Figure 4-3: Luma Stream Over One Video Line - 1080i

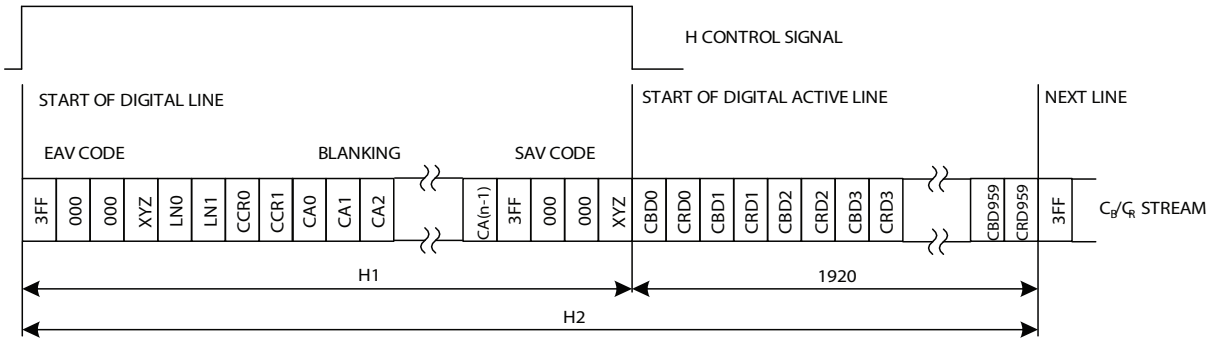


Figure 4-4: Chroma Stream Over One Video Line - 1080i

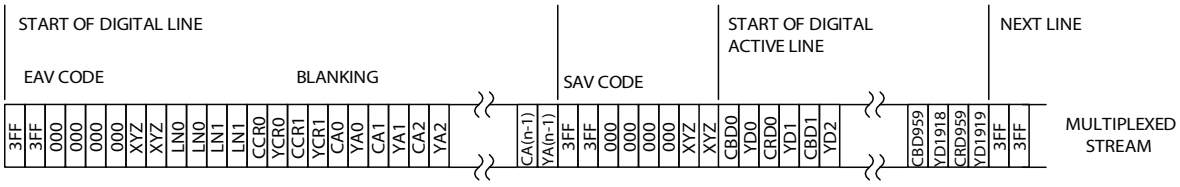


Figure 4-5: Multiplexed Luma and Chroma Over One Video Line - 1080i

Table 4-2: 1080-line Interlaced Horizontal Timing

Interlaced	60Hz or 60/1.001Hz	50Hz
H1	280	720
H2	2200	2640

4.2.1.2 High Definition 1080p Input Formats

ITU-R BT.1120 also includes progressive scan formats with 1080 active lines, with $Y'C'_BC'_R$ 4:2:2 sampling at pixel rates of 74.25MHz or 74.25/1.001MHz. The following diagrams show horizontal and vertical timing for 1080-line progressive systems.

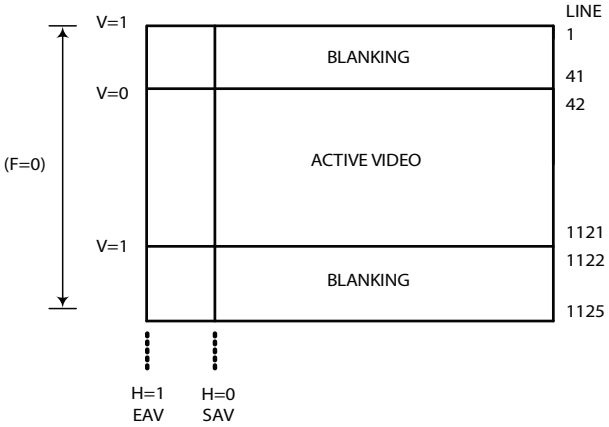


Figure 4-6: Frame Timing Relationship For 1080-line Progressive Systems

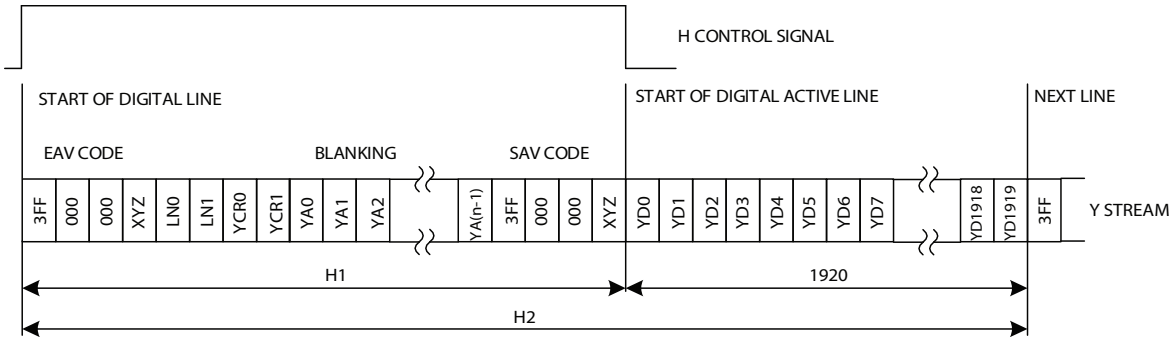


Figure 4-7: Luma Stream Over One Video Line - 1080p

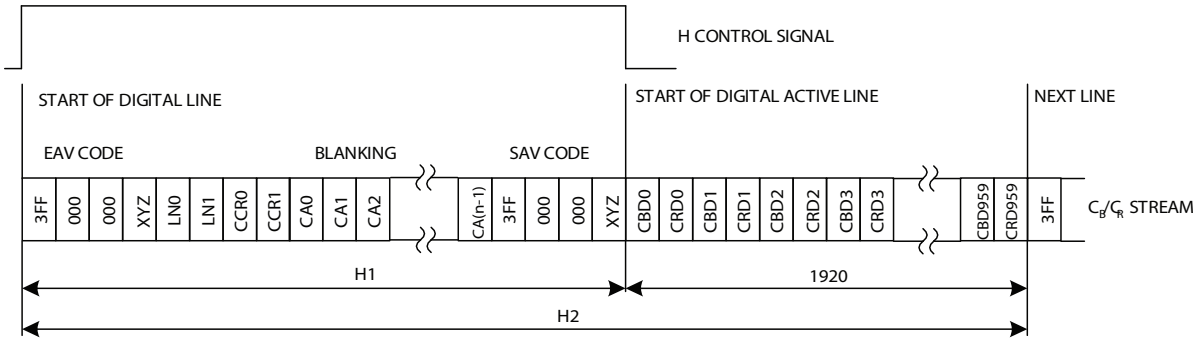


Figure 4-8: Chroma Stream Over One Video Line - 1080p

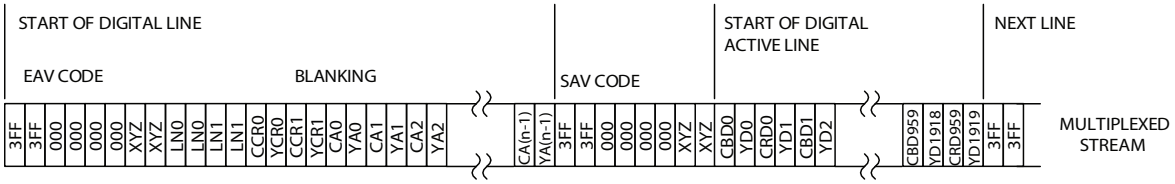


Figure 4-9: Multiplexed Luma and Chroma Over One Video Line - 1080p

Table 4-3: 1080-line Progressive Horizontal Timing

Progressive	30Hz, 30/1.001Hz, 60Hz, 60/1.001Hz	25Hz or 50Hz	24Hz or 24/1.001Hz
H1	280	720	830
H2	2200	2640	2750

4.2.1.3 High Definition 720p Input Formats

The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for progressive scan 720-line HD image formats. SMPTE ST 296-2001 specifies the representation for 720p digital $Y'C'_BC'_R$ 4:2:2 signals at pixel rates of 74.25MHz or 74.25/1.001MHz.

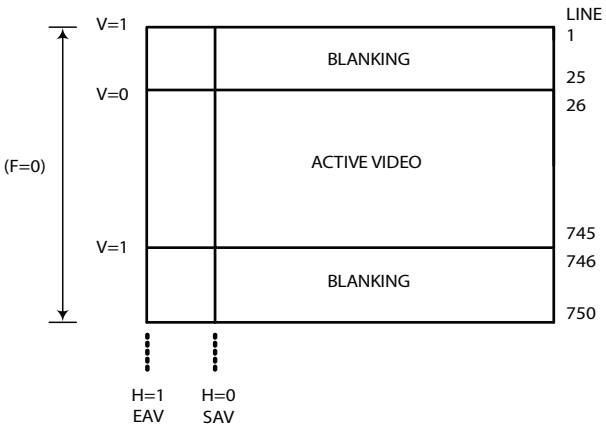


Figure 4-10: 720p Digital Vertical Timing

The frame rate determines the horizontal timing, which is shown in Table 4-4.

Table 4-4: 720p Horizontal Timing

Frame Rate	H = 1 Sample Number	H = 0 Sample Number	Total Samples Per Line
25	1280	0	3960
30 or 30/1.001	1280	0	3300
50	1280	0	1980
60 or 60/1.001	1280	0	1650

4.2.1.4 3G-SDI 1080p Input Formats

The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for 3G-SDI image formats in ST 425. The GV7700 supports 1080p50/60 $Y'C'_BC'_R$ 4:2:2 8/10-bit.

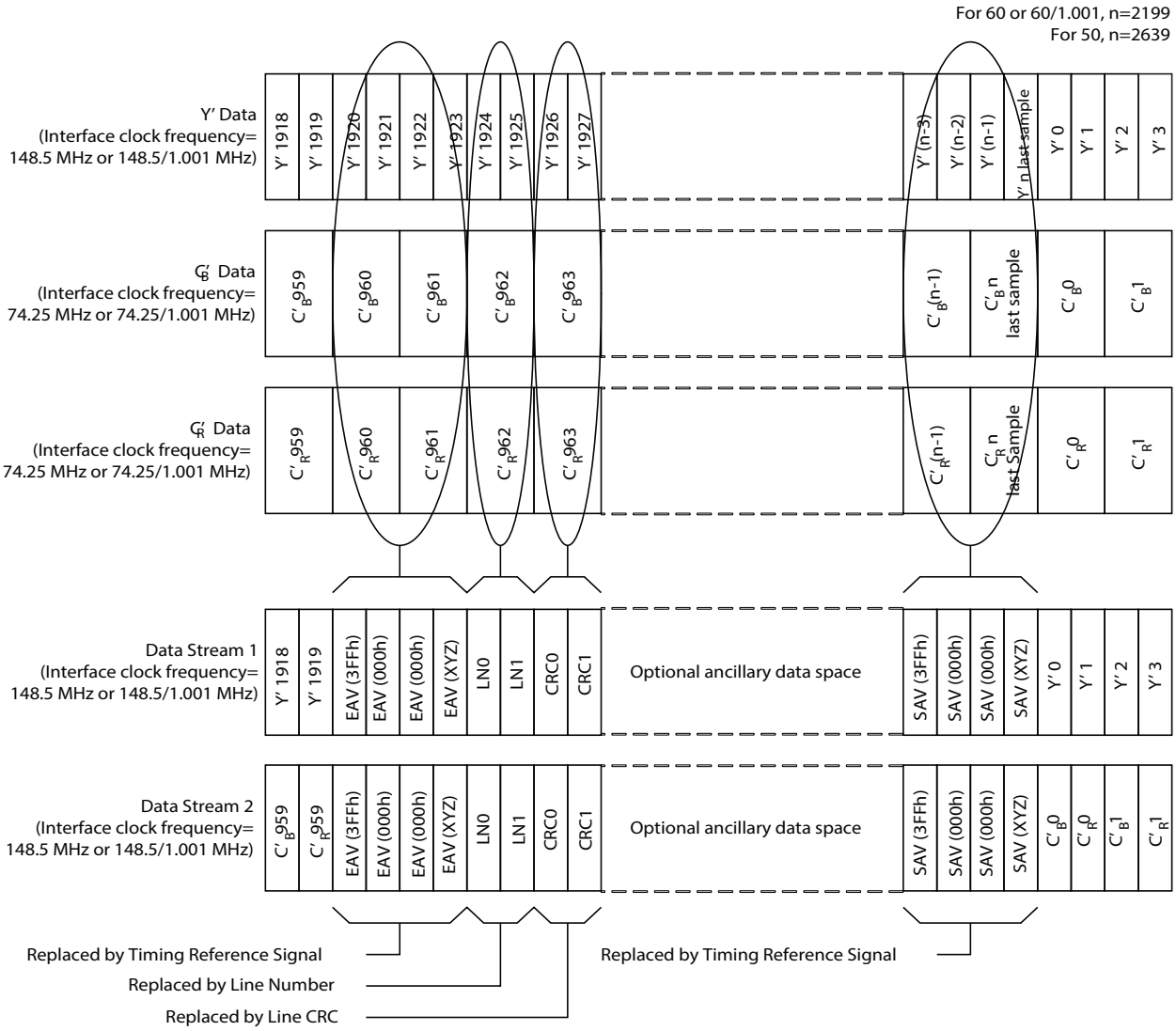


Figure 4-11: 20-bit Mapping Structure for 1920 x 1080 50/60Hz Progressive 4:2:2 (Y'C'BC'R) 8/10-bit Signals

Table 4-5: 1080p Y′C′$_B$C′$_R$ 4:2:0 & 4:2:2 10-bit Bit Structure Mapping

Data Stream	Bit Number									
	9	8	7	6	5	4	3	2	1	0
DS1	Y′[9:0]									
DS2	C′$_B$C′$_R$[9:0]									

Note: For 8-bit systems, the data should be justified to the most significant bit (Y′9 and C′$_B$C′$_R$9), with the two least significant bits (Y′[1:0] and C′$_B$C′$_R$[1:0]) set to zero.

4.3 Video Processing

The GV7700 is designed to carry out data scrambling according to ITU-R BT.1120, and to carry out NRZ to NRZI encoding prior to presentation to the parallel to serial converter.

4.3.1 H:V:F Timing

The GV7700 can automatically detect the video standard and generate all internal timing signals. The total line length, active line length, total number of lines per field/frame and total active lines per field/frame are calculated for the received parallel video.

When DETECT_TRS is LOW, the video standard and timing signals are based on the externally supplied horizontal blanking, vertical blanking, and field identification signals. These signals go to the HIN, VIN, and FIN pins respectively. When DETECT_TRS is HIGH, the video standard timing signals are extracted from the embedded TRS ID words in the parallel input data. Both 8-bit and 10-bit TRS code words are identified by the device.

The GV7700 determines the video standard by timing the horizontal and vertical reference information supplied at the HIN, VIN, and FIN input pins, or contained in the TRS ID words of the received video data. Therefore, full synchronization to the received video standard requires at least one complete video frame.

Once synchronization has been achieved, the GV7700 continues to monitor the received TRS timing or the supplied H, V, and F timing information to maintain synchronization. The GV7700 loses all timing information immediately following loss of H, V, and F.

The timing of these signals is shown in Figure 4-12 to Figure 4-13 below.

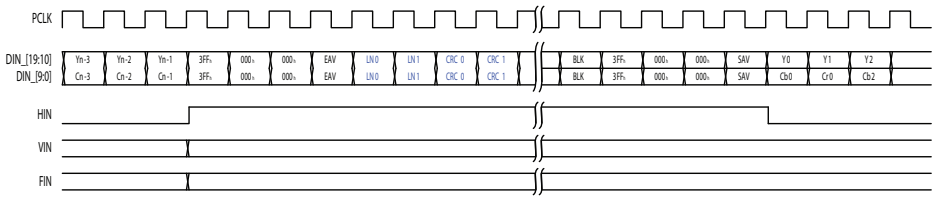


Figure 4-12: H:V:F Input Timing — HD 20-bit Input Mode

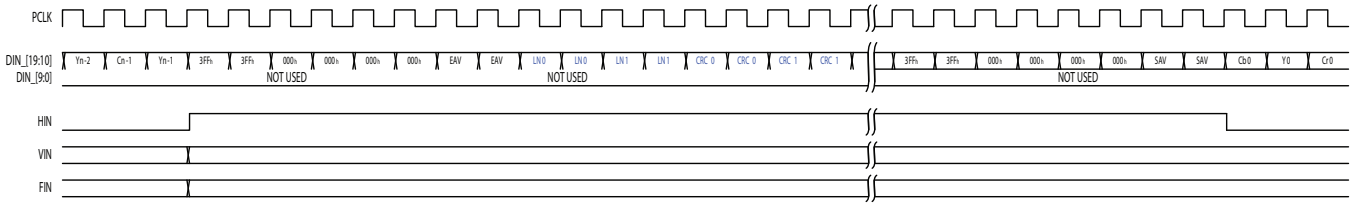


Figure 4-13: H:V:F Input Timing — HD 10-bit Input Mode

4.4 HD-VLC™ Encoder

The GV7700 integrates the High Definition Visually Lossless CODEC (HD-VLC) encoder for extended reach video transmission. When used in conjunction with the GV7704 HD-VLC Quad Receiver, HD video transmission can be extended significantly over existing HD serial digital video systems. HD-VLC is based on a simple visually lossless implementation of the Dirac compression tool kit. The visually lossless encoder is used to reduce the video bandwidth, using a very low latency mode, from a transmission rate of 1.485Gb/s (HD-SDI) to 270Mb/s (SD-SDI).

At a data rate of 270Mb/s, the serial digital encoded HD video can be transmitted over longer runs of coaxial cable. Table 4-6 below shows a comparison of cable distances between HD video transmission at 1.485Gb/s and HD-VLC encoded at 270Mb/s for various common coaxial cable types.

Table 4-6: Cable Reach for Various Cable Types (In Meters)

Cable Type	HD-VLC: 270Mb/s (m)	HD-VLC: 540Mb/s (m)	HD-SDI: 1.485Gb/s (m)	3G-SDI: 2.97Gb/s (m)
Belden 1694A / Canare L-4.5CHD	710	400	230	80
Belden 543945	550	300	150	50
KW-Link SYV 75-5	500	275	140	50
Canare L-3C2V	300	160	95	30
KW-Link SYV 75-3	300	160	80	30

Note: These values apply for new, properly terminated cables. Actual performance may vary.

Note: Longer cable reach performance at both 3G and 540M is possible; up to 100m at 3G and 400m at 540M can be achieved using Belden 543945. However, GV7704 lock times can increase significantly at these cable ranges, and may exceed the lock time requirements of the intended application.

After transmission over the coaxial cable, the 270Mb/s serial data is recovered using the GV7704 HD-VLC Quad Receiver and the data decoded back to the native HD format. The encoding and decoding process has a total latency of 12-14 HD lines, which makes the CODEC ideal for low latency real-time applications. Table 4-7 below shows the total encode/decode latency through the GV7700 and the GV7704.

Table 4-7: Encode and Decode Total Latency (GV7700 + GV7704)

Video Format	Delay (µs)	Delay (HD/3G Lines)
1080p25	422.2	11.9
1080p29.97	368.8	12.4
1080p30	368.4	12.4
720p25	635.1	11.9
720p29.97	546.6	12.2
720p30	546.6	12.2
720p50	368.6	13.8
720p59.94	324.2	14.5
720p60	324.2	14.5
1080p60	184.2	12.4
1080p59.94	184.4	12.4
1080p50	211.1	11.9

The HD-VLC encoder can be enabled by setting the HDVLC_EN input pin HIGH. When this pin is set HIGH, the GV7700 will output HD encoded video at 270Mb/s and 3G encoded video at 540Mb/s. Configuration pins should be set prior to device reset. The 270Mb/s data stream uses the same timing and frame structure as Standard Definition SDI (SD-SDI), and can be monitored using standard SD-SDI test equipment to check signal integrity. However, the data contained within the active picture area of the SD-SDI stream contains only encoded HD packets. The HD video content can only be viewed after the HD-VLC decoding process.

When the GV7700 is HD-VLC encoding video formats at “true” 30 or 60 frames per second, the 270Mb/s (540Mb/s) serial data output will actually operate at 270x1.001Mb/s (540x1.001Mb/s). This multiplication factor is to account for the fractional increase in the original HD video frame rate. For all other HD frame rates, the GV7700 serial data output will be exactly 270Mb/s (540Mb/s).

4.5 Stream ID Packet Insertion

The GV7700 will always insert Stream ID packets immediately after the CRC1 word of the Y channel if the chip is in Reclocker mode (HDVLC_EN = 0) or immediately after the CRC1 word of the YCbCr multiplexed data if the chip is in HD-VLC compression mode (HDVLC_EN = 1).

The chip will insert the Stream ID packet on the following lines shown in Table 4-8 below.

Table 4-8: Stream ID Line Insertion for Video Standards

Input Video Standard	HDVLC_EN	Output Video Standard	Line Number for Insertion
720p25	0	720p25	8
	1	625i50	7, 320
720p29.97	0	720p29.97	8
	1	525i59.94	11, 274
720p30	0	720p30	8
	1	525i60	11, 274
720p50	0	720p50	8
	1	625i25	7, 320
720p59.94	0	720p59.94	8
	1	525i29.97	11, 274
720p60	0	720p60	8
	1	525i30	11, 274
1080p25	0	1080p25	8
	1	625i25	7, 320
1080p29.97	0	1080p29.97	8
	1	525i29.97	11, 274
1080p30	0	1080p30	8
	1	525i30	11, 274
1080i50	0	1080i50	8, 570
	1	625i25	7, 320
1080i59.94	0	1080i59.94	8, 570
	1	525i29.97	11, 274
1080p60	0	1080p60	8
	1	525i69	11, 274

Table 4-8: Stream ID Line Insertion for Video Standards (Continued)

Input Video Standard	HDVLC_EN	Output Video Standard	Line Number for Insertion
1080p59.94	0	1080p59.94	8
	1	525i59.94	11, 274
1080p50	0	1080p50	8
	1	625i50	7, 320

4.6 Audio Embedding

The GV7700 includes an Audio Multiplexer, which is enabled by setting the AUDIO_EN pin HIGH. The device will embed audio in both HD and HD-VLC encoding modes.

The GV7700 can embed up to four channels of serial digital audio at an audio sampling rate of 32kHz, 44.1kHz, or 48kHz.

4.6.1 Serial Audio Data Inputs

The GV7700 supports the insertion of up to 4 channels of embedded audio, in one audio group according to SMPTE ST 299. When in HD-VLC mode (HDVLC_EN = 1), the audio data packets will be inserted in the YCbCr multiplexed data. When HD-VLC encoding is disabled (HDVLC_EN = 0), the audio data packets will be inserted in the C channel of the HD signal as per SMPTE ST 299.

The four audio channels must be input as 2-channel pairs, timed to a serial bit clock (ACLK) at a frequency of 64*f_S, and a word clock (WCLK) at a frequency of f_S, where f_S can be 32kHz, 44.1kHz, or 48kHz. The serial audio input format must conform to I^2S.

The serial audio input signals and WCLK input signals enter the device on the rising edge of ACLK as shown in Figure 4-14.

The audio sampling frequency can be programmed from the host interface by writing to the AUDIO_SAMPLING_FREQ bits in register 109. See Table 4-9 below.

Table 4-9: Audio Sampling Frequency Selection

AUDIO_SAMPLING_FREQ	Input Audio Sampling Rate
00	48kHz
01	44.1kHz
10	32kHz