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GV7704

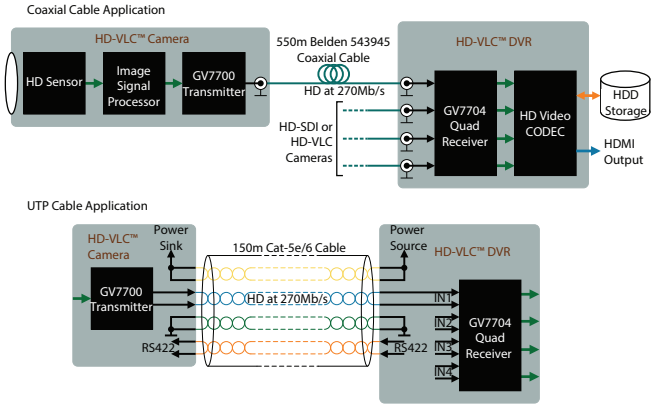
Quad HD-VLC™ Receiver

Key Features

- Quad channel serial digital video receiver for HD and 3G video surveillance and HDcctv applications
- Quad rate operation: 270Mb/s, 540Mb/s, 1.485Gb/s, and 2.97Gb/s
- Supports HDcctv 1.0, HD-SDI (ST 292), 3G-SDI (ST 424), and SD-SDI (ST 259)*
- Four independent receiver channels with high performance cable equalization, with support for 50/75Ω coaxial and twisted pair cable transmission
- Integrated High Definition Visually Lossless CODEC (HD-VLC™) for extended cable reach:
  - HD over 550m of Belden 543945 CCTV coax at 270Mb/s
  - Full HD over 300m of Belden 543945 CCTV coax at 540Mb/s
  - HD over 150m of Cat-5e/6 UTP cable at 270Mb/s
- Serial digital loop-though output per channel
- Integrated audio de-embedder for the extraction of up to 4 channels of I^2S serial digital audio at 32kHz, 44.1kHz and 48kHz sample rates, per video channel
- Supports both 720p and 1080p HD formats:
  - Full HD: 1080p50/59.94/60fps
  - HD: 1080p25/29.97/30fps
  - HD: 720p25/29.97/30/50/59.94/60fps
- Four 8/10-bit BT.1120 compliant output video interfaces, with embedded TRS and external HVF timing outputs
- Automatic independent detection of HD-SDI and HD-VLC video input data streams per channel
- Downstream ancillary data detection and extraction
- Automatic HDcctv Stream ID detection
- 4-wire Gennum Serial Peripheral Interface (GSPI 2.0) for external host command and control
- JTAG test interface
- 1.2V core voltage power supplies
- 1.8V digital I/O power supply
- Small footprint 169-BGA (11mm x 11mm)
- Low power operation, typically 810mW
- Wide operating temperature range: -20°C to + 85°C
- Pb-free and RoHS compliant

Applications

- Digital video recorders (DVR)
- Video servers
- Video multiplexers
- Video PC capture cards
- HDcctv peripherals



Description

The GV7704 is a quad channel serial digital video receiver for High Definition component video. With integrated high performance cable equalizer technology, the GV7704 is capable of receiving compressed video at 270Mb/s or 540Mb/s, or uncompressed at 1.485Gb/s or 2.97Gb/s, over 75Ω coaxial cable, or differentially over a 100Ω twisted pair cable.

The GV7704 integrates the High Definition Visually Lossless CODEC (HD-VLC™) technology, which has been developed specifically to reduce the transmission data rate of HD video over both coaxial and unshielded twisted pair (UTP) cable. This is achieved by encoding the HD video, normally transmitted at a serial data rate of 1.485Gb/s, to the same rate as Standard Definition (SD) video, at 270Mb/s serial data rate.

At 270Mb/s, the effect of cable loss is greatly reduced, resulting in much longer cable transmission. For 75Ω

coaxial cable, cable reach can be extended up to 3x the normal reach when transmitting encoded HD at 270Mb/s. In typical video over coaxial installations, cable distances of up to 550m are possible.

Similarly, a 2.97Gb/s 3G signal can be transmitted at 540Mb/s using HD-VLC.

The GV7704 can also be configured to receive HD and 3G video over UTP cable, such as Cat-5e and Cat-6 cable, when HD-VLC encoded at 270Mb/s and 540Mb/s, respectively.

The device supports the reception of both 8-bit and 10-bit per pixel YCbCr 4:2:2 BT.1120 component digital video. A single 10-bit wide parallel digital video output bus per channel is provided, with associated pixel clock and timing signal outputs. The GV7704 supports direct interfacing of HD video formats conforming to ITU-R BT.709 and BT.1120-6 for 1125-line formats, and SMPTE ST 296 for 750-line formats.

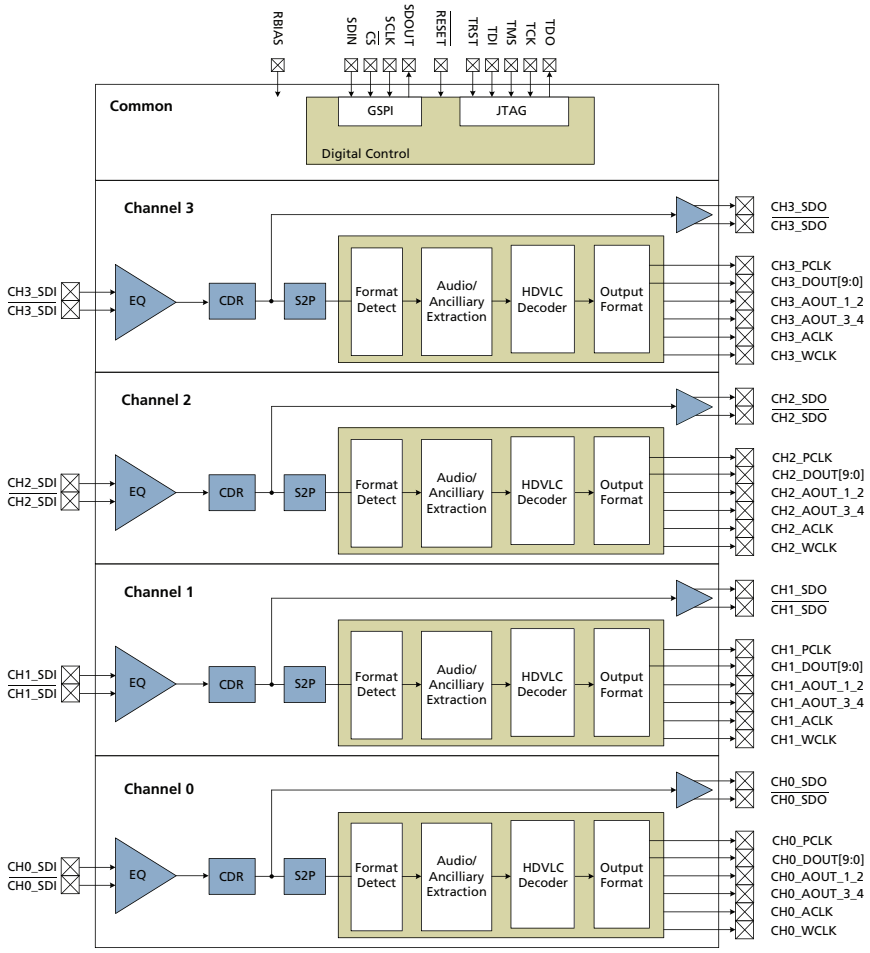
The GV7704 supports the extraction of ancillary data from the horizontal blanking of the input video data stream. Ancillary data packets can be accessed via the GSPI, allowing downstream communication from the video source to sink device. The GV7704 recognizes data packets formatted in compliance with the HDcctv 2.0 communications protocol.

The GV7704 features an audio de-embedding core, which provides the extraction of up to 4 channels of I^2S serial digital audio from the ancillary data space of the input video data stream. The audio de-embedding core supports 32kHz, 44.1kHz, and 48kHz sample rates.

Packaged in a space saving 169 ball 11 x 11mm BGA, the GV7704 is ideal for high density, multi-channel video recorder architectures. Typically requiring only 810mW of power, the device does not require any special heat sinking or air flow, reducing the over cost of HD DVR designs.

**Frame structure with encoded HD only. Does not support SD/D1 video.*

Functional Block Diagram



Revision History

Version	ECO	PCN	Date	Description
5	031801	—	June 2016	Table 2-3: AC Electrical Characteristics VDD18_A, VDD18_D = 1.8V±5% and T_A = -20°C to +85°C unless otherwise stated was updated
4	029083	—	March 2016	Updated to Final Data Sheet. Updated Table 2-3 with added Input Jitter Tolerance and changes to values in Rise/Fall Time, Rise/Fall Time Matching, and Output Total Jitter.
3	027518	—	September 2015	Updated to Preliminary Data Sheet. Updated Section 2.1, Section 2.2, Section 2.3, Section 4., and Figure 6-2. Added Figure 6-3. Various updates throughout document.
2	027065	—	July 2015	Updated cable reach values. Updated Table 2-2 and Table 2-3.
1	024435	—	March 2015	Updated Section 2.2, Section 2.3, Section 5., and Figure 6-1. Added Section 3., Section 4.11 and Section 4.12. Various updates throughout document.
0	021239	—	October 2014	New Document

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1. Pin Out

1.1 GV7704 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	CH3_SDI	$\overline{\text{CH3\_SDI}}$	GND	CH3_SDO	TCK	CH3_WCLK	CH2_WCLK	CH3_HOUT	CH3_PCLK	CH3_DOUT_5	CH3_DOUT_3	CH3_DOUT_1	CH3_DOUT_0
B	GND	GND	VDD18_A	$\overline{\text{CH3\_SDO}}$	TMS	CH3_ACLK	CH2_ACLK	CH3_VOUT	CH3_DOUT_8	CH3_DOUT_6	CH3_DOUT_4	CH3_DOUT_2	CH2_VOUT
C	N/C	N/C	VDD18_A	TDI	TDO	CH3_AOUT_1_2	CH2_AOUT_1_2	CH3_FOUT	CH3_DOUT_9	CH3_DOUT_7	CH2_HOUT	CH2_FOUT	CH2_PCLK
D	CH2_SDI	$\overline{\text{CH2\_SDI}}$	GND	TRST	EXT_FW	CH3_AOUT_3_4	CH2_AOUT_3_4	GND	GND	GND	CH2_DOUT_9	CH2_DOUT_8	CH2_DOUT_7
E	GND	GND	VDD18_A	VDD12_A	RSVD	GND	VDD18_D	VDD18_D	GND	GND	CH2_DOUT_6	CH2_DOUT_5	CH2_DOUT_4
F	CH2_SDO	$\overline{\text{CH2\_SDO}}$	VDD18_A	VDD12_A	GND	VDD12_D	VDD12_D	VDD12_D	VDD18_D	GND	CH2_DOUT_3	CH2_DOUT_2	CH2_DOUT_1
G	GND	GND	VDD18_A	VDD12_A	GND	VDD12_D	VDD12_D	VDD12_D	VDD18_D	GND	GND	CH1_HOUT	CH2_DOUT_0
H	CH1_SDO	$\overline{\text{CH1\_SDO}}$	VDD18_A	VDD12_A	GND	VDD12_D	VDD12_D	VDD12_D	VDD18_D	GND	CH1_VOUT	CH1_FOUT	CH1_PCLK
J	GND	GND	VDD18_A	VDD12_A	GND	GND	VDD18_D	VDD18_D	GND	GND	CH1_DOUT_9	CH1_DOUT_8	CH1_DOUT_7
K	CH1_SDI	$\overline{\text{CH1\_SDI}}$	GND	$\overline{\text{RESET}}$	RSVD	CH0_WCLK	CH1_WCLK	GND	GND	GND	CH1_DOUT_6	CH1_DOUT_5	CH1_DOUT_4
L	RBIAS	VDD18_A	GND	SDIN	SDOUT	CH0_ACLK	CH1_ACLK	CH0_DOUT_2	CH0_DOUT_5	CH0_DOUT_8	CH1_DOUT_3	CH1_DOUT_2	CH1_DOUT_1
M	GND	GND	VDD18_A	$\overline{\text{CH0\_SDO}}$	$\overline{\text{CS}}$	CH0_AOUT_1_2	CH1_AOUT_1_2	CH0_DOUT_1	CH0_DOUT_4	CH0_DOUT_7	CH0_DOUT_9	CH0_VOUT	CH1_DOUT_0
N	CH0_SDI	$\overline{\text{CH0\_SDI}}$	GND	CH0_SDO	SCLK	CH0_AOUT_3_4	CH1_AOUT_3_4	CH0_DOUT_0	CH0_DOUT_3	CH0_DOUT_6	CH0_PCLK	CH0_HOUT	CH0_FOUT

Figure 1-1: GV7704 Pin Out

1.2 Pin Descriptions

Table 1-1: GV7704 Pin Descriptions

Pin Number	Name	Type	Description
Analog High-Speed Inputs			
N1, N2	CH0_SDI, $\overline{\text{CH0\_SDI}}$	Analog High-Speed Input	Differential high-speed data input 0. (75Ω nominal input impedance)
K1, K2	CH1_SDI, $\overline{\text{CH1\_SDI}}$	Analog High-Speed Input	Differential high-speed data input 1. (75Ω nominal input impedance)
D1, D2	CH2_SDI, $\overline{\text{CH2\_SDI}}$	Analog High-Speed Input	Differential high-speed data input 2. (75Ω nominal input impedance)
A1, A2	CH3_SDI, $\overline{\text{CH3\_SDI}}$	Analog High-Speed Input	Differential high-speed data input 3. (75Ω nominal input impedance)
Analog High-Speed Outputs			
N4, M4	CH0_SDO, $\overline{\text{CH0\_SDO}}$	Analog High-Speed Output	Differential high-speed test output 0. (75Ω nominal output impedance)
H1, H2	CH1_SDO, $\overline{\text{CH1\_SDO}}$	Analog High-Speed Output	Differential high-speed test output 1. (75Ω nominal output impedance)
F1, F2	CH2_SDO, $\overline{\text{CH2\_SDO}}$	Analog High-Speed Output	Differential high-speed test output 2. (75Ω nominal output impedance)
A4, B4	CH3_SDO, $\overline{\text{CH3\_SDO}}$	Analog High-Speed Output	Differential high-speed test output 3. (75Ω nominal output impedance)
Analog Bias			
L1	RBIAS	Input/Output	External 10kΩ resistor for bias reference. Connect the resistor to ground.
Digital Video Outputs			
L8, L9, L10, M8, M9, M10, M11, N8, N9, N10	CH0_DOUT_[9:0]	Output	Parallel digital video output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
N12	CH0_HOUT	Output	Horizontal blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
M12	CH0_VOUT	Output	Vertical blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
N13	CH0_FOUT	Output	Frame indication output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
N11	CH0_PCLK	Output	Pixel clock output (148.5MHz or 148.5/1.001 MHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
J[11:13], K[11:13], L[11:13], M13	CH1_DOUT_[9:0]	Output	Parallel digital video output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
G12	CH1_HOUT	Output	Horizontal blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
H11	CH1_VOUT	Output	Vertical blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
H12	CH1_FOUT	Output	Frame indication output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
H13	CH1_PCLK	Output	Pixel clock output (148.5MHz or 148.5/1.001 MHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
D[11:13], E[11:13], F[11:13], G13	CH2_DOUT_[9:0]	Output	Parallel digital video output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
C11	CH2_HOUT	Output	Horizontal blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
B13	CH2_VOUT	Output	Vertical blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
C12	CH2_FOUT	Output	Frame indication output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
C13	CH2_PCLK	Output	Pixel clock output (148.5MHz or 148.5/1.001 MHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
A[10:13], B[9:12], C9, C10	CH3_DOUT_[9:0]	Output	Parallel digital video output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
A8	CH3_HOUT	Output	Horizontal blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
B8	CH3_VOUT	Output	Vertical blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
C8	CH3_FOUT	Output	Frame indication output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
A9	CH3_PCLK	Output	Pixel clock output (148.5MHz or 148.5/1.001 MHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
Digital Audio Outputs			
K6	CH0_WCLK	Output	Channel 0 word clock (32kHz, 44.1kHz, or 48kHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
L6	CH0_ACLK	Output	Channel 0 I^2S Audio clock (64 x word clock). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
M6	CH0_AOUT_1_2	Output	Channel 0 I^2S Audio output 1 & 2. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
N6	CH0_AOUT_3_4	Output	Channel 0 I^2S Audio output 3 & 4. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
K7	CH1_WCLK	Output	Channel 1 word clock (32kHz, 44.1kHz, or 48kHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
L7	CH1_ACLK	Output	Channel 1 I^2S Audio clock (64 x word clock). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
M7	CH1_AOUT_1_2	Output	Channel 1 I^2S Audio output 1 & 2. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
N7	CH1_AOUT_3_4	Output	Channel 1 I^2S Audio output 3 & 4. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
A7	CH2_WCLK	Output	Channel 2 word clock (32kHz, 44.1kHz, or 48kHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
B7	CH2_ACLK	Output	Channel 2 I^2S Audio clock (64 x word clock). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
C7	CH2_AOUT_1_2	Output	Channel 2 I^2S Audio output 1 & 2. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
D7	CH2_AOUT_3_4	Output	Channel 2 I^2S Audio output 3 & 4. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
A6	CH3_WCLK	Output	Channel 3 word clock (32kHz, 44.1kHz, or 48kHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
B6	CH3_ACLK	Output	Channel 3 I^2S Audio clock (64 x word clock). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
C6	CH3_AOUT_1_2	Output	Channel 3 I^2S Audio output 1 & 2. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
D6	CH3_AOUT_3_4	Output	Channel 3 I^2S Audio output 3 & 4. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
JTAG Interface			
B5	TMS	Input	Dedicated JTAG pin – Test Mode Select. This pin is used to control the operation of the JTAG test. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin may be left floating.
C4	TDI	Input	Dedicated JTAG pin – Test data input. This pin is used to shift JTAG test data into the device. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin may be left floating.
C5	TDO	Output	Dedicated JTAG pin – Test data output. This pin is used to shift results from the device.
A5	TCK	Input	Dedicated JTAG pin – Serial data clock signal. This pin is the JTAG clock. Schmitt Trigger Input. If JTAG is not used this pin must be pulled LOW.
D4	TRST	Input	Dedicated JTAG pin – Test Reset. When set LOW, the JTAG logic will be reset. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin must be pulled LOW.
General I/O and Host Interface			
K4	$\overline{\text{RESET}}$	Input	Digital active–low reset input. Used to reset the internal. operating conditions to default settings. Schmitt Trigger Input.
M5	$\overline{\text{CS}}$	Input	Used to initiate and terminate GSPI commands. Active-low.
L4	SDIN	Input	Serial input data, clocked in on the rising edge of SCLK.
L5	SDOUT	Output	Serial data output. Only used in GSPI mode. Clocked out on the falling edge of SCLK. Drive strength may be adjusted using register GSPI_SDOUT_DRV_STRENGTH_SEL_REG.
N5	SCLK	Input	Serial clock. The rising edge is used to latch the SDIN bits and the falling edge to drive SDOUT bits.
D5	EXT_FW	Input	External firmware loading control: When HIGH, indicates to the GV7704 that the host will download firmware to the GV7704. When LOW, indicates to the GV7704 to boot with internal firmware.

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
Supply Pins			
B3, C3, E3, F3, G3, H3, J3, L2, M3	VDD18_A	Power	Analog 1.8V Power Supply. Connect to 1.8V.
E7, E8, F9, G9, H9, J7, J8	VDD18_D	Power	Digital 1.8V Power Supply. Connect to 1.8V.
E4, F4, G4, H4, J4	VDD12_A	Power	Analog 1.2V Power Supply. Connect to 1.2V.
F6, F7, F8, G6, G7, G8, H6, H7, H8	VDD12_D	Power	Digital 1.2V Power Supply. Connect to 1.2V.
A3, B1, B2, D3, D8, D9, D10, E1, E2, E6, E9, E10, F5, F10, G1, G2, G5, G10, G11, H5, H10, J1, J2, J5, J6, J9, J10, K3, K8, K9, K10, L3, M1, M2, N3	GND	Power	Connect to GND.
C1, C2	N/C	—	Do not Connect.
E5, K5	RSVD	—	Connect to GND.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
1.8V I/O and Analog Supply Voltage	–0.5V to +2.5V DC
1.2V Analog and Core Supply Voltage	–0.3V to +1.5V DC
DC Input Voltage, VIN (Not to exceed 2.5V)	–0.5V to (VDD18 + 0.5V)
DC Output Voltage, VOUT (Not to exceed 2.5V)	–0.5V to (VDD18 + 0.5V)
Input ESD Voltage (HBM)	2kV
Input ESD Voltage (CDM)	500V
Storage Temperature Range (T_S)	-50°C to 125°C
Operating Temperature Range (T_A)	-20°C to 85°C
Solder Reflow Temperature (4s)	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC and DC Electrical Characteristics is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

T_A = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
+1.2V Supply Current	I_{1V2}	270Mb/s	—	172	—	mA	
		1.485Gb/s	—	250	—	mA	
+1.8V Supply Current	I_{1V8}	270Mb/s	—	440	—	mA	
		1.485Gb/s	—	456	—	mA	
+1.8V Power Supply Range	VDD18	At the device pin (nominal ±5%)	1.71	1.8	1.89	V	
+1.2V Power Supply Range	VDD12	At the device pin (nominal ±5%)	1.14	1.2	1.26	V	
External RBIAS Resistor	—		9.9	10	10.1	kΩ	
Power Supply Noise Mask +1.2V	—	0-200kHz	—	—	100	mV_{pp}	1
	—	200kHz to 1MHz	—	—	100	mV_{pp}	1
	—	>1MHz	—	—	100	mV_{pp}	1
Power Supply Noise Mask +1.8V	—	0 to 200kHz	—	—	10	mV_{pp}	1
	—	200kHz to 1MHz	—	—	30	mV_{pp}	1
	—	>1MHz	—	—	100	mV_{pp}	1
Total Power Consumption	P_{total}	270Mb/s, All Cable Drivers Enabled	—	950	1030	mW	
		270Mb/s, All Cable Drivers Disabled	—	810	910	mW	
		540Mb/s All Cable Drivers Enabled	—	1065	1180	mW	
		540Mb/s All Cable Drivers Disabled	—	925	1040	mW	
		1.485Gb/s, All Cable Drivers Enabled	—	1070	1160	mW	
		1.485Gb/s, All Cable Drivers Disabled	—	900	1020	mW	
		2.97Gb/s, All Cable Drivers Enabled	—	1200	1370	mW	
		2.97Gb/s, All Cable Drivers Disabled	—	1030	1200	mW	
Digital Logic Input	V_{IL}	Input LOW	-0.3	—	0.63	V	
	V_{IH}	Input HIGH	1.17	—	1.89	V	

Table 2-2: DC Electrical Characteristics (Continued)

T_A = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Digital Logic Output	V_{OL}	Output LOW	—	—	0.45	V	2
	V_{OH}	Output HIGH	1.35	—	—	V	2
	C_{LOAD}	148.5MHz	—	—	12	pF	

Notes:

1. Using recommended supply decoupling. See Figure 6-1: Typical Application Circuit (Part 1).
2. All digital outputs.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VDD18_A, VDD18_D = 1.8V±5% and T_A = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Conditions							
Input Return Loss	—	1MHz to 5MHz	23	—	—	dB	
	—	5MHz to 1.485GHz	12	—	—	dB	
	—	1.485GHz to 2.25GHz	10	—	—	dB	
Input Jitter Tolerance	—	Data rate = 270Mb/s	0.29	—	—	UI	
	—	Data rate = 540Mb/s	0.29	—	—	UI	
	—	Data rate = 1.485Gb/s	0.20	—	—	UI	
	—	Data rate = 2.97Gb/s	0.20	—	—	UI	
Clock and Data Output Conditions							
Output PCLK Clock Frequency	f_{PCLK}		—	148.5 or 148.5/1.001	—	MHz	
SDO Output Impedance	—	75Ω single-ended	66	75	84	Ω	
	—	100Ω differential	88	100	112	Ω	
Output Return loss	—	1MHz to 5MHz	25	—	—	dB	
	—	5MHz to 1.485GHz	6	—	—	dB	
	—	1.485GHz to 2.25GHz	6	—	—	dB	
Amplitude	—	75Ω single-ended	0.36	0.8	0.9	V_{pp}	
	—	100Ω differential	0.36	0.8	0.9	V_{ppd}	

Table 2-3: AC Electrical Characteristics (Continued)

VDD18_A, VDD18_D = 1.8V±5% and T_A = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Rise/Fall Time	—	100Ω differential 20% - 80%	—	85	95	ps	
	—	75Ω single-ended 20% - 80%	—	102	150	ps	
Rise/Fall Time Mismatch	—	20% - 80%	—	—	50	ps	
Overshoot	—		—	—	10	%	
Output Total Jitter	—	Data rate = 270Mb/s	—	0.08	—	UI_{pp}	
	—	Data rate = 540Mb/s	—	0.1	—	UI_{pp}	
	—	Data rate = 1.485Gb/s	—	0.12	—	UI_{pp}	
	—	Data rate = 2.97Gb/s	—	0.17	—	UI_{pp}	
GSPI Digital Control							
GSPI Read/Write Clock Frequency	—		—	—	55	MHz	
Reset Time	—		10	—	—	ms	
Register Access Time	—		—	—	300	ns	

3. Input/Output Circuits

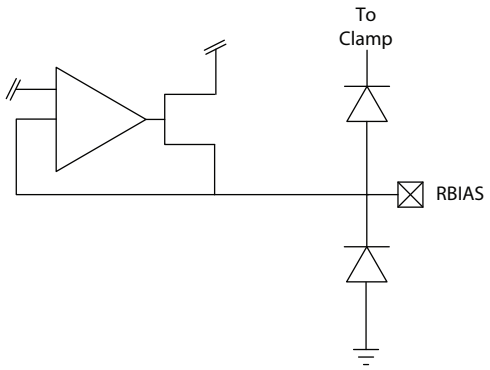

Figure 3-1: RBIAS

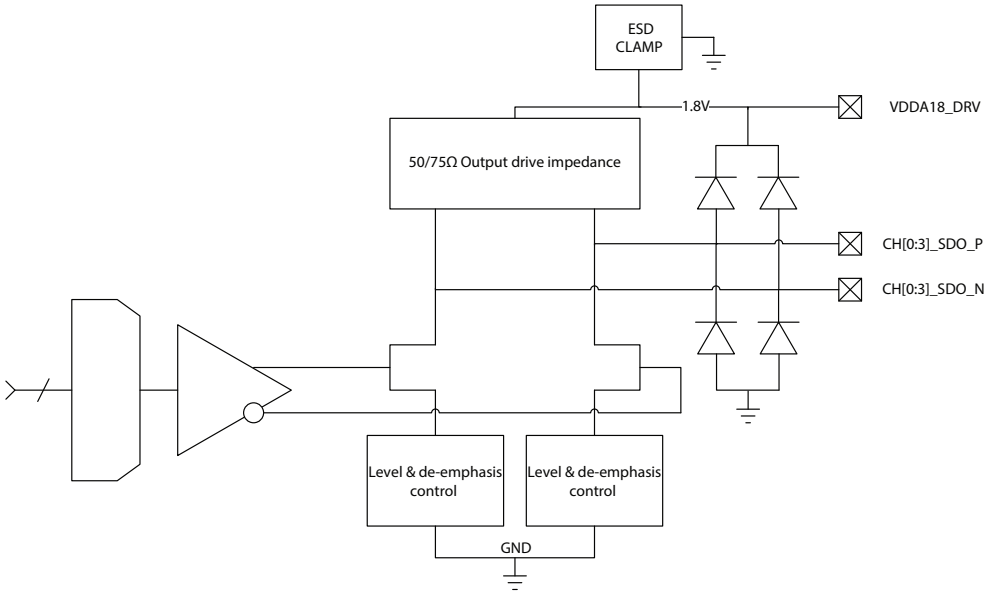

Figure 3-2: Serial Output Driver

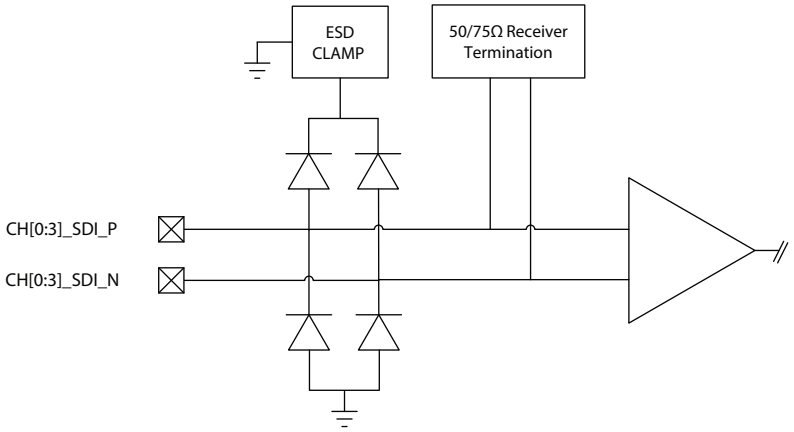

Figure 3-3: Serial Input Receiver

4. Detailed Description

4.1 Functional Overview

The GV7704 is a low cost, quad channel HD-VLC receiver of compressed or uncompressed high-definition video. With integrated cable equalizer technology, the GV7704 is capable of receiving compressed video at 270Mb/s or 540Mb/s, or uncompressed video at 1.485Gb/s or 2.97Gb/s over 75Ω coaxial cable. Compressed signals can also be received differentially over 100Ω twisted pair cable.

The High Definition Visually Lossless CODEC (HD-VLC™) technology is integrated in order to reduce the transmission data rate of HD video over both coaxial and unshielded twisted pair (UTP) cable. This is achieved by encoding the HD-SDI video, normally transmitted at a serial data rate of 1.485Gb/s, to the same rate as Standard Definition (SD-SDI) video, at 270Mb/s serial data rate. This provides extended cable reach for HD video up to 550m over Belden 543945 CCTV coax or 150m over Cat-5e/6 UTP cable. Similarly, 3G-SDI normally transmitted at 2.97Gb/s can be encoded down to 540Mb/s.

The GV7704 features an audio de-embedding core, which provides the extraction of up to 4 channels of I^2S serial digital audio from the ancillary data space of the input video data stream. The audio de-embedding core supports 32kHz, 44.1kHz and 48kHz sample rates.

The device supports the reception of both 8-bit and 10-bit per pixel YCbCr 4:2:2 BT.1120 component digital video. A single 10-bit wide parallel digital video output bus per channel is provided, with associated pixel clock and H/V/F timing signal inputs.

The GV7704 supports the extraction of ancillary data from the horizontal blanking of the input video data stream. Ancillary data packets can be accessed via the GSPI, allowing downstream communication from the video source to sink device. The GV7704 recognizes data packets formatted in compliance with the HDcctv 2.0 communications protocol.

The device includes a 4-wire Gennum Serial Peripheral Interface (GSPI 2.0) for external host command and control. All read or write access to the GV7704 is initiated and terminated by the application host processor. The host interface is provided to allow optional configuration of some of the functions and operating modes of the GV7704.

4.2 Serial Digital Inputs

The GV7704 can accept up to four separate channels of serial digital input signals compliant with ITU-R BT.709, and ITU-R BT.1120-6. The four differential input channels are CH0_SDI/$\overline{\text{CH0\_SDI}}$, CH1_SDI/$\overline{\text{CH1\_SDI}}$, CH2_SDI/$\overline{\text{CH2\_SDI}}$ and CH3_SDI/$\overline{\text{CH3\_SDI}}$.

The GV7704 integrates adaptive 75Ω coaxial cable equalizer technology which is capable of >50dB for HD-VLC encoded input signals and >35dB for HD uncompressed signals.

Table 4-1: Typical Cable Length Performance

Data Rate	Belden 543945 CCTV Coaxial	Cat-5e/6 UTP
HD data @ 1.485Gb/s	150m	N/A
HD-VLC encoded data @ 270Mb/s	550m	150m
3G data @ 2.97Gb/s	50m	N/A
HD-VLC encoded data @ 540Mb/s	300m	75m*

*Theoretical

The Serial Data Signal may be connected to the input pins of any of the four channels in either a differential or single ended configuration. Only AC coupling of the inputs is supported, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

Note: The serial data output should be disabled to achieve maximum SDI cable reach.

4.2.1 Input Termination Selection

Each of the four channels can be individually configured to work in either 50Ω or 75Ω input termination. Please refer to Register Map for details.

4.2.2 Automatic Signal Rate Detection

The device is able to automatically detect the rate of the incoming video signal. There are four data rates which are supported:

- HD-VLC encoded 270Mb/s (including 270x1.001Mb/s)
- HD-VLC encoded 540Mb/s (including 540x1.001Mb/s)
- HD-SDI 1.485Gb/s (including 1.485/1.001Gb/s)
- 3G-SDI 2.97Gb/s (including 2.97/1.001Gb/s)

The detected rate is indicated by bits SD_HDB, THREEG_HDB, and OUT_THREEG_HDB in register GEN_VIDEO_CFG_0_REG which specify whether the incoming signal is HD-VLC encoded (270Mb/s), HD-VLC encoded (540Mb/s), HD (1.485Gb/s), or 3G (2.97Gb/s). Table 4-2 describes how these three bits are used in combination to indicate the input signal rate.

Table 4-2: Input Rate Detection

Rate	GEN_VIDEO_CFG_0_REG		
	SD_HDB	THREEG_HDB	OUT_THREEG_HDB
HD 1.485Gb/s	0	0	0
HD-VLC 270Mb/s	1	0	0
3G 2.97Gb/s	0	1	1
HD-VLC 540MB/s	1	0	1

4.3 Serial Digital Outputs

The GV7704's serial data output pins, SDO and $\overline{\text{SDO}}$, provide complementary outputs, each capable of driving at least 800mV into a 75Ω single-ended load.

Compliance with all requirements defined in Section 4.3.1 through Section 4.3.2 is guaranteed when measured across a 75Ω terminated load at the output of 1m of Belden 543945 cable, including the effects of the BNC and coaxial cable connection, except where otherwise stated.

Figure 4-1 illustrates this requirement.

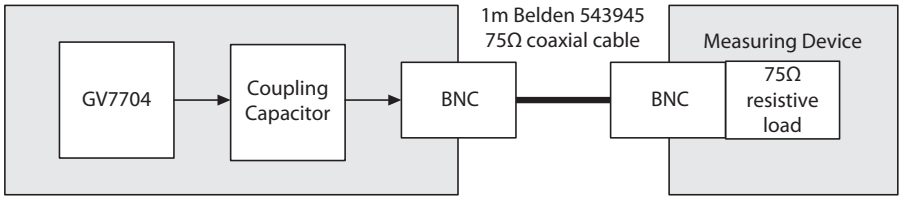

Figure 4-1: BNC and Coaxial Cable Connection

4.3.1 Output Signal Interface Levels

The Serial Data Output signals (SDO and $\overline{\text{SDO}}$ pins), of the device meet the amplitude requirements as defined in ITU-R BT.656 and BT.1120 for an unbalanced generator (single-ended).

These requirements are met across all ambient temperature and power supply operating conditions described in 2. Electrical Characteristics.

4.3.2 Serial Data Output Signal

The device supports two output termination modes (75Ω and 50Ω). The user can program the SDO_50_EN_REG to make that selection, on a per channel basis. Please refer to Register Map for details.

4.3.2.1 Serial Data Output Signal Procedure

To enable the serial data output, the user must do a series of GSPI write transactions. The order is very important and must be followed exactly. The sequence is as shown below:

1. Write 03 to the POWER_UP_DRIVER_REG
2. Write 01 to the P2S_CLK_EN_REG
3. Write 01 to the TX_WORD_CLK_ENABLE_REG
4. Write 01 to the CDR_TX_CLK_EN_REG
5. Write 01 to the P2S_RSTB_REG
6. Write 09 to the DATALANE_FIFO_CTRL_REG
7. Write 08 to the DATALANE_FIFO_CTRL_REG

Please refer to Section 5. Register Map for detailed register information.

Refer to Section 4.10 for GSPI timing requirements.

Note: The serial data output should be disabled to achieve maximum SDI cable reach.

4.4 Video Functionality

4.4.1 Descrambling and Word Alignment

The GV7704 performs NRZI to NRZ decoding and data descrambling according to ITU-R BT.1120, and word aligns the data to TRS sync words.

The GV7704 carries out descrambling and word alignment to enable the detection of TRS sync words. When two consecutive valid TRS words (SAV and EAV), with the same bit alignment have been detected, the device word-aligns the data to the TRS ID words.

Note: Both 8-bit and 10-bit TRS headers are identified by the device.

4.4.2 HD-VLC Decoding

The GV7704 integrates the High Definition Visually Lossless CODEC (HD-VLC) decoder for extended reach video reception. When used in conjunction with the GV7700 HD-VLC transmitter, HD video transmission can be extended significantly over existing HD serial digital video systems. HD-VLC is based on a simple visually lossless implementation of the Dirac compression tool kit (http://diracvideo.org/) The visually lossless decoder is used to reduce the video bandwidth, using a very low latency mode, from a transmission rate of 1.485Gb/s (HD-SDI) to 270Mb/s (SD-SDI).

At a data rate of 270Mb/s, the serial digital encoded HD video can be transmitted over longer runs of coaxial cable. Table 4-3 below shows a comparison of cable distances between HD video transmission at 1.485Gb/s and HD-VLC encoded at 270Mb/s for various common coaxial cable types.

Table 4-3: Cable Reach for Various Cable Types (In Metres)

Cable Type	HD-VLC: 270Mb/s (m)	HD-VLC: 540Mb/s (m)	HD-SDI: 1.485Gb/s (m)	3G-SDI: 2.97Gb/s (m)
Belden 1694A / Canare L-4.5CHD	710	400	230	80
Belden 543945	550	300	150	50
KW-Link SYV 75-5	500	275	140	50
Canare L-3C2V	300	160	95	30
KW-Link SYV 75-3	300	160	85	30

Note: These values apply for new, properly terminated cables. Actual performance may vary.

Note 1: Longer cable reach performance at both 3G and 540M is possible; up to 100m at 3G and 400m at 540M can be achieved using Belden 543945. However, GV7704 lock times can increase significantly at these cable ranges, and may exceed the lock time requirements of the intended application.

Note 2: The serial data output should be disabled to achieve maximum SDI cable reach.

After transmission over the coaxial cable, the 270Mb/s or 540Mb/s serial data is recovered using the GV7704 and the data is decoded back into the native HD or 3G format. The encoding and decoding process has a total latency of 12-14 HD/3G lines which makes the CODEC ideal for low latency real-time applications. Table 4-4 below shows the total encode/decode latency through the GV7704 and the GV7700.

Table 4-4: Encode and Decode Total Latency (GV7704 + GV7700)

Video Format	Delay (µs)	Delay (HD/3G Lines)
1080p25	422.2	11.9
1080p29.97	368.8	12.4
1080p30	368.4	12.4
1080p50	211.1	11.9
1080p59.94	184.4	12.4
1080p60	184.2	12.4
720p25	635.1	11.9
720p29.97	546.6	12.2
720p30	546.6	12.2
720p50	368.6	13.8
720p59.94	324.2	14.5
720p60	324.2	14.5

The 270Mb/s data stream uses the same timing and frame structure as Standard Definition SDI (SD-SDI), and can be monitored using standard SD-SDI test equipment to check signal integrity. However, the data contained within the active picture area of the

SD-SDI stream contains only encoded HD packets. The HD video content can only be viewed after the HD-VLC decoding process.

When the GV7704 is HD-VLC encoding video formats at “true” 30 or 60 frames per second, the 270Mb/s (540Mb/s) serial data input will actually be incoming at a rate of 270x1.001Mb/s (540x1.001Mb/s). This multiplication factor is to account for the fractional increase in the original HD video frame rate. For all other HD frame rates, the incoming serial data will be exactly 270Mb/s.

4.4.3 High Definition Output Video Format

ITU-R BT.1120 describes the serial and parallel format for 1080-line interlaced and progressive digital video. The field/frame blanking period (V), the line blanking period (H), and the field identification (F), are embedded as digital timing codes (TRS) within the video. After deserialization, a single 10-bit bus carrying the C'B, Y', C'R, Y', etc. data pattern is output on the 10-bit parallel data interface, operating at a pixel clock rate of 148.5MHz or 148.5/1.001MHz.

For 3G formats the parallel interface uses a DDR pixel clock at 148.5MHz or 148.5/1.001MHz.

The following figures show horizontal and vertical timing for 1080-line interlaced systems.

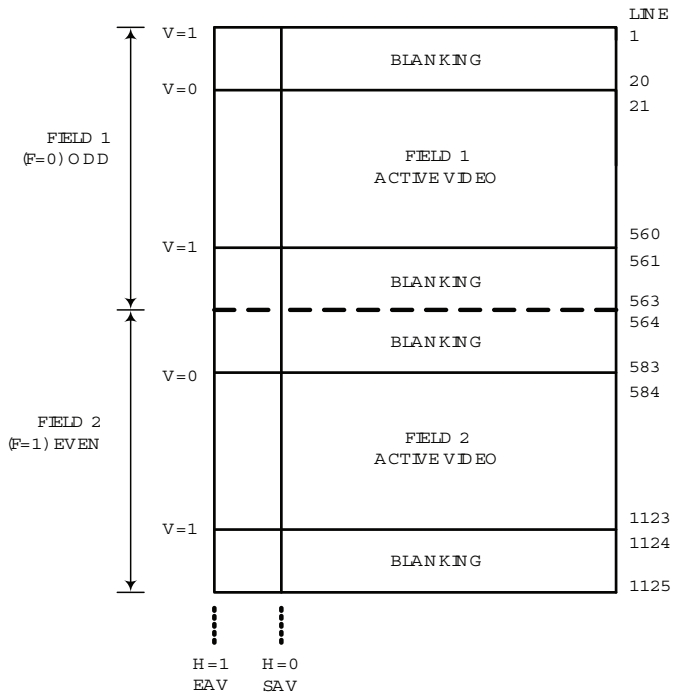

Figure 4-2: Field Timing Relationship for 1080-line Interlaced Systems

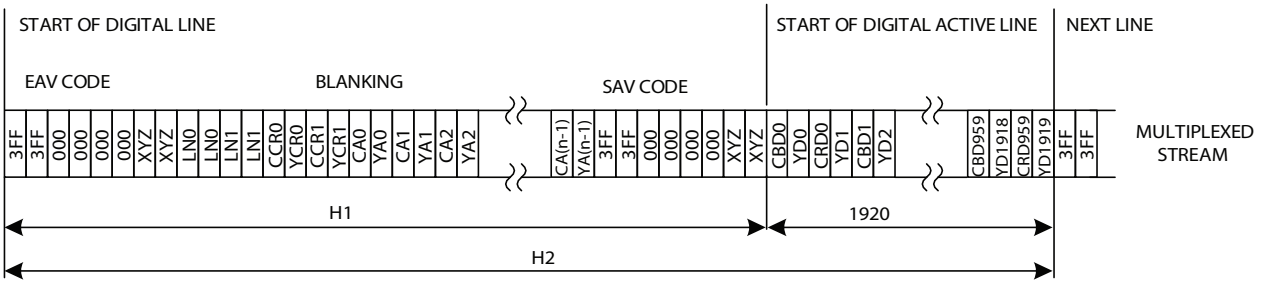

Figure 4-3: Multiplexed Luma and Chroma Over One Video Line - 1080i

Table 4-5: 1080-line Interlaced Horizontal Timing

Interlaced	60 or 60/1.001 Hz	50Hz
H1	560	1440
H2	4400	5280

4.4.3.1 High Definition 1080p Output Formats

ITU-R BT.1120 also includes progressive scan formats with 1080 active lines, with $Y'C'_BC'_R$ 4:2:2 sampling at pixel rates of 74.25MHz or 74.25/1.001 MHz. The following diagrams show horizontal and vertical timing for 1080-line progressive systems. The GV7704 provides a 10-bit multiplexed output interface, doubling the pixel clock output rate to 148.5MHz or 148.5/1.001 MHz.

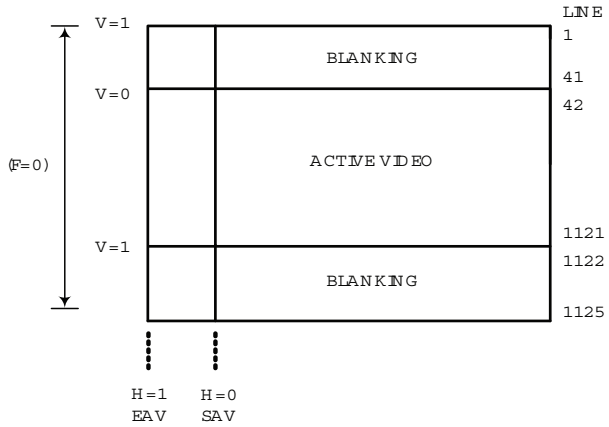

Figure 4-4: Frame Timing Relationship For 1080-line Progressive Systems

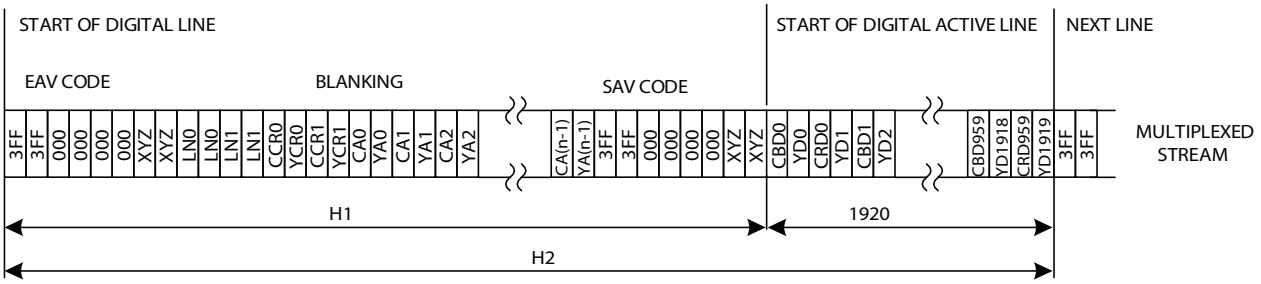

Figure 4-5: Multiplexed Luma and Chroma Over One Video Line - 1080p

Table 4-6: 1080-line Progressive Horizontal Timing

Progressive	30Hz, 30/1.001Hz, 60Hz, 60/1.001Hz	25Hz or 50Hz	24Hz or 24/1.001Hz
H1	560	1440	1660
H2	4400	5280	5500

4.4.3.2 High Definition 720p Output Formats

The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for progressive scan 720-line HD image formats. SMPTE ST 296-2001 specifies the representation for 720p digital $Y'C'_BC'_R$ 4:2:2 signals at pixel rates of 74.25MHz or 74.25/1.001 MHz. The GV7704 provides a 10-bit multiplexed output interface, doubling the pixel clock output rate to 148.5MHz or 148.5/1.001 MHz.

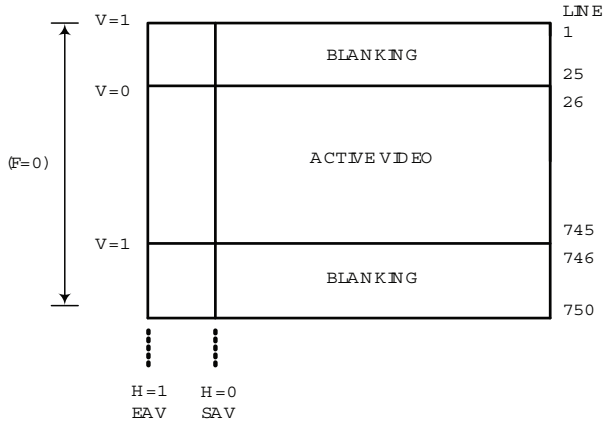

Figure 4-6: 720p Digital Vertical Timing

The frame rate determines the horizontal timing, which is shown in Table 4-7.

Table 4-7: 720p Horizontal Timing

Frame Rate	H = 1 Sample Number	H = 0 Sample Number	Total Samples Per Line
25	2560	0	7920
30 or 30/1.001	2560	0	6600
50	2560	0	3960
60 or 60/1.001	2560	0	3300

4.4.3.3 BT.656 Video Output Timing Mode

By default, the 10-bit parallel video output will contain two embedded TRS words, as defined in ITU-R BT.1120. Some commercially available CODEC devices cannot detect the presence of the double TRS in the HD video stream, and require that the 8/10-bit HD video contain only one TRS word, as per the ITU-R BT.656 Standard Definition format. When the BT656_ENABLE bit is HIGH, the GV7704 will re-format the parallel video