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SEMTECH
GENNUM PRODUCTS

GX3290

290 x 290 3.5Gb/s Crosspoint Switch with Trace Equalization and Output De-emphasis

Key Features

- 290 x 290 crosspoint switch architecture supporting broadcast and multi-cast modes
- Supports all data rates up to 3.5Gb/s
- Low power consumption: 34.25W typical (all channels active)
- Sophisticated, dynamic on-chip power management control
- Independent, programmable input trace equalization to reduce deterministic jitter (ISI)
- Independent, programmable output de-emphasis for driving long board traces
- High-speed, video-optimized control for multi-format applications
- Built-in system test features with on-chip PRBS generators and analyzers
- 2.5V analog core voltage, 1.8V digital core voltage
- Input and output voltages support either 1.2V, 1.8V or 2.5V CML
- JTAG-controlled boundary scan
- Selectable parallel/serial host interface
- 50mm x 50mm BGA (2377 ball)
- Operating temperature range: 0°C to +85°C
- RoHS compliant

Applications

Large m x n cascaded routers/switch fabrics for:

- Professional broadcast applications
- Enterprise and carrier applications
- High-speed automated test equipment
- 10GbE and InfiniBand networks

Description

The GX3290 is a low-power, high-speed 290 x 290 crosspoint switch, with robust signal conditioning circuits for driving and receiving high-speed signals through backplanes.

The device typically consumes 34.25W of power with all channels operational, and features sophisticated, dynamically scalable power management. Unused portions of the core are automatically turned off without affecting the operation of the remaining channels.

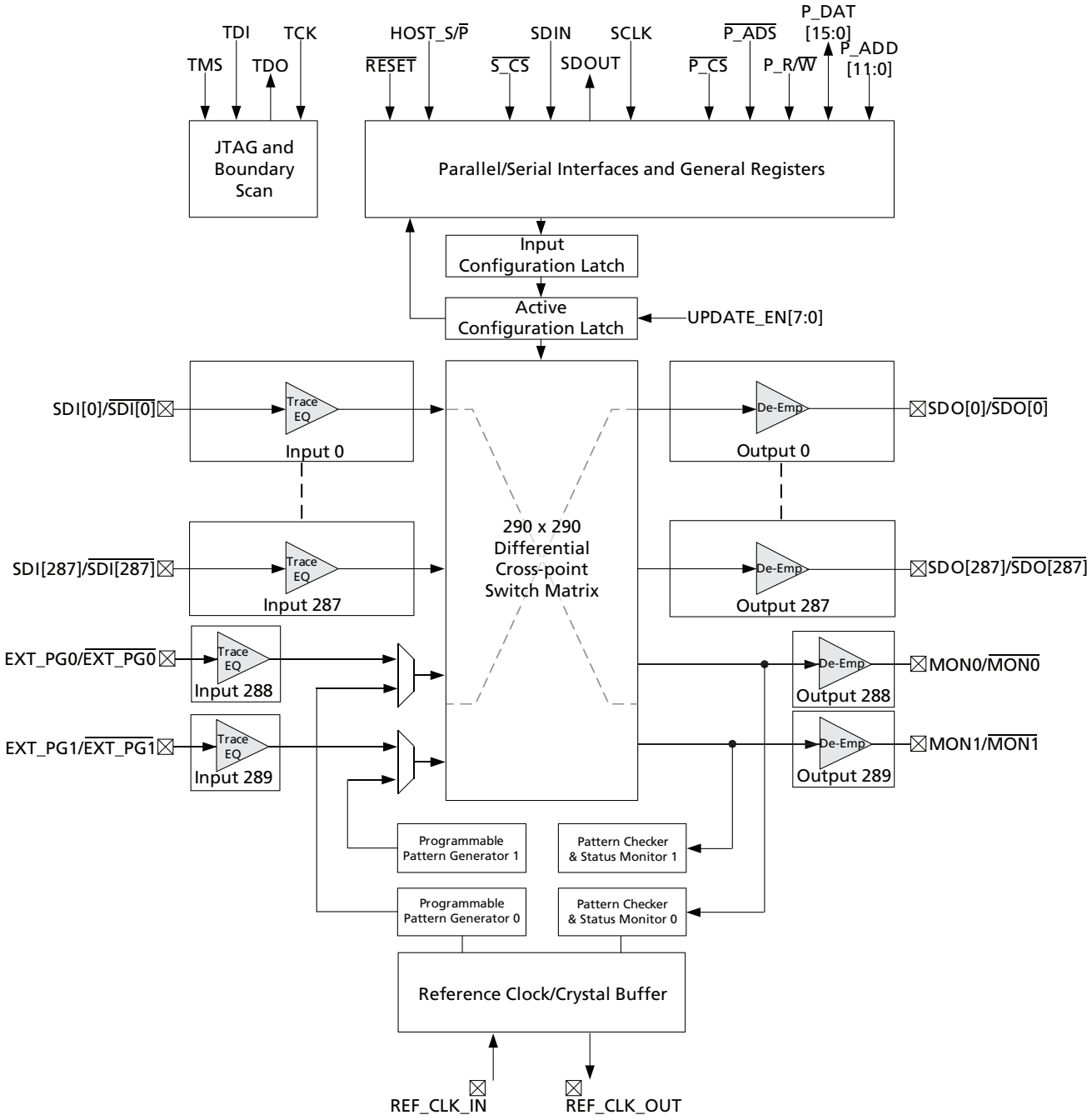
The signal conditioning features of the GX3290 include per-input programmable equalization and per-output programmable de-emphasis. The input equalizer removes ISI jitter—typically caused by PCB trace losses—by opening the input data eye in applications where long PCB traces are used. There are four settings available for the input equalizer, allowing flexibility in adjusting the equalization level on a per-input basis.

Output de-emphasis capability provides a boost of the high-frequency content of the output signal, such that the data eye remains open after passing through a long interconnect of PCB traces and connectors. There are four de-emphasis settings that can be enabled on a per-output basis.

Two integrated programmable pattern generators, and two pattern checkers are provided to assist in system test and configuration.

The pattern generators can each be routed to any output of the device without impacting the normal operation of any other channel. Any input can be routed to each of the pattern checkers.

The chip features eight independent strobe inputs, UPDATE_EN[7:0], which are used to determine the timing of the output updates. Any output can be linked to any strobe.



GX3290 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
2	011719	–	March 2013	Corrected second bullet in Section 4.7.1, and added a note to Section 4.4.
1	158372	–	October 2012	Included ESD Voltage Sensitivity in Table 2-1. Modifications to Table 4-18 and Section 4.12.2 to include Auto-Increment Timing and functionality. Updates to Appendix - Relevant Documentation with clear reference to correct documents. Converted document to Final Data Sheet.
0	157403	–	February 2012	Converted document to Preliminary Data Sheet. Updates throughout.
F	157275	–	November 2011	Minor updates through entire document.
E	156342	–	July 2011	Updates throughout entire document. Removed Configuration and Status Registers (transferred to document Crosspoint (GX3290 and family) Reference Manual (for CSRs)).
D	154735	–	September 2010	Changed maximum data rate to 3.5Gb/s. Updates to Figure 4-10 and Figure 4-11, 4.12.2 Serial Host Interface Specifications, Package Dimensions and Marking Diagram.
C	154303	–	July 2010	Updates throughout entire document. Changes to GX3290 Ball Assignment Overview (Top View). Addition of multiple sections in Section 4. Detailed Description. Addition of Ball Descriptions. Changes to Input/Output Equivalent Circuits and Application Information.
B	153176	–	January 2010	Updates to Table 2-3: DC Electrical Characteristics. Updates to Section 4.12 Host Interface. Updates to Figure 1-1: GX3290 Ball Assignment Overview (Top View). Addition of Section 3. Input/Output Equivalent Circuits.
A	152552	–	October 2009	New document.

Contents

1. Ball Out

1.1 Ball Assignment

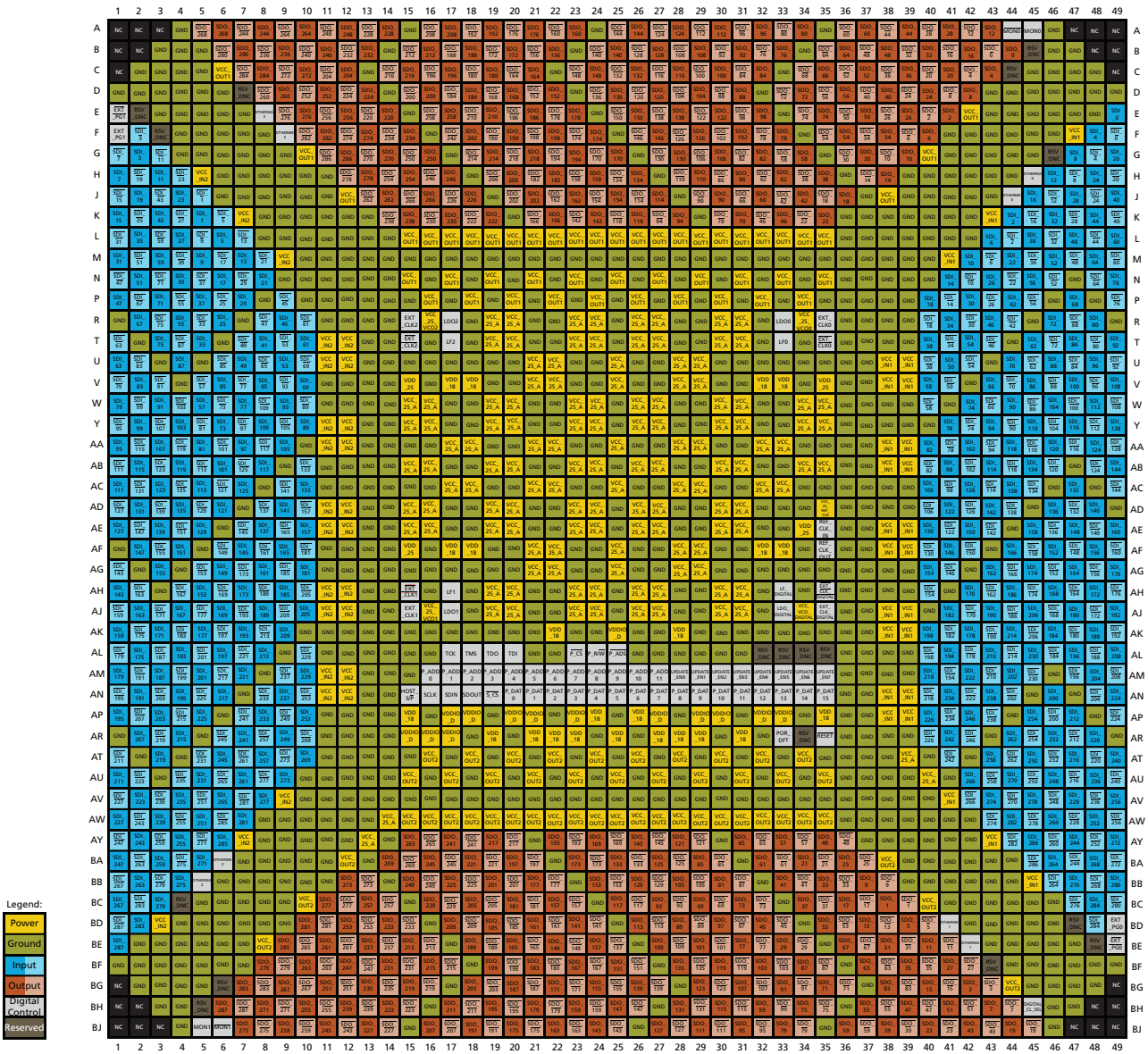


Figure 1-1: GX3290 Ball Assignment Overview (Top View)

1.2 Ball Descriptions

Table 1-1 shows the descriptions for selected GX3290 balls. For a comprehensive list of balls from the GX3290 Crosspoint family, please refer to GX3290 (and family) Crosspoint Ball Guide.

Table 1-1: Ball Descriptions

Ball #	Ball Name	I/O	Description
Serial Interface I/O			
AN16	SCLK	I	Serial Host Interface Clock. If unused, tie to ground.
AN17	SDIN	I	Serial Host Interface Data Input. If unused, tie to ground.
AN18	SDOUT	O	Serial Host Interface Data Output. Leave NC if not used.
AN19	$\overline{S\_CS}$	I	Serial Host Interface Chip Select. Active-LOW. Must be tied LOW when HOST_S/$\overline{P}$ is set LOW.
Parallel Interface I/O			
AL23	$\overline{P\_CS}$	I	Parallel host interface chip select. Active-LOW. Must be tied LOW when HOST_S/$\overline{P}$ is set HIGH.
AL24	P_R/$\overline{W}$	I	Selects between read and write operations on the parallel host interface. HIGH = Read, LOW = Write. If unused, tie to ground.
AL25	$\overline{P\_ADS}$	I	Address and Data Strobe. Strobe signal for latching the address and data into the chip. See Section 4.12.1 for timing information. If unused, tie to ground.
AM27 - AM16	P_ADD[11:0]	I	Address bus for the parallel interface. If unused, tie to ground.
AN35 - AN20	P_DAT[15:0]	I/O	Bi-directional data bus for the parallel interface. If $\overline{P\_CS}$ is HIGH, these pins are configured as inputs. If unused, tie to ground.
General I/O			
AN15	HOST_S/$\overline{P}$	I	Host Interface Select pin. Selects between serial and parallel host interfaces. Serial host interface is enabled when HIGH, parallel host interface is enabled when LOW. Must assert $\overline{RESET}$ after changing this pin.
AM35 - AM28	UPDATE_EN [7:0]	I	Update Strobes used to update the switch matrix configuration (see Section 4.5). If unused, weak pull-down to ground.
AR33	POR_DFT	I	This pin disables the Power On Reset circuitry when HIGH. Weak internal pull-down. Leave NC if not used.
AR35	$\overline{RESET}$	I	Active-LOW reset for entire chip (see Section 4.11 for timing details). Weak internal pull-up. Leave NC if not used.
Test Interface			
AL17	TCK	I	JTAG test clock. Weak pull-up if not used.
AL18	TMS	I	JTAG test mode start. Weak pull-up if not used.
AL19	TDO	O	JTAG test data out. Leave NC if not used.
AL20	TDI	I	JTAG test data in. Weak pull-up if not used.

Table 1-1: Ball Descriptions (Continued)

Ball #	Ball Name	I/O	Description
Filtering			
R17	LDO2	—	LDO filter capacitor for VCO_2. Connect through a 220nF capacitor to ground. See Figure 3-4 for configuration.
R33	LDO0	—	LDO filter capacitor for VCO_0. Connect through a 220nF capacitor to ground. See Figure 3-4 for configuration.
T17	LF2	—	PLL loop filter capacitor for VCO_2. See Figure 3-4 for configuration. Leave NC if not used.
T33	LF0	—	PLL loop filter capacitor for VCO_0. See Figure 3-4 for configuration. Leave NC if not used.
AH17	LF1	—	PLL loop filter capacitor for VCO_1. See Figure 3-4 for configuration. Leave NC if not used.
AH33	LF_DIGITAL	—	PLL loop filter capacitor for VCO_DIGITAL. Connect through a 47nF capacitor to ground. See Figure 3-4 for configuration.
AJ17	LDO1	—	LDO filter capacitor for VCO_1. Connect through a 220nF capacitor to ground. See Figure 3-4 for configuration.
AJ33	LDO_DIGITAL	—	LDO filter capacitor for VCO_DIGITAL. Connect through a 220nF capacitor to ground. See Figure 3-4 for configuration.
Crystal Oscillator			
AE35	REF_CLK_IN	—	Connect a 27MHz crystal between this ball and REF_CLK_OUT (or connect to a 27MHz clock source). See Section 4.9 and Figure 3-6.
AF35	REF_CLK_OUT	—	Connect a 27MHz crystal between this ball and REF_CLK_IN (if a clock source is used, leave floating). See Section 4.9 and Figure 3-6. Leave NC if not used.
External Clocks			
R15	EXT_CLK2	I	External CML clock for Pattern Generator 1 (true). Leave NC if not used.
R35	EXT_CLK0	I	External CML clock for Pattern Checker 0 (true). Leave NC if not used.
T15	$\overline{\text{EXT\_CLK2}}$	I	External CML clock for Pattern Generator 1 (complement). Leave NC if not used.
T35	$\overline{\text{EXT\_CLK0}}$	I	External CML clock for Pattern Checker 0 (complement). Leave NC if not used.
AH15	$\overline{\text{EXT\_CLK1}}$	I	External CML clock for Pattern Checker 1 (complement). Leave NC if not used.
AH35	$\overline{\text{EXT\_CLK\_DIGITAL}}$	I	External CML clock for Pattern Transmitter 0/Digital Core (complement). Leave NC if not used.
AJ15	EXT_CLK1	I	External CML clock for Pattern Checker 1 (true). Leave NC if not used.
AJ35	EXT_CLK_DIGITAL	I	External CML clock for Pattern Transmitter 0/Digital Core (true). Leave NC if not used.
BH45	DIGITAL_CL_SEL	I	Clock select between external clock source (EXT_CLK_DIGITAL) and internal VCO (VCO_DIGITAL). This pin has a weak internal pull-up, and should be pulled LOW to use an external clock.

Table 1-1: Ball Descriptions (Continued)

Ball #	Ball Name	I/O	Description
Temperature Sensors			
E8	DTHERMA3	—	Thermometer 3 diode terminals. See Section 4.8. Leave NC if not used.
F9	DTHERMK3	—	Thermometer 3 diode terminals. See Section 4.8. Leave NC if not used.
H45	DTHERMA0	—	Thermometer 0 diode terminals. See Section 4.8. Leave NC if not used.
J44	DTHERMK0	—	Thermometer 0 diode terminals. See Section 4.8. Leave NC if not used.
BA6	DTHERMK2	—	Thermometer 2 diode terminals. See Section 4.8. Leave NC if not used.
BB5	DTHERMA2	—	Thermometer 2 diode terminals. See Section 4.8. Leave NC if not used.
BD41	DTHERMK1	—	Thermometer 1 diode terminals. See Section 4.8. Leave NC if not used.
BE42	DTHERMA1	—	Thermometer 1 diode terminals. See Section 4.8. Leave NC if not used.
Monitors			
A44	$\overline{\text{MON0}}$	O	Serial monitoring output 0 (complement). Leave NC if not used.
A45	MON0	O	Serial monitoring output 0 (true). Leave NC if not used.
BJ5	MON1	O	Serial monitoring output 1 (true). Leave NC if not used.
BJ6	$\overline{\text{MON1}}$	O	Serial monitoring output 1 (complement). Leave NC if not used.
External Pattern Generators			
E1	$\overline{\text{EXT\_PG1}}$	I	Serial pattern generator input 1 (complement). Leave NC if not used.
F1	EXT_PG1	I	Serial pattern generator input 1 (true). Leave NC if not used.
BD49	EXT_PG0	I	Serial pattern generator input 0 (true). Leave NC if not used.
BE49	$\overline{\text{EXT\_PG0}}$	I	Serial pattern generator input 0 (complement). Leave NC if not used.
Reserved - Do Not Connect			
B45, C44, D7, E2, F3, G46, AL32, AL33, AL34, AL35, AR34, BC4, BD47, BE48, BF43, BG6, BH5,	RSV_DNC	—	Reserved. Do not connect.
SDI/SDO			
Refer to the GX3290 (and family) Crosspoint Ball Guide for a detailed list of SDI and SDO balls.			
Power			
Refer to the GX3290 (and family) Crosspoint Ball Guide for a detailed list of power supply balls.			
Ground			
Refer to the GX3290 (and family) Crosspoint Ball Guide for a detailed list of ground balls.			

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage (VDD_18)	-0.3V to +2.1V
Supply Voltage (VCC_IN1, VCC_IN2, VCC_25_A, VDD_25, VDDIO_D, VCC_OUT1, VCC_OUT2, VCC_25_REF_CLK, VCC_25_VCO0, VCC_25_VCO1, VCC_25_VCO2)	-0.3V to +2.8V
Input Voltage Range	-0.3 to (0.3 + min[VCC_IN1, VCC_25_A])V for even numbered SDI inputs and EXT_PG0
	-0.3 to (0.3 + min[VCC_IN2, VCC_25_A])V for odd numbered SDI inputs and EXT_PG1
ESD Voltage (HBM; all balls)	1kV
ESD Voltage (CDM; all balls)	100V
Storage Temperature Range	-50°C to +125°C
Operating Temperature Range	0°C to +85°C
Solder Reflow Temperature	245°C

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Notes
Operating Power Supply	VCC_25_A, VCC_25_REF_CLK	2.375	2.5	2.625	V	1
	VCC_IN1, VCC_IN2	1.14	1.2	1.26	V	2
		1.71	1.8	1.89	V	3
		2.375	2.5	2.625	V	1
	VCC_OUT1, VCC_OUT2	1.14	1.2	1.26	V	2
		1.71	1.8	1.89	V	3
		2.375	2.5	2.625	V	1
	VDD_18	1.71	1.8	1.89	V	3
	VDDIO_D	1.71	1.8	1.89	V	3
		2.375	2.5	2.625	V	1
	VDD_25	2.375	2.5	2.625	V	1
Operating Temperature Range (case)	T_{OP}	0	25	85	°C	—
Start-up Temperature Range	T_{SU}	-40	—	85	°C	—

Notes:

1. 2.5V supply.
2. 1.2V supply.
3. 1.8V supply.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Power	P	All channels active, VCC_IN[1,2] = VCC_OUT[1,2] = 1.2V±5%, ΔV_{OD} = 200mV, ΔV_{SDI} = 800mVppd, de-emphasis=6, without Pattern Generator/Checker, AC-coupled	—	34.25	43	W	1
		All channels active, VCC_IN[1,2] = VCC_OUT[1,2] = 1.2V±5%, ΔV_{OD} = 400mV, ΔV_{SDI} = 800mVppd, de-emphasis=6, without Pattern Generator/Checker, AC-coupled	—	37.66	—	W	1
		All channels active, VCC_IN[1,2] = VCC_OUT[1,2] = 2.5V±5%, ΔV_{OD} = 800mV, ΔV_{SDI} = 800mVppd, de-emphasis=6, without Pattern Generator/Checker, AC-coupled	—	44.39	54	W	1
		All channels active, VCC_IN[1,2] = VCC_OUT[1,2] = 2.5V±5%, ΔV_{OD} = 1200mV, ΔV_{SDI} = 800mVppd, de-emphasis=6, without Pattern Generator/Checker, AC-coupled	—	49.02	60	W	1
		PRBS Generator/Checker	—	1.86	—	W	—
Power in Reset Mode	P	$\overline{\text{RESET}}$ = 0	—	0.5	—	W	—
Current - VCC_25_A	ICC_25_A	With de-emphasis, without Pattern Generator/Checker	—	13.8	16.7	A	—
		Without de-emphasis, without Pattern Generator/Checker	—	13	—	A	—

Table 2-3: DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Current - VCC_IN1	ICC_IN1	All inputs active, ΔV_{SDI} = 1.2Vppd, DC-coupled	—	1.75	—	A	2
		All inputs active, ΔV_{SDI} = 1.2Vppd, AC-coupled	-0.2	—	0	A	3
Current - VCC_IN2	ICC_IN2	All inputs active, ΔV_{SDI} = 1.2Vppd, DC-coupled	—	1.75	—	A	2
		All inputs active, ΔV_{SDI} = 1.2Vppd, AC-coupled	-0.2	—	0	A	3
Current - VCC_OUT1	ICC_OUT1	VCC_OUT1 = 1.2V ±5%, all outputs active, ΔV_{OD} = 200mV, with De-emphasis	—	0.30	0.38	A	4
		VCC_OUT1 = 1.2V ±5%, all outputs active, ΔV_{OD} = 400mV, with De-emphasis	—	0.60	—	A	4
		VCC_OUT1 = 1.2V ±5%, all outputs active, ΔV_{OD} = 800mV, with De-emphasis	—	1.12	—	A	4, 5
		VCC_OUT1 = 2.5V ±5%, all outputs active, ΔV_{OD} = 200mV, with De-emphasis	—	0.34	—	A	4
		VCC_OUT1 = 2.5V ±5%, all outputs active, ΔV_{OD} = 400mV, with De-emphasis	—	0.60	—	A	4
		VCC_OUT1 = 2.5V ±5%, all outputs active, ΔV_{OD} = 800mV, with De-emphasis	—	1.23	1.55	A	4
		VCC_OUT1 = 2.5V ±5%, all outputs active, ΔV_{OD} = 1200mV, with De-emphasis	—	1.64	2.13	A	4

Table 2-3: DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Current - VCC_OUT2	ICC_OUT2	VCC_OUT2 = 1.2V ±5%, all outputs active, ΔV_{OD} = 200mV, with De-emphasis	—	0.30	0.38	A	4
		VCC_OUT2 = 1.2V ±5%, all outputs active, ΔV_{OD} = 400mV, with De-emphasis	—	0.60	—	A	4
		VCC_OUT2 = 1.2V ±5%, all outputs active, ΔV_{OD} = 800mV, with De-emphasis	—	1.12	—	A	4, 5
		VCC_OUT2 = 2.5V ±5%, all outputs active, ΔV_{OD} = 200mV, with De-emphasis	—	0.34	—	A	4
		VCC_OUT2 = 2.5V ±5%, all outputs active, ΔV_{OD} = 400mV, with De-emphasis	—	0.60	—	A	4
		VCC_OUT2 = 2.5V ±5%, all outputs active, ΔV_{OD} = 800mV, with De-emphasis	—	1.23	1.55	A	4
		VCC_OUT2 = 2.5V ±5%, all outputs active, ΔV_{OD} = 1200mV, with De-emphasis	—	1.64	2.13	A	4
Current - VCC_25_REF_CLK	ICC_25 _REF_CLK		—	20	40	mA	—
Current - VCC_VCO_DIGITAL	ICC_VCO _DIGITAL		—	6	10	mA	—
Current - VCC_25_VCO0	ICC_25 _VCO0		—	6	10	mA	—
Current - VCC_25_VCO1	ICC_25 _VCO1		—	6	10	mA	—
Current - VCC_25_VCO2	ICC_25 _VCO2		—	6	10	mA	—
Current - VDD_18	IDD_18	VDD_18 = 1.8V±5%	—	260	750	mA	—
Current - VDD_25	IDD_25	VDD_25 = 2.5V±5%	—	20	40	mA	—
Current - VDDIO_D	IDDIO_D	VDDIO_D = 1.8V±5%, all inputs active (15pF load)	—	50	100	mA	—
		VDDIO_D = 2.5V±5%, all inputs active (15pF load)	—	70	140	mA	—

Table 2-3: DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
High-speed Inputs/Outputs							
Serial Input Termination		Differential	—	100	—	Ω	6
		Single-ended	—	50	—	Ω	
Serial Output Termination		Differential	—	100	—	Ω	—
Serial Input Common Mode Voltage	V_{ICM}	VCC_IN[1,2] = 1.2V±5%, VCC_IN[1,2] = 1.8V±5%, VCC_IN[1,2] = 2.5V±5%, terminated to VCC_IN[1,2]	VCC_IN [1,2] - (ΔV_{SDI_max}/4)	—	VCC_IN [1,2] - (ΔV_{SDI_min}/4)	V	7, 8, 9, 10
Serial Output Common Mode Voltage	V_{OCM}	VCC_OUT[1,2] = 1.2V±5%, VCC_OUT[1,2] = 1.8V±5%, VCC_OUT[1,2] = 2.5V±5%	VCC_OUT [1,2] - (ΔV_{OD_max}/4)	—	VCC_OUT [1,2] - (ΔV_{OD_min}/4)	V	—
Host Interface							
Logic HIGH voltage on digital input pins	V_{IH}		0.7 x VDDIO_D	—	VDDIO_D + 0.3	V	11
Logic LOW voltage on digital input pins	V_{IL}		-0.3	—	0.3 x VDDIO_D	V	11
Output Logic LOW	V_{OL}	I_{OL} = 2mA, 2.5V operation	—	—	0.7	V	11
		I_{OL} = 2mA, 1.8V operation	—	—	0.45	V	11
Output Logic HIGH	V_{OH}	I_{OH} = -2mA, 2.5V operation	1.7	—	—	V	11
		I_{OH} = -2mA, 1.8 operation	1.35	—	—	V	11

Notes:

1. Total Maximum Power is lower than individual maximum currents multiplied by individual maximum supply voltages because the individual maximum currents can not occur simultaneously (they occur at different conditions).
2. The ICC_IN1 and ICC_IN2 current flows out of the GX3290 and into the input signal source, and is subject to variability in that source. Some variability in input signal source current draw should be assumed, and up to ±15% is possible.
3. When the common mode termination points for AC-coupled inputs are connected to VCC_IN1, VCC_IN2, the GX3290 equalizer input bias currents can lead to current flowing out of the VCC_IN1, VCC_IN2 supply pins.
4. Currents apply for output DC-coupled applications. When AC-coupled, the current draw may be increased by up to 2x.
5. For DC-coupled applications only.
6. Input termination is selectable between 100Ω differential and 50Ω single-ended. See Section 3. Input/Output Equivalent Circuits.
7. DC common mode current into/out of each EQ input differential pair should not exceed 14mA, and the current into/out of each half of the differential pair should not exceed 14mA.
8. No more than VCC_IN[1,2] - ΔV_{SDI_actual}/4.
9. Where it is understood that VCC_IN[1,2] have a ±5% tolerance.
10. In no case should either side of the input differential pair be allowed to rise above VCC_25_A + 0.3V or fall below -0.3V.
11. Specifications relate to all host interface pins.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Serial Input Data Rate	DR_{SDO}	—	—	—	3.5	Gb/s	—
Propagation Delay	t_P	—	—	—	6	ns	1
Propagation Delay Difference	Δt_P	Between any two channels	—	—	5.5	ns	1
High-speed Inputs/Outputs							
Output Switch Time using Update Enable Strobes			0.9	—	1.8	µs	2
Input Voltage Swing	ΔV_{SDI}	—	100	—	1200	mVppd	—
Output Voltage Swing	ΔV_{OD}	VCC_OUT[1,2] = 1.2V±5%, Output = 200mVppd	150	225	300	mVppd	—
		VCC_OUT[1,2] = 1.2V±5%, Output = 400mVppd	300	450	600	mVppd	—
		VCC_OUT[1,2] = 1.2V±5%, Output = 800mVppd	600	900	1200	mVppd	3
		VCC_OUT[1,2] = 1.8V±5%, Output = 200mVppd	150	225	300	mVppd	—
		VCC_OUT[1,2] = 1.8V±5%, Output = 400mVppd	300	450	600	mVppd	—
		VCC_OUT[1,2] = 1.8V±5%, Output = 800mVppd	600	900	1200	mVppd	—
		VCC_OUT[1,2] = 2.5V±5%, Output = 200mVppd	150	225	300	mVppd	—
		VCC_OUT[1,2] = 2.5V±5%, Output = 400mVppd	300	450	600	mVppd	—
		VCC_OUT[1,2] = 2.5V±5%, Output = 800mVppd	600	900	1200	mVppd	—
		VCC_OUT[1,2] = 2.5V±5%, Output = 1200mVppd	1000	1350	1700	mVppd	—
Output Rise/Fall Time	t_r/t_f	All output swings. 20% to 80%.	—	—	150	ps	—
Duty Cycle Distortion		All data rates, all output swings.	-50	—	+50	ps	—
Additive Jitter		All inputs active, peak-to-peak (PRBS 31)	—	—	60	ps_{p-p}	—
Input Trace Equalization			0	—	12	dB	4
Output De-Emphasis Setting		Range	0	—	11.2	dB	4
		Maximum Setting	9	—	—	dB	

Table 2-4: AC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Host Interface							
Parallel Rate of Operation			0.1	—	112.5	Mop/s	5, 6, 7
Serial Interface Operating Speed			0.1	—	25	MHz	5, 8

Notes:

1. See Section 4.4 for more details.
2. This parameter is the time it takes for the outputs to change to a new switch matrix configuration when the corresponding strobe signal assigned to that output is asserted.
3. DC-coupled.
4. Selectable, maximum gain occurs at 3Gb/s (or 1.5GHz).
5. Specifications relate to all host interface pins.
6. Millions of operations per second.
7. For detailed timing specifications, see Section 4.12.1.
8. For detailed timing specifications, see Section 4.12.2.

3. Input/Output Equivalent Circuits

Note: Please refer to the following supplementary documents: Crosspoint Design Guide and EB-GX3290 Schematics, PCB Layout and Bill of Materials.

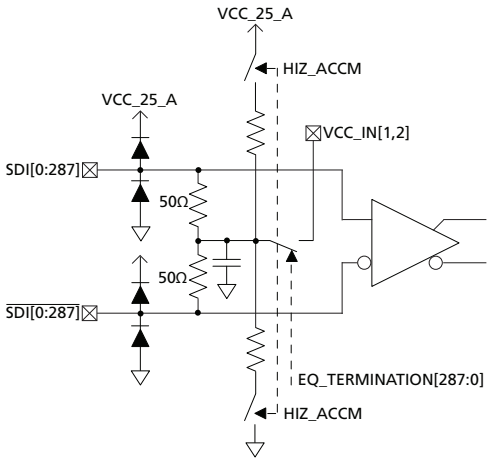


Figure 3-1: Equalizer Input Equivalent Circuit

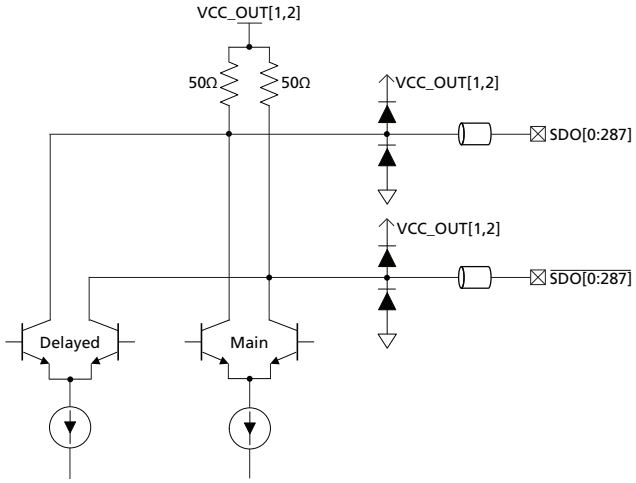


Figure 3-2: Trace Driver Output Equivalent Circuit

Note: the MON0 and MON1 outputs are terminated to the VCC_25_A supply.

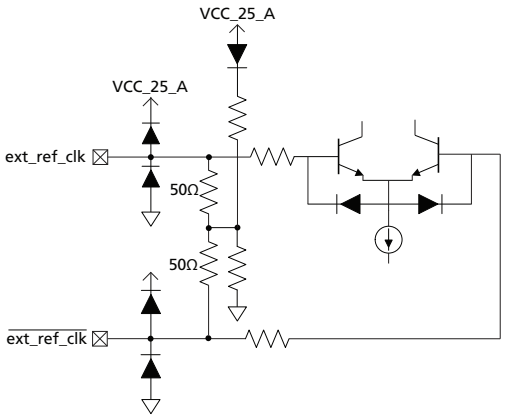
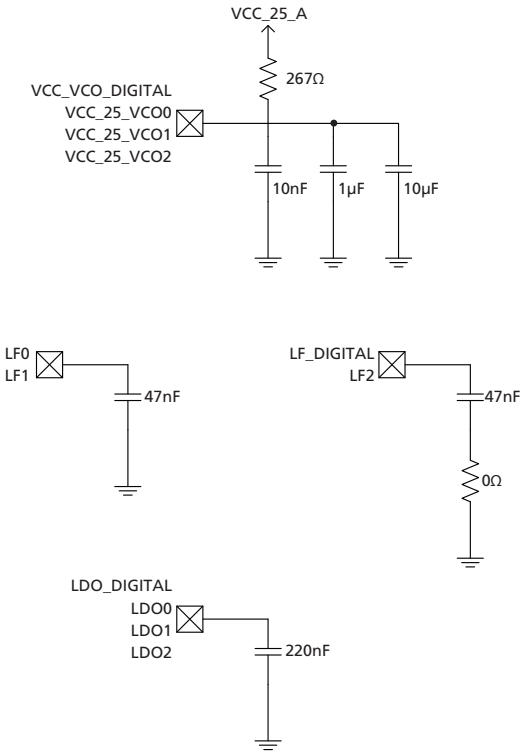
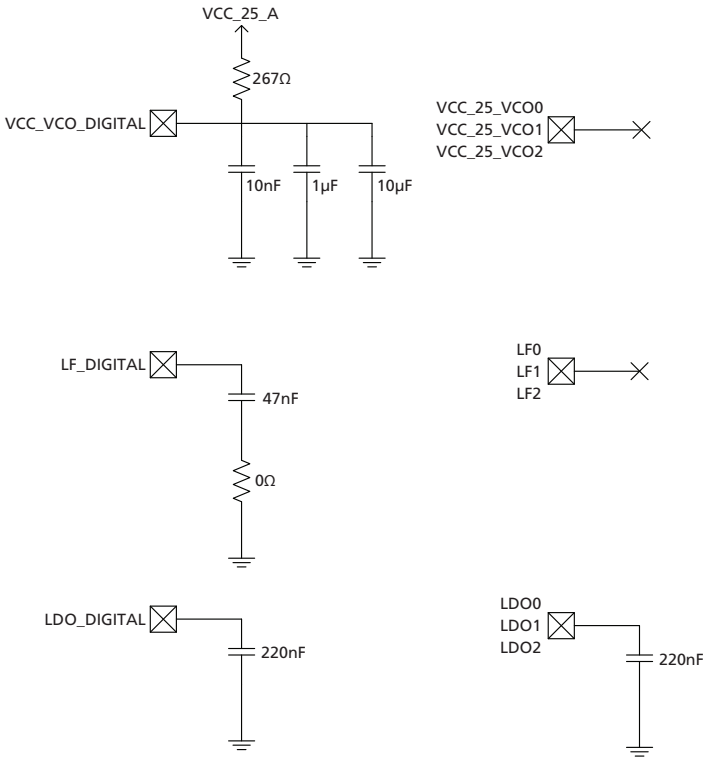


Figure 3-3: External Clock Input Equivalent Circuit

If the internal temperature ADCs, pattern generators, and checkers are used, these connections are required.

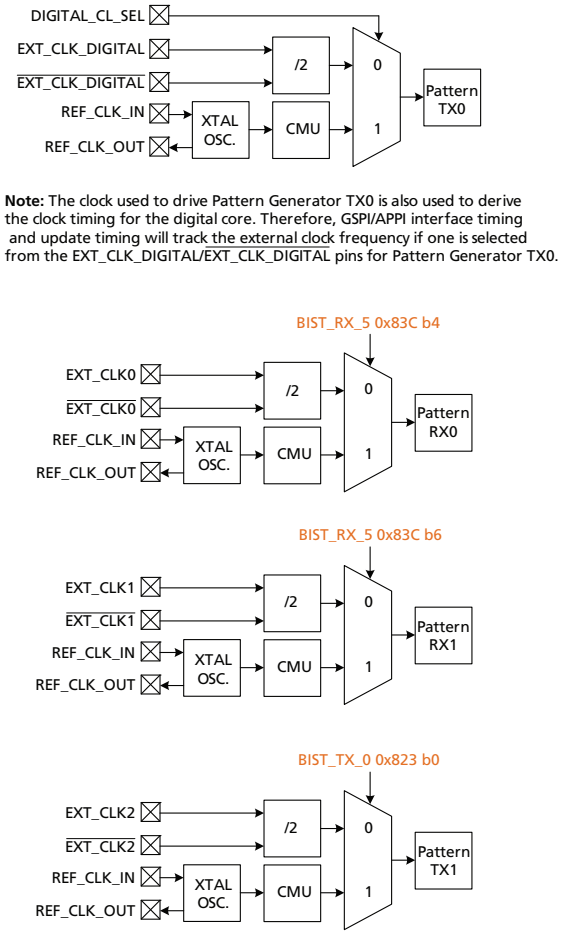


If the internal temperature ADCs, pattern generators, and checkers are not used, only these connections are required.



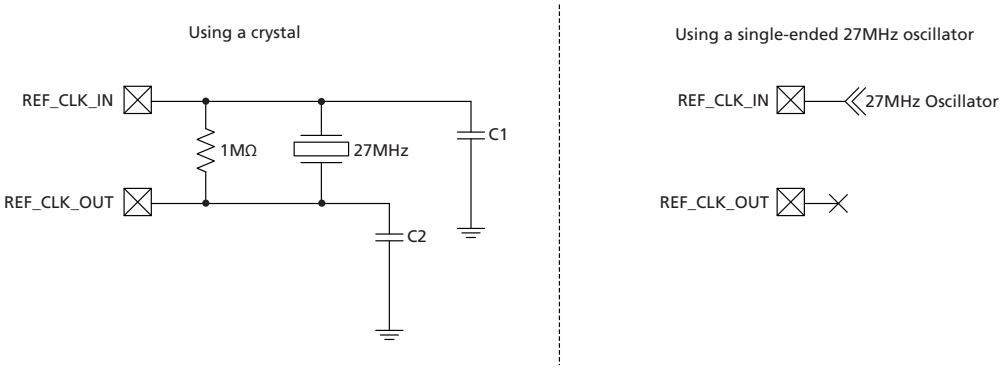
Note 1: Each of the VCC_VCO_DIGITAL, VCC_VCO0, VCC_VCO1, and VCC_VCO2 pins require an independent RC network.
Note 2: The LF_DIGITAL and LF2 pins each require an independent RC network.
Note 3: The LF0 and LF1 pins each require an independent capacitor to ground.
Note 4: Each of the LDO_DIGITAL, LDO0, LDO1, and LDO2 pins require an independent capacitor to ground.
Note 5: VCC_VCO_DIGITAL, LF_DIGITAL and LDO_DIGITAL used for pattern generator TX0, digital communication (GSPI and APPI), and the internal temperature ADC for JNCTN_TEMP_1. VCC_VCO_DIGITAL, LF_DIGITAL and LDO_DIGITAL must always be connected.
Note 6: VCC_25_VCO0, LF0, LDO0 used for pattern checker RX0 and the internal temperature ADC for JNCTN_TEMP_0.
If VCC_25_VCO0, LF0, and LDO0 are not connected, pattern checker RX0 and the internal temperature ADC for JNCTN_TEMP_0 will not operate.
Note 7: VCC_25_VCO1, LF1, LDO1 used for pattern checker RX1 and the internal temperature ADC for JNCTN_TEMP_2.
If VCC_25_VCO1, LF1, and LDO1 are not connected, pattern checker RX1 and the internal temperature ADC for JNCTN_TEMP_2 will not operate.
Note 8: VCC_25_VCO2, LF2, LDO2 used for pattern generator TX1 and the internal temperature ADC for JNCTN_TEMP_3.
If VCC_25_VCO2, LF2, and LDO2 are not connected, pattern generator TX1 and the internal temperature ADC for JNCTN_TEMP_3 will not operate.

Figure 3-4: Required connections for VCC_VCO_DIGITAL, VCC_25_VCO0, VCC_25_VCO1, VCC_25_VCO2, LF_DIGITAL, LF0, LF1, LF2, LDO_DIGITAL, LDO0, LDO1 and LDO2



Note: The clock used to drive Pattern Generator TX0 is also used to derive the clock timing for the digital core. Therefore, GSPI/APPI interface timing and update timing will track the external clock frequency if one is selected from the EXT_CLK_DIGITAL/EXT_CLK_DIGITAL pins for Pattern Generator TX0.

Figure 3-5: PRBS Generator/Checker Clock Selection



Note: The value of the C1 and C2 load capacitors are dependent on the chosen crystal.

Figure 3-6: Crystal Oscillator

4. Detailed Description

4.1 Serial Data Input

Each of the GX3290 SDI inputs provide on-chip 100Ω differential terminations (or 50Ω single-ended). Each is compatible with input differential amplitudes from 100mVppd to 1200mVppd, and input signal sources having CML outputs referred to DC supplies of 1.2V, 1.8V or 2.5V. Note that for AC-coupled inputs, the recommended supply voltage for VCC_IN1 and VCC_IN2 is 1.8V.

Each of the 290 SDI input channels include frequency domain equalization, independently-programmable to one of four levels, to compensate from 0 to 47 inches (119 cm) of FR4 trace at 3Gb/s. The boost at the 1.5GHz Nyquist frequency, and recommended trace length range, are shown under EQ_BOOST[287:0], EXT_PG0_EQ_BOOST, EXT_PG1_EQ_BOOST in Table 4-1. See Figure 3-1.

Each input can be powered-down independently using the corresponding EQ_POWERDOWN[287:0] or EXT_PG0_EQ_POWERDOWN or EXT_PG1_EQ_POWERDOWN bit.

To accommodate input signal sources with 1.2V supplies and 1200mVppd signal amplitudes, the input common mode point should be terminated to the respective VCC_IN1 or VCC_IN2 supply.

The common mode termination connection to the respective VCC_IN1 or VCC_IN2 supply of each input can be independently controlled using the EQ_TERMINATION[287:0] or EXT_PG0_EQ_TERMINATION or EXT_PG1_EQ_TERMINATION bit (see Figure 3-1 and Table 4-1).

Note 1: When the HIZ_ACCM bit is set (register address 0x400h bit 0), inputs with their common mode termination not connected to VCC_IN1 or VCC_IN2 are connected to an internal common mode bias.

When an input EQ is powered-down, its common mode termination is automatically disconnected from the corresponding VCC_IN1 or VCC_IN2.

For each of the inputs, there are control parameters (register address 0x401h to 0x522h). See Table 4-1 below.

Note 2: The EXT_PG01_SOURCE_PIN_PRBSB and EXT_PG1_SOURCE_PIN_PRBSB bits in the TEST_SETUP register must be set to connect the EXT_PG0 and EXT_PG1 pins to the matrix.

Table 4-1: Serial Data Input

EQ_BOOST[287:0], EXT_PG0_EQ_BOOST and EXT_PG1_EQ_BOOST bits 1:0 (binary)	Boost Applied (@ nominal 1.5GHz)	
00	0dB boost	0” to 6” (15 cm) trace
01	3.5dB boost	6” (15 cm) to 16” (40 cm) trace
10	7.6dB boost	16” (40 cm) to 35” (89 cm) trace

Table 4-1: Serial Data Input (Continued)

EQ_BOOST[287:0], EXT_PG0_EQ_BOOST and EXT_PG1_EQ_BOOST bits 1:0 (binary)	Boost Applied (@ nominal 1.5GHz)	
11	12dB boost	35" (89 cm) to 47" (119 cm) trace
EQ_TERMINATION[287:0], EXT_PG0_EQ_TERMINATION and EXT_PG1_EQ_TERMINATION bits 3:3	**Input Termination Common Mode Point Switch to VCC_IN_1, VCC_IN_2**	
0	Open (see Figure 3-1)	
1	Closed (see Figure 3-1)	
EQ_POWERDOWN[287:0], EXT_PG0_EQ_POWERDOWN and EXT_PG1_EQ_POWERDOWN bits 4:4	**Equalizer Power**	
0	On	
1	Off	

4.2 Serial Data Output

Each of the GX3290 SDI outputs have two on-chip 50Ω single-ended terminations, and can be programmed to output differential amplitudes of 200mVppd, 400mVppd or 800mVppd when the corresponding VCC_OUT1 or VCC_OUT2 is connected to either 1.2V or 1.8V, or 200mVppd, 400mVppd, 800mVppd, or 1200mVppd when the corresponding VCC_OUT1 or VCC_OUT2 is connected to 2.5V. The selection of the output swing is made using the corresponding OUTPUT_SWING_SET[287:0], MON0_OUTPUT_SWING_SET or MON1_OUTPUT_SWING_SET bits, shown in Table 4-3.

If the HIGH_OP_V bit is set when either the VCC_OUT1 or VCC_OUT2 supplies are 1.2V or 1.8V, the 800mVppd swing setting is no longer valid for that output bank. Swing settings for an output bank connected to a 2.5V supply are unaffected.

Table 4-2: HIGH_OP_V Swing Selection

	HIGH_OP_V = 0	HIGH_OP_V = 1	
VCC_OUTx Supply Voltage (V)	**Valid Output Swing Selection (mVppd)**	**Valid Output Swing Selection (mVppd)**	**Note**
1.2	200, 400, 800	200, 400	1
1.8	200, 400, 800	200, 400	—

Table 4-2: HIGH_OP_V Swing Selection (Continued)

	HIGH_OP_V = 0	HIGH_OP_V = 1	
VCC_OUTx Supply Voltage (V)	Valid Output Swing Selection (mVppd)	Valid Output Swing Selection (mVppd)	Note
2.5	200, 400, 800	200, 400, 800, 1200	2

Notes:

1. For an 800mVppd output swing when the corresponding VCC_OUT1 or VCC_OUT2 is connected to 1.2V, the output must be DC-coupled to a receiving device terminated to 1.2V.
2. When VCC_OUT1 or VCC_OUT2 is set to 2.5V, the HIGH_OP_V bit must be set to enable 1200mVppd swing selection.

Each of the 290 SDI output channels provide independently programmable de-emphasis, to compensate from 0 to 47 inches (119 cm) of FR4 trace at 3Gb/s. The selection of the amount of output de-emphasis is made using the corresponding OUTPUT_DEEMPHASIS[287:0], MON0_OUTPUT_DEEMPHASIS or MON1_OUTPUT_DEEMPHASIS bits, shown in Table 4-3.

Each output can be independently powered-down by the setting of the corresponding bit: ACTIVE_POWER_DOWN[287:0], DYNAMIC_POWER_DOWN[287:0] together with the assigned strobe, MON0_POWER_DOWN, or MON1_POWER_DOWN.

The polarity of the signal at each output can be independently inverted by setting the corresponding bit: ACTIVE_SIGNAL_INVERT[287:0], DYNAMIC_SIGNAL_INVERT[287:0] together with the assigned strobe, MON0_SIGNAL_INVERT, or MON1_SIGNAL_INVERT.

Table 4-3: Serial Data Output

OUTPUT_SWING_SET[287:0], MON0_OUTPUT_SWING_SET and MON1_OUTPUT_SWING_SET bits 2:0 (binary)	Output Swing
000	200mVppd
001	400mVppd
011	800mVppd
110	1200mVppd
111	Reserved. Do not use.
OUTPUT_DEEMPHASIS[287:0], MON0_OUTPUT_DEEMPHASIS and MON1_OUTPUT_DEEMPHASIS bits 5:3 (binary)	**Level of De-emphasis**
000	Off
100	12” (30 cm) nominal
101	24” (60 cm) nominal
110	36” (90 cm) nominal
111	48” (120 cm) nominal

Table 4-3: Serial Data Output (Continued)

ACTIVE_SIGNAL_INVERT[287:0], DYNAMIC_SIGNAL_INVERT[287:0], MON0_SIGNAL_INVERT or MON1_SIGNAL_INVERT	Status
0	Not inverted
1	Inverted
ACTIVE_POWER_DOWN[287:0], DYNAMIC_POWER_DOWN[287:0], MON0_POWER_DOWN or MON1_POWER_DOWN	**Status**
0	On
1	Off

4.3 Crosspoint Switch Matrix Operation

The crosspoint switch matrix routes the serial digital input signals (SDI[0:287]/$\overline{\text{SDI}}$[0:287], EXT_PG0/$\overline{\text{EXT\_PG0}}$ or EXT_PG1/$\overline{\text{EXT\_PG1}}$) to one or more serial digital outputs (SDO[0:287]/$\overline{\text{SDO}}$[0:287], MON0/$\overline{\text{MON0}}$ or MON1/$\overline{\text{MON1}}$). The matrix is configured on a per output basis. Each serial digital output can be configured to accept a signal from one serial digital input. Multiple serial digital outputs can accept input from the same serial digital input.

Updates to the switch matrix take place as soon as they are written to the host interface when controlling the device through the ACTIVE Configuration and Status Registers. These registers are the ACTIVE[287:0], MON0, and MON1 registers found in Section 2 of the Crosspoint (GX3290 and family) Reference Manual (for CSRs) document.

Before the ACTIVE[287:0], MON0, and MON1 registers at addresses 0x200h through 0x321h can be directly used to update the crosspoint switch matrix, an initialization procedure is required. One of the UPDATE_EN[7:0] pins needs be toggled from a low state to a high state, and back to a low state again.

Alternatively, set the SOFTWARE_UPDATE_ENABLE bit in the CONTROL_SETUP register at address 0xA00h to a value of 1, and then toggle one of the SOFT_UPDATE_EN[7:0] bits in the SOFT_UPDATE_CONTROL register at address 0xA01h from a value of 0 to a value of 1, and then back to a value of 0.

If the ACTIVE[287:0], MON0, and MON1 registers are not being directly written by the system controller, this procedure is not required. Reading from the ACTIVE[287:0], MON0, and MON1 registers will work regardless of whether or not the above procedure is executed.

Updating the crosspoint switch matrix using the DYNAMIC[287:0] registers (discussed below) does not require the initialization procedure described above.

The switch matrix can also be updated using double-buffering when controlling the device through the DYNAMIC Configuration and Status Registers. These registers are DYNAMIC[287:0] in Section 1 of the Crosspoint (GX3290 and family) Reference Manual (for CSRs) document.

When using dynamic configuration, updates to the switch matrix are first written to the DYNAMIC[287:0] registers where they are held until the corresponding update strobe signal, selected using the UPDATE_SELECT[287:0] bits in the DYNAMIC[287:0] registers, changes state from LOW-to-HIGH.

The source for the update strobes can either be via external pins (UPDATE_EN[7:0]) or register bits (SOFT_UPDATE_EN[7:0]) as selected by the setting of the SOFTWARE_UPDATE_ENABLE bit in the CONTROL_SETUP register. Setting the SOFTWARE_UPDATE_ENABLE bit LOW causes the device to use the external UPDATE_EN[7:0] pins as update strobes for the switch matrix. Setting the SOFTWARE_UPDATE_ENABLE bit HIGH causes the device to use the SOFT_UPDATE_EN[7:0] bits as update strobes for the switch matrix. See Section 6 of the Crosspoint (GX3290 and family) Reference Manual (for CSRs) document.

When the selected update strobe signal (or bit) transitions from LOW-to-HIGH, the state of all the outputs configured to respond to that update strobe signal (or bit) are updated at that time.

Regardless of which register set is used to configure the switch matrix, the current configuration of the matrix is always available by reading back the ACTIVE[287:0] registers.

Note: The MON0 and MON1 outputs can not be powered up/down, switched, or polarity inverted dynamically (Dynamic Configuration). They can only be configured in the Active Configuration mode described above using the settings in registers 0x320h and 0x321h, respectively. Also, the MON0 and MON1 outputs are terminated to the VCC_25_A supply.

4.4 Propagation Delay

The propagation delay is dependent on the path that the signal takes through the device. Although the delay difference from the shortest path to the longest path could be up to 5.5ns, this difference is at a minimum for connections from inputs numerically close together and on the same side of the device to outputs that are numerically close together and on the same side of the device. Propagation delay differences of less than 750ps can be expected when the inputs are adjacent in the ballout and the outputs are also adjacent in the ballout.

Note: The 750ps propagation delay difference (skew) between physically adjacent channels is guaranteed by simulation.

4.5 Using Multiple Strobes

The GX3290 has eight fully-independent update strobes.

Outputs 287 to 0 can be assigned to one of the eight strobes through the setting of the UPDATE_SELECT bits in the corresponding DYNAMIC[287:0] register. The input signal selection, output power switching and signal inversion will take effect on the LOW-to-HIGH edge of its assigned strobe signal or bit. This allows different portions of the crosspoint to be switched at different points in time. This is particularly useful in systems supporting multiple data or video formats, where the switch point/time varies from format to format.

4.6 Pattern Generator and Pattern Checker

4.6.1 Pattern Generator

Note 1: There are two pattern generator "Tx" blocks in the GX3290. In the following, wherever only TX0 is mentioned, the corresponding is also true for TX1.

Note 2: When the PRBS Generator is disabled, the generated signal does not completely terminate. The PRBS polynomial bits must be re-written in order to terminate the signal.

The two pattern generator "Tx" blocks in the GX3290 can each independently generate PRBS 2^7-1, PRBS 2^{15}-1, and PRBS 2^{23}-1 data patterns, or alternating 1's and 0's. The built-in clock multiplier PLLs independently synthesize rates of 270Mb/s and 2.97Gb/s from the required, external 27MHz reference clock (see Section 4.9). Other rates up to 3Gb/s can be generated by providing an external clock signal at 2x, 4x, or 22x the desired bit rate to TX1, with a maximum external clock frequency of 6GHz.

Table 4-4: Tx External Clocks

TX0	TX1
EXT_CLK_DIGITAL (AJ35)	EXT_CLK2 (R15)
$\overline{\text{EXT\_CLK\_DIGITAL}}$ (AH35)	$\overline{\text{EXT\_CLK2}}$ (T15)

While this facility exists for both TX0 and TX1, the user is cautioned that the digital core clock is derived from the TX0 data clock, and therefore interface and update timing will track the external clock frequency if one is provided to TX0.

The pattern generators are enabled by the TX0_PRBS_GEN_ENABLE and TX1_PRBS_GEN_ENABLE bits (register address 0x802h, bits [1:0] respectively).

The PRBS generating polynomials used are:

1. PRBS7: $x^7 + x^6 + 1$
2. PRBS15: $x^{15} + x^{14} + 1$
3. PRBS23: $x^{23} + x^{18} + 1$

The pattern generated is selected via the TX0_PRBS_POLYNOMIAL and TX1_PRBS_POLYNOMIAL bits (register address 0x800h and 0x801h respectively).

Table 4-5: Generated Patterns

TX0_PRBS_POLYNOMIAL[1:0] (binary)	Pattern Generated
00	PRBS7
01	PRBS15
10	PRBS23
11	Square Wave