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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





# Section I. HardCopy Stratix Device Family Data Sheet

This section provides designers with the data sheet specifications for HardCopy® Stratix structured ASICs. The chapters contain feature definitions of the internal architecture, JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, and a reference to power consumption for HardCopy Stratix structured ASICs.

This section contains the following:

- [Chapter 1, Introduction to HardCopy Stratix Devices](#)
- [Chapter 2, Description, Architecture, and Features](#)
- [Chapter 3, Boundary-Scan Support](#)
- [Chapter 4, Operating Conditions](#)
- [Chapter 5, Quartus II Support for HardCopy Stratix Devices](#)
- [Chapter 6, Design Guidelines for HardCopy Stratix Performance Improvement](#)

## Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.





# 1. Introduction to HardCopy Stratix Devices

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## Introduction

HardCopy® Stratix® structured ASICs, Altera's second-generation HardCopy structured ASICs, are low-cost, high-performance devices with the same architecture as the high-density Stratix FPGAs. The combination of Stratix FPGAs for prototyping and design verification, HardCopy Stratix devices for high-volume production, and the Quartus® II design software beginning with version 3.0, provide a complete and powerful alternative to ASIC design and development.

HardCopy Stratix devices are architecturally equivalent and have the same features as the corresponding Stratix FPGA. They offer pin-to-pin compatibility using the same package as the corresponding Stratix FPGA prototype. Designers can prototype their design to verify functionality with Stratix FPGAs before seamlessly migrating the proven design to a HardCopy Stratix structured ASIC.

The Quartus II software provides a complete set of inexpensive and easy-to-use tools for designing HardCopy Stratix devices. Using the successful and proven methodology from HardCopy APEX™ devices, Stratix FPGA designs can be seamlessly and quickly migrated to a low-cost ASIC alternative. Designers can use the Quartus II software to design HardCopy Stratix devices to obtain an average of 50% higher performance and up to 40% lower power consumption than can be achieved in the corresponding Stratix FPGAs. The migration process is fully automated, requires minimal customer involvement, and takes approximately eight weeks to deliver fully tested HardCopy Stratix prototypes.

The HardCopy Stratix devices use the same base arrays across multiple designs for a given device density and are customized using the top two metal layers. The HardCopy Stratix family consists of the HC1S25, HC1S30, HC1S40, HC1S60, and HC1S80 devices. [Table 1-1](#) provides the details of the HardCopy Stratix devices.

**Table 1–1. HardCopy Stratix Devices and Features**

| Device | LEs (1) | M512 Blocks | M4K Blocks | M-RAM Blocks | DSP Blocks (2) | PLLs (3) |
|--------|---------|-------------|------------|--------------|----------------|----------|
| HC1S25 | 25,660  | 224         | 138        | 2            | 10             | 6        |
| HC1S30 | 32,470  | 295         | 171        | 2 (4)        | 12             | 6        |
| HC1S40 | 41,250  | 384         | 183        | 2 (4)        | 14             | 6        |
| HC1S60 | 57,120  | 574         | 292        | 6            | 18             | 12       |
| HC1S80 | 79,040  | 767         | 364        | 6 (4)        | 22             | 12       |

**Notes to Table 1–1:**

- (1) LE: logic elements.
- (2) DSP: digital signal processing.
- (3) PLLs: phase-locked loops.
- (4) In HC1S30, HC1S40, and HC1S80 devices, there are fewer M-RAM blocks than in the equivalent Stratix FPGA. All other resources are identical to the Stratix counterpart.

## Features

HardCopy Stratix devices are manufactured on the same 1.5-V, 0.13  $\mu\text{m}$  all-layer-copper metal fabrication process (up to eight layers of metal) as the Stratix FPGAs.

- Preserves the functionality of a configured Stratix device
- Pin-compatible with the Stratix counterparts
- On average, 50% faster than their Stratix equivalents
- On average, 40% less power consumption than their Stratix equivalents
- 25,660 to 79,040 LEs
- Up to 5,658,408 RAM bits available
- TriMatrix memory architecture consisting of three RAM block sizes to implement true dual-port memory and first-in-first-out (FIFO) buffers
- Embedded high-speed DSP blocks provide dedicated implementation of multipliers, multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device which provide identical features as the FPGA counterparts, including spread spectrum, programmable bandwidth, clock switchover, real-time PLL reconfiguration, advanced multiplication, and phase shifting
- Supports numerous single-ended and differential I/O standards
- Supports high-speed networking and communications bus standards including RapidIO™, UTOPIA IV, CSIX, HyperTransport technology, 10G Ethernet XSBI, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
- Differential on-chip termination support for LVDS

- Supports high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast-cycle RAM (FCRAM), and single data rate (SDR) SDRAM
- Support for multiple intellectual property (IP) megafunctions from Altera® MegaCore® functions, and Altera Megafunction Partners Program (AMPP<sup>SM</sup>) megafunctions
- Available in space-saving flip-chip FineLine BGA® and wire-bond packages (Tables 1–2 and 1–3)
- Optional emulation of original FPGA configuration sequence
- Optional instant-on power-up



The actual performance and power consumption improvements over the Stratix equivalents mentioned in this data sheet are design-dependent.

**Table 1–2. HardCopy Stratix Device Package Options and I/O Pin Counts**  
*Note (1)*

| Device | 672-Pin<br>FineLine BGA (2) | 780-Pin<br>FineLine BGA (3) | 1,020-Pin<br>FineLine BGA (3) |
|--------|-----------------------------|-----------------------------|-------------------------------|
| HC1S25 | 473                         |                             |                               |
| HC1S30 |                             | 597                         |                               |
| HC1S40 |                             | 613 (4)                     |                               |
| HC1S60 |                             |                             | 782                           |
| HC1S80 |                             |                             | 782                           |

**Notes to Table 1–2:**

- (1) Quartus II I/O pin counts include one additional pin, PLENA, which is not a general-purpose I/O pin. PLENA can only be used to enable the PLLs.
- (2) This device uses a wire-bond package.
- (3) This device uses a flip-chip package.
- (4) In the Stratix EP1S40F780 FPGA, the I/O pins U12 and U18 are general-purpose I/O pins. In the FPGA prototype, EP1S40F780\_HARDCOPY\_FPGA\_PROTOTYPE, and in the HardCopy Stratix HC1S40F780 device, U12 and U18 must be connected to ground. The EP1S40F780\_HARDCOPY\_FPGA\_PROTOTYPE and HC1S40F780 pin-outs are identical.

**Table 1–3. HardCopy Stratix Device Package Sizes**

| Device                      | 672-Pin<br>FineLine BGA | 780-Pin<br>FineLine BGA | 1,020-Pin<br>FineLine BGA |
|-----------------------------|-------------------------|-------------------------|---------------------------|
| Pitch (mm)                  | 1.00                    | 1.00                    | 1.00                      |
| Area (mm <sup>2</sup> )     | 729                     | 841                     | 1,089                     |
| Length × width<br>(mm × mm) | 27 × 27                 | 29 × 29                 | 33 × 33                   |

## Document Revision History

Table 1–4 shows the revision history for this chapter.

**Table 1–4. Document Revision History**

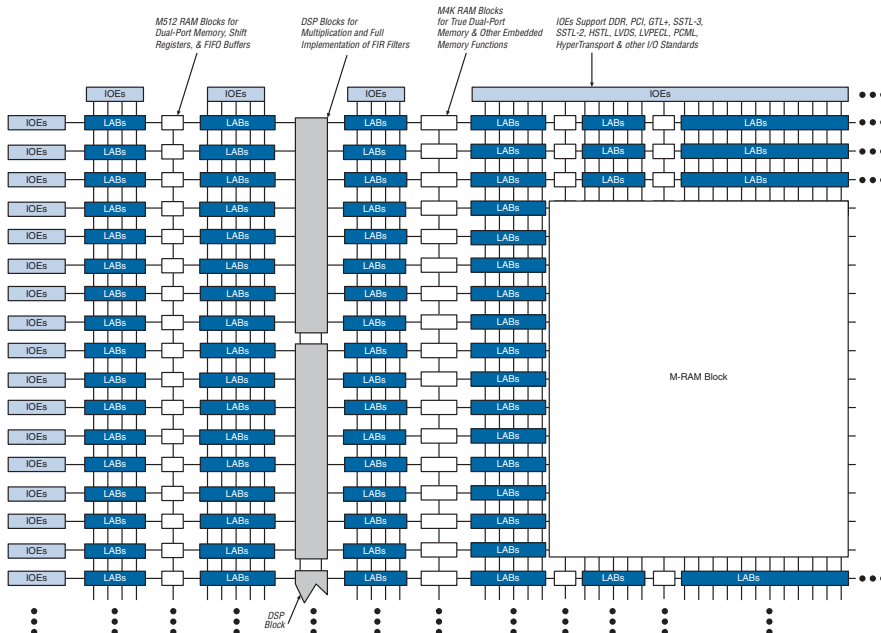
| Date and Document Version | Changes Made                                                                                                             | Summary of Changes |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------|--------------------|
| September 2008 v2.4       | Revised chapter number and metadata.                                                                                     | —                  |
| June 2007 v2.3            | Updated Introduction section.<br>Updated Table 1–2.                                                                      | —                  |
| December 2006 v2.2        | Updated revision history.                                                                                                | —                  |
| March 2006                | Formerly chapter 5; no content change.                                                                                   | —                  |
| October 2005 v2.1         | Minor edits                                                                                                              | —                  |
| January 2005 v2.0         | Minor edits                                                                                                              | —                  |
| June 2003 v1.0            | Initial release of Chapter 5, <i>Introduction to HardCopy Stratix Devices</i> , in the <i>HardCopy Device Handbook</i> . | —                  |

### Introduction

HardCopy® Stratix® structured ASICs provide a comprehensive alternative to ASICs. The HardCopy Stratix device family is fully supported by the Quartus® II design software, and, combined with a vast intellectual property (IP) portfolio, provides a complete path from prototype to volume production. Designers can now procure devices, tools, and Altera® IP for their high-volume applications.

As shown in Figure 2-1, HardCopy Stratix devices preserve their Stratix FPGA counterpart's architecture, but the programmability for logic, memory, and interconnect is removed. HardCopy Stratix devices are also manufactured in the same process technology and process voltage as Stratix FPGAs. Removing all configuration and programmable routing resources and replacing it with direct metal interconnect results in considerable die size reduction and the ensuing cost savings.

**Figure 2-1. HardCopy Stratix Device Architecture**



The HardCopy Stratix family consists of base arrays that are common to all designs for a particular device density. Design-specific customization is done within the top two metal layers. The base arrays use an area-efficient sea-of-logic-elements (SOLE) core and extend the flexibility of high-density Stratix FPGAs to a cost-effective, high-volume production solution. With a seamless migration process employed in numerous successful designs, functionality-verified Stratix FPGA designs can be migrated to fixed-function HardCopy Stratix devices with minimal risk and guaranteed first-time success.

The SRAM configuration cells of the original Stratix devices are replaced in HardCopy Stratix devices by metal connects, which define the function of each logic element (LE), digital signal processing (DSP) block, phase-locked loop (PLL), embedded memory, and I/O cell in the device. These resources are interconnected using metallization layers. Once a HardCopy Stratix device has been manufactured, the functionality of the device is fixed and no re-programming is possible. However, as is the case with Stratix FPGAs, the PLLs can be dynamically configured in HardCopy Stratix devices.

## HardCopy Stratix and Stratix FPGA Differences

To ensure HardCopy Stratix device functionality and performance, designers should thoroughly test the original Stratix FPGA-based design for satisfactory results before committing the design for migration to a HardCopy Stratix device. Unlike Stratix FPGAs, HardCopy Stratix devices are customized at the time of manufacturing and therefore do not have programmability support.

Since HardCopy Stratix devices are customized within the top two metal layers, no configuration circuitry is required. Refer to [“Power-Up Modes in HardCopy Stratix Devices” on page 2–7](#) for more information.

Depending on the design, HardCopy Stratix devices can provide, on average, a 50% performance improvement over equivalent Stratix FPGAs. The performance improvement is achieved by die size reduction, metal interconnect optimization, and customized signal buffering. HardCopy Stratix devices consume, on average, 40% less power than their equivalent Stratix FPGAs.



Designers can use the Quartus II software to design HardCopy Stratix devices, estimate performance and power consumption, and maximize system throughput.

Table 2–1 illustrates the differences between HardCopy Stratix and Stratix devices.

| <b>HardCopy Stratix</b>                                                                                                                         | <b>Stratix</b>                                                                                                                            |
|-------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| Customized device. All reprogrammability support is removed and no configuration is required.                                                   | Re-programmable with configuration is required upon power-up.                                                                             |
| Average of 50% performance improvement over corresponding FPGA (1).                                                                             | High-performance FPGA.                                                                                                                    |
| Average of 40% less power consumption compared to corresponding FPGA (1).                                                                       | Standard FPGA power consumption.                                                                                                          |
| Contact Altera for information regarding specific IP support.                                                                                   | IP support for all devices is available.                                                                                                  |
| Double data rate (DDR) SDRAM maximum operating frequency is pending characterization.                                                           | DDR SDRAM can operate at 200 MHz for -5 speed grade devices.                                                                              |
| All routing connections are direct and all unused routing is removed.                                                                           | MultiTrack™ routing stitches together routing resources to provide a path.                                                                |
| HC1S30 and HC1S40 devices have two M-RAM blocks. HC1S80 devices have six M-RAM blocks.                                                          | EP1S30 and EP1S40 devices have four M-RAM blocks. EP1S80 devices have nine M-RAM blocks.                                                  |
| It is not possible to initialize M512 and M4K RAM contents during power-up.                                                                     | The contents of M512 and M4K RAM blocks can be preloaded during configuration with data specified in a memory initialization file (.mif). |
| The contents of memory output registers are unknown after power-on reset (POR).                                                                 | The contents of memory output registers are initialized to '0' after POR.                                                                 |
| HC1S30 and HC1S40 devices have six PLLs.                                                                                                        | HC1S30 devices have 10 PLLs. HC1S40 devices have 12 PLLs.                                                                                 |
| PLL dynamic reconfiguration uses ROM for information. This reconfiguration is performed in the back-end and does not affect the migration flow. | PLL dynamic reconfiguration uses a MIF to initialize a RAM resource with information.                                                     |
| The I/O elements (IOEs) are equivalent but not identical to FPGA IOEs due to slight design optimizations for HardCopy devices.                  | The IOEs are optimized for the FPGA architecture.                                                                                         |

**Table 2–1. HardCopy Stratix and Stratix Device Comparison (Part 2 of 2)**

| HardCopy Stratix                                                                                                            | Stratix                                                                                                        |
|-----------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|
| The I/O drive strength for single-ended I/O pins are slightly different and is modeled in the HardCopy Stratix IBIS models. | The I/O drive strength for single-ended I/O pins are found in Stratix IBIS models.                             |
| In the HC1S40 780-pin FineLine BGA® device, the I/O pins U12 and U18 must be connected to ground.                           | In the HC1S40 780-pin FineLine BGA device, the I/O pins U12 and U18 are available as general-purpose I/O pins. |
| The BSDL file describes re-ordered Joint Test Action Group (JTAG) boundary-scan chains.                                     | The JTAG boundary-scan chain is defined in the BSDL file.                                                      |

*Note to Table 2–1:*

- (1) Performance and power consumption are design dependant.

## Logic Elements

Logic is implemented in HardCopy Stratix devices using the same architectural units as the Stratix device family. The basic unit is the logic element (LE) with logic array blocks (LAB) consisting of 10 LEs. The implementation of LEs and LABs is identical to the Stratix device family.

In the HardCopy Stratix device family, all extraneous routing resources not essential to the specific design are removed for performance and die size efficiency. Therefore, the MultiTrack interconnect for routing implementation between LABs and other device resources in the Stratix device family is no longer necessary in the HardCopy Stratix device family.

Table 2–2 illustrates the differences between HardCopy Stratix and Stratix logic.

**Table 2–2. HardCopy Stratix and Stratix Logic Comparison**

| HardCopy Stratix                                                      | Stratix                                                                   |
|-----------------------------------------------------------------------|---------------------------------------------------------------------------|
| All routing connections are direct and all unused routing is removed. | MultiTrack routing stitches routing resources together to provide a path. |

## Embedded Memory

TriMatrix™ memory blocks from Stratix devices, including M512, M4K, and M-RAM memory blocks, are available in HardCopy Stratix devices. Embedded memory is seamlessly implemented in the equivalent resource.

Although memory resource implementation is equivalent, the number of specific M-RAM blocks are not necessarily the same between corresponding Stratix and HardCopy Stratix devices. [Table 2-3](#) shows the number of M-RAM blocks available in each device.

**Table 2-3. HardCopy Stratix and Stratix M-RAM Block Comparison**

| HardCopy Stratix |              | Stratix |              |
|------------------|--------------|---------|--------------|
| Device           | M-RAM Blocks | Device  | M-RAM Blocks |
| HC1S25           | 2            | EP1S25  | 2            |
| HC1S30           | 2            | EP1S30  | 4            |
| HC1S40           | 2            | EP1S40  | 4            |
| HC1S60           | 6            | EP1S60  | 6            |
| HC1S830          | 6            | EP1S830 | 9            |

In HardCopy Stratix devices, it is not possible to preload RAM contents using a MIF after powering up; the output registers of memory blocks will have unknown values. This occurs because there is no configuration process that is executed.



Violating the setup or hold time requirements on address registers could corrupt the memory contents. This requirement applies to both read and write operations.

[Table 2-4](#) illustrates the differences between HardCopy Stratix and Stratix memory.

**Table 2-4. HardCopy Stratix and Stratix Memory Comparison**

| HardCopy Stratix                                                                       | Stratix                                                                                                     |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| HC1S30 and HC1S40 devices have two M-RAM blocks. HC1S80 devices have six M-RAM blocks. | EP1S30 and EP1S40 devices have four M-RAM blocks. EP1S80 devices have nine M-RAM blocks.                    |
| It is not possible to initialize M512 and M4k RAM contents during power-up.            | The contents of M512 and M4K RAM blocks can be preloaded during configuration with data specified in a MIF. |
| The contents of memory output registers are unknown after POR.                         | The contents of memory output registers are initialized to '0' after POR.                                   |

## DSP Blocks

DSP blocks in HardCopy Stratix devices are architecturally identical to those in Stratix devices. The number of DSP blocks available in HardCopy Stratix devices matches the number of DSP blocks available in the corresponding Stratix device.

## PLLs and Clock Networks

The PLLs in HardCopy Stratix devices are identical to those in Stratix devices. The clock networks are also implemented exactly as they are in Stratix devices. The number of PLLs can vary between corresponding Stratix and HardCopy Stratix devices. [Table 2-5](#) shows the number of PLLs available in each device.

**Table 2-5. HardCopy Stratix and Stratix PLL Comparison**

| HardCopy Stratix |      | Stratix |      |
|------------------|------|---------|------|
| Device           | PLLs | Device  | PLLs |
| HC1S25           | 6    | EP1S25  | 6    |
| HC1S30           | 6    | EP1S30  | 10   |
| HC1S40           | 6    | EP1S40  | 12   |
| HC1S60           | 12   | EP1S60  | 12   |
| EP1S830          | 12   | EP1S830 | 12   |

[Table 2-6](#) illustrates the differences between HardCopy Stratix and Stratix PLLs.

**Table 2-6. HardCopy Stratix and Stratix PLL Differences**

| HardCopy Stratix                                                                                                                                | Stratix                                                                               |
|-------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| HC1S30 and HC1S40 devices have six PLLs.                                                                                                        | HC1S30 devices have 10 PLLs.<br>HC1S40 devices have 12 PLLs.                          |
| PLL dynamic reconfiguration uses ROM for information. This reconfiguration is performed in the back-end and does not affect the migration flow. | PLL dynamic reconfiguration uses a MIF to initialize a RAM resource with information. |

## I/O Structure and Features

The HardCopy Stratix IOEs are equivalent, but not identical to, the Stratix FPGA IOEs. This is due to the reduced die size, layout difference, and metal customization of the HardCopy Stratix device. The differences are minor but may be relevant to customers designing with tight DC and switching characteristics. However, no signal integrity concerns are introduced with HardCopy Stratix IOEs.

When designing with very tight timing constraints (for example, DDR or quad data rate [QDR]), or if using the programmable drive strength option, Altera recommends verifying final drive strength using updated IBIS models located on the Altera website at [www.altera.com](http://www.altera.com). Differential I/O standards are unaffected.

I/O pin placement and  $V_{REF}$  pin placement rules are identical between HardCopy Stratix and Stratix devices. Unused pin settings will carry over from Stratix device settings and are implemented as tri-stated outputs driving ground or outputs driving  $V_{CC}$ .

In Stratix EP1S40 780-pin FineLine BGA FPGAs, the I/O pins U12 and U18 are available as general-purpose I/O pins. In the FPGA prototype, EP1S40F780\_HARDCOPY\_FPGA\_PROTOTYPE, and in the Hardcopy Stratix HC1S40 780-pin FineLine BGA device, the I/O pins U12 and U18 must be connected to ground. HC1S40 780-pin FineLine BGA and EP1S40F780\_HARDCOPY\_FPGA\_PROTOTYPE pin-outs are identical.

Table 2-7 illustrates the differences between HardCopy Stratix and Stratix I/O pins.

| <i>Table 2-7. HardCopy Stratix and Stratix I/O Pin Comparison</i>                                                          |                                                                                                                |
|----------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|
| <b>HardCopy Stratix</b>                                                                                                    | <b>Stratix</b>                                                                                                 |
| The IOEs are equivalent, but not identical to, the FPGA IOEs due to slight design optimizations for HardCopy devices.      | IOEs are optimized for the FPGA architecture.                                                                  |
| The I/O drive strength for single-ended I/O pins are slightly different and are found in the HardCopy Stratix IBIS models. | The I/O drive strength for single-ended I/O pins are found in Stratix IBIS models.                             |
| In the HC1S40 780-pin FineLine BGA device, the I/O pins U12 and U18 must be connected to ground.                           | In the EP1S40 780-pin FineLine BGA device, the I/O pins U12 and U18 are available as general-purpose I/O pins. |

## Power-Up Modes in HardCopy Stratix Devices

Designers do not need to configure HardCopy Stratix devices, unlike their FPGA counterparts. However, to facilitate seamless migration, configuration can be emulated in HardCopy Stratix devices.

The modes in which a HardCopy Stratix device can be made ready for operation after power-up are: instant on, instant on after 50 ms, and configuration emulation. These modes are briefly described below.

- In instant on mode, the HardCopy Stratix device is available for use shortly after the device receives power. The on-chip POR circuit resets all registers. The `CONF_DONE` output is tri-stated once the POR has elapsed. No configuration device or configuration data is necessary.
- In instant on after 50 ms mode, the HardCopy Stratix device performs in a fashion similar to the instant on mode, except that there is an additional delay of 50 ms, during which time the device is held in reset stage. The `CONF_DONE` output is pulled low during this time, and then tri-stated after the 50 ms have elapsed. No configuration device or configuration data is necessary for this option.
- In configuration emulation mode, the HardCopy series device emulates the behavior of an APEX or Stratix FPGA during its configuration phase. When this mode is used, the HardCopy device uses a configuration emulation circuit to receive configuration bit streams. When all the configuration data is received, the HardCopy series device transitions into an initialization phase and releases the `CONF_DONE` pin to be pulled high. Pulling the `CONF_DONE` pin high signals that the HardCopy series device is ready for normal operation. If the optional open-drain `INIT_DONE` output is used, the normal operation is delayed until this signal is released by the HardCopy series device.



HardCopy II and some HardCopy Stratix devices do not support configuration emulation mode.

Instant on and instant on after 50 ms modes are the recommended power-up modes because these modes are similar to an ASIC's functionality upon power-up. No changes to the existing board design or the configuration software are required.

All three modes provide significant benefits to system designers. They enable seamless migration of the design from the FPGA device to the HardCopy device with no changes to the existing board design or the configuration software. The pull-up resistors on `nCONFIG`, `nSTATUS`, and `CONF_DONE` should be left on the printed circuit board.



For more information, refer to the *HardCopy Series Configuration Emulation* chapter in the *HardCopy Series Handbook*.

## Hot Socketing

HardCopy Stratix devices support hot socketing without any external components. In a hot socketing situation, a device's output buffers are turned off during system power up or power down. To simplify board design, HardCopy Stratix devices support any power-up or power-down sequence ( $V_{CCIO}$  and  $V_{CCINT}$ ). For mixed-voltage environments, you can

drive signals into the device before or during power up or power down without damaging the device. HardCopy Stratix devices do not drive out until they have attained proper operating conditions.

You can power up or power down the  $V_{CCIO}$  and  $V_{CCINT}$  pins in any sequence. The power supply ramp rates can range from 100 ns to 100 ms. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

- The hot socketing DC specification is  $|I_{IOPIN}| < 300 \mu\text{A}$ .
- The hot socketing AC specification is  $|I_{IOPIN}| < 8 \text{ mA}$  for 10 ns or less. This specification takes into account the pin capacitance only. Additional capacitance for trace, connector, and loading needs to be taken into consideration separately.  $I_{IOPIN}$  is the current at any user I/O pin on the device.



The DC specification applies when all  $V_{CC}$  supplies to the device are stable in the powered-up or powered-down conditions. For the AC specification, the peak current duration due to power-up transients is 10 ns or less.

## HARDCOPY\_ FPGA\_ PROTOTYPE Devices

HARDCOPY\_FPGA\_PROTOTYPE devices are Stratix FPGAs available for designers to prototype their HardCopy Stratix designs and perform in-system verification before migration to a HardCopy Stratix device. The HARDCOPY\_FPGA\_PROTOTYPE devices have the same available resources as in the final HardCopy Stratix devices.

The Quartus II software version 4.1 and later contains the latest timing models. For designs with tight timing constraints, Altera strongly recommends compiling the design with the Quartus II software version 4.1 or later. To properly verify I/O features, it is important to design with the HARDCOPY\_FPGA\_PROTOTYPE device option prior to migrating to a HardCopy Stratix device.



Some HARDCOPY\_FPGA\_PROTOTYPE devices, as indicated in Table 2–8, have fewer M-RAM blocks compared to the equivalent Stratix FPGAs. The selective removal of these resources provides a significant price benefit to designers using HardCopy Stratix devices.

**Table 2–8. M-RAM Block Comparison Between Various Devices**

| Number of LEs | HARDCOPY_FPGA_PROTOTYPE Devices |              | HardCopy Stratix Devices |              | Stratix Devices |              |
|---------------|---------------------------------|--------------|--------------------------|--------------|-----------------|--------------|
|               | Device                          | M-RAM Blocks | Device                   | M-RAM Blocks | Device          | M-RAM Blocks |
| 25,660        | EP1S25                          | 2            | HC1S25                   | 2            | EP1S25          | 2            |
| 32,470        | EP1S30                          | 2            | HC1S30                   | 2            | EP1S30          | 4            |
| 41,250        | EP1S40                          | 2            | HC1S40                   | 2            | EP1S40          | 4            |
| 57,120        | EP1S60                          | 6            | HC1S60                   | 6            | EP1S60          | 6            |
| 79,040        | EP1S830                         | 6            | HC1S830                  | 6            | EP1S830         | 9            |



For more information about how the various features in the Quartus II software can be used for designing HardCopy Stratix devices, refer to the *Quartus II Support for HardCopy Stratix Devices* chapter of the *HardCopy Series Handbook*.

HARDCOPY\_FPGA\_PROTOTYPE FPGA devices have the identical speed grade as the equivalent Stratix FPGAs. However, HardCopy Stratix devices are customized and do not have any speed grading. HardCopy Stratix devices, on an average, can be 50% faster than their equivalent HARDCOPY\_FPGA\_PROTOTYPE devices. The actual improvement is design-dependent.

## Document Revision History

Table 2–9 shows the revision history for this chapter.

**Table 2–9. Document Revision History (Part 1 of 2)**

| Date and Document Version | Changes Made                                                                                                                                                                   | Summary of Changes |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| September 2008 v3.4       | Revised chapter number and metadata.                                                                                                                                           | —                  |
| June 2007 v3.3            | <ul style="list-style-type: none"> <li>● Updated Table 2–1.</li> <li>● Added note to the “Embedded Memory” section.</li> <li>● Updated the “Hot Socketing” section.</li> </ul> | —                  |

**Table 2–9. Document Revision History (Part 2 of 2)**

| Date and Document Version | Changes Made                                                                                                                                                                                                                                                                                                      | Summary of Changes |
|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| December 2006<br>v3.2     | Updated revision history.                                                                                                                                                                                                                                                                                         | —                  |
| March 2006                | Formerly chapter 6; no content change.                                                                                                                                                                                                                                                                            | —                  |
| October 2005 v3.1         | <ul style="list-style-type: none"> <li>● Minor edits</li> <li>● Updated graphics</li> </ul>                                                                                                                                                                                                                       | Minor edits.       |
| May 2005<br>v3.0          | <ul style="list-style-type: none"> <li>● Added Table 6-1</li> <li>● Added the Logic Elements section</li> <li>● Added the Embedded Memory section</li> <li>● Added the DSP Blocks section</li> <li>● Added the PLLs and Clock Networks section</li> <li>● Added the I/O Structure and Features section</li> </ul> | Minor update.      |
| January 2005<br>v2.0      | <ul style="list-style-type: none"> <li>● Added summary of I/O and timing differences between Stratix FPGAs and HardCopy Stratix devices</li> <li>● Removed section on Quartus II support of HardCopy Stratix devices</li> <li>● Added “Hot Socketing” section</li> </ul>                                          | Minor update.      |
| August 2003<br>v1.1       | Edited section headings’ hierarchy.                                                                                                                                                                                                                                                                               | Minor edits.       |
| June 2003<br>v1.0         | Initial release of Chapter 6, Description, Architecture and Features, in the <i>HardCopy Device Handbook</i>                                                                                                                                                                                                      | —                  |





## 3. Boundary-Scan Support

H51004-3.4

### IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All HardCopy® Stratix® structured ASICs provide JTAG boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1-1990 specification. The BST architecture offers the capability to efficiently test components on printed circuit boards (PCBs) with tight lead spacing by testing pin connections, without using physical test probes, and capturing functional data while a device is in normal operation. Boundary-scan cells in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results.

A device using the JTAG interface uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. HardCopy Stratix devices support the JTAG instructions as shown in [Table 3-1](#).

**Table 3-1. HardCopy Stratix JTAG Instructions (Part 1 of 2)**

| JTAG Instruction | Instruction Code | Description                                                                                                                                                                                                                        |
|------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SAMPLE/PRELOAD   | 00 0000 0101     | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.                                                   |
| EXTEST (1)       | 00 0000 0000     | Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.                                                                |
| BYPASS           | 11 1111 1111     | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.                                        |
| USERCODE         | 00 0000 0111     | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.                                                                                          |
| IDCODE           | 00 0000 0110     | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.                                                                                                              |
| HIGHZ (1)        | 00 0000 1011     | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins. |

**Table 3–1. HardCopy Stratix JTAG Instructions (Part 2 of 2)**

| JTAG Instruction | Instruction Code | Description                                                                                                                                                                                                                                                                     |
|------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLAMP (1)        | 00 0000 1010     | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register. |

**Note to Table 3–1:**

- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.



The boundary-scan description language (BSDL) files for HardCopy Stratix devices are different from the corresponding Stratix FPGAs. The BSDL files for HardCopy Stratix devices are available for download from the Altera website at [www.altera.com](http://www.altera.com).

The HardCopy Stratix device instruction register length is 10 bits; the USERCODE register length is 32 bits. The USERCODE registers are mask-programmed, so they are not re-programmable. The designer can choose an appropriate 32-bit sequence to program into the USERCODE registers.

Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for HardCopy Stratix devices.

**Table 3–2. HardCopy Stratix Boundary-Scan Register Length**

| Device                        | Maximum Boundary-Scan Register Length |
|-------------------------------|---------------------------------------|
| HC1S25 672-pin FineLine BGA   | 1,458                                 |
| HC1S30 780-pin FineLine BGA   | 1,878                                 |
| HC1S40 780-pin FineLine BGA   | 1,878                                 |
| HC1S60 1,020-pin FineLine BGA | 2,382                                 |
| HC1S80 1,020-pin FineLine BGA | 2,382                                 |

**Table 3–3. 32-Bit HardCopy Stratix Device IDCODE**

| Device | IDCODE (32 Bits) (1) |                       |                                 |                 |
|--------|----------------------|-----------------------|---------------------------------|-----------------|
|        | Version (4 Bits)     | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | LSB (1 Bit) (2) |
| HC1S25 | 0000                 | 0010 0000 0000 0011   | 000 0110 1110                   | 1               |
| HC1S30 | 0000                 | 0010 0000 0000 0100   | 000 0110 1110                   | 1               |
| HC1S40 | 0000                 | 0010 0000 0000 0101   | 000 0110 1110                   | 1               |
| HC1S60 | 0000                 | 0010 0000 0000 0110   | 000 0110 1110                   | 1               |
| HC1S80 | 0000                 | 0010 0000 0000 0111   | 000 0110 1110                   | 1               |

**Notes to Table 3–3:**

- (1) The most significant bit (MSB) is on the left.
- (2) The IDCODE's least significant bit (LSB) is always 1.

Figure 3–1 shows the timing requirements for the JTAG signals.

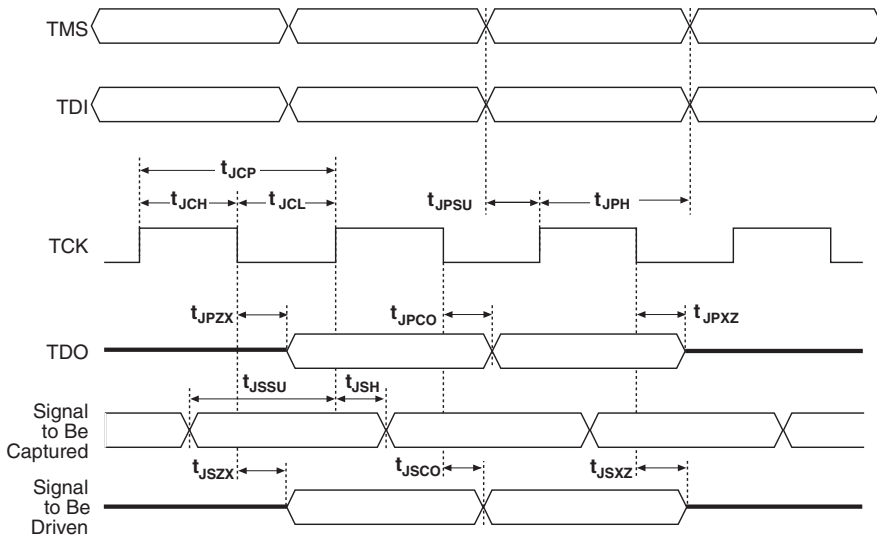
**Figure 3–1. HardCopy Stratix JTAG Waveforms**

Table 3–4 shows the JTAG timing parameters and values for HardCopy Stratix devices.

**Table 3–4. HardCopy Stratix JTAG Timing Parameters and Values**

| Symbol     | Parameter                                      | Min | Max | Unit |
|------------|------------------------------------------------|-----|-----|------|
| $t_{JCP}$  | TCK clock period                               | 100 |     | ns   |
| $t_{JCH}$  | TCK clock high time                            | 50  |     | ns   |
| $t_{JCL}$  | TCK clock low time                             | 50  |     | ns   |
| $t_{JPSU}$ | JTAG port setup time                           | 20  |     | ns   |
| $t_{JPH}$  | JTAG port hold time                            | 45  |     | ns   |
| $t_{JPCO}$ | JTAG port clock to output                      |     | 25  | ns   |
| $t_{JPZX}$ | JTAG port high impedance to valid output       |     | 25  | ns   |
| $t_{JPXZ}$ | JTAG port valid output to high impedance       |     | 25  | ns   |
| $t_{JSSU}$ | Capture register setup time                    | 20  |     | ns   |
| $t_{JSH}$  | Capture register hold time                     | 45  |     | ns   |
| $t_{JSCO}$ | Update register clock to output                |     | 35  | ns   |
| $t_{JSZX}$ | Update register high impedance to valid output |     | 35  | ns   |
| $t_{JSXZ}$ | Update register valid output to high impedance |     | 35  | ns   |



For more information on JTAG, refer to *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*.

## Document Revision History

Table 3–5 shows the revision history for this chapter.

**Table 3–5. Document Revision History (Part 1 of 2)**

| Date and Document Version | Changes Made                           | Summary of Changes |
|---------------------------|----------------------------------------|--------------------|
| September 2008 v3.4       | Updated chapter number and metadata.   | —                  |
| June 2007 v3.3            | Updated <a href="#">Figure 3–1</a> .   | —                  |
| December 2006 v3.2        | Updated revision history.              | —                  |
| March 2006                | Formerly chapter 7; no content change. | —                  |

**Table 3–5. Document Revision History (Part 2 of 2)**

| Date and Document Version | Changes Made                                                                                | Summary of Changes |
|---------------------------|---------------------------------------------------------------------------------------------|--------------------|
| October 2005 v3.1         | <ul style="list-style-type: none"><li>• Minor edits</li><li>• Graphic updates</li></ul>     | —                  |
| May 2005 v3.0             | Updated “IEEE Std. 1149.1 (JTAG) Boundary-Scan Support” section                             |                    |
| January 2005 v2.0         | Added information about <code>USERCODE</code> registers                                     |                    |
| June 2003 v1.0            | Initial release of Chapter 7, Boundary-Scan Support, in the <i>HardCopy Device Handbook</i> |                    |





## 4. Operating Conditions

H51005-3.4

### Recommended Operating Conditions

Tables 4–1 through 4–3 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.5-V HardCopy® Stratix® devices.

**Table 4–1. HardCopy Stratix Device Absolute Maximum Ratings** Notes (1), (2)

| Symbol      | Parameter                  | Conditions              | Minimum | Maximum | Unit |
|-------------|----------------------------|-------------------------|---------|---------|------|
| $V_{CCINT}$ | Supply voltage             | With respect to ground  | –0.5    | 2.4     | V    |
| $V_{CCIO}$  |                            |                         | –0.5    | 4.6     | V    |
| $V_I$       | DC input voltage (3)       |                         | –0.5    | 4.6     | V    |
| $I_{OUT}$   | DC output current, per pin |                         | –25     | 40      | mA   |
| $T_{STG}$   | Storage temperature        | No bias                 | –65     | 150     | °C   |
| $T_J$       | Junction temperature       | BGA packages under bias |         | 135     | °C   |

**Table 4–2. HardCopy Stratix Device Recommended Operating Conditions**

| Symbol      | Parameter                                           | Conditions         | Minimum      | Maximum      | Unit |
|-------------|-----------------------------------------------------|--------------------|--------------|--------------|------|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | (4)                | 1.425        | 1.575        | V    |
| $V_{CCIO}$  | Supply voltage for output buffers, 3.3-V operation  | (4), (5)           | 3.00 (3.135) | 3.60 (3.465) | V    |
|             | Supply voltage for output buffers, 2.5-V operation  | (4)                | 2.375        | 2.625        | V    |
|             | Supply voltage for output buffers, 1.8-V operation  | (4)                | 1.71         | 1.89         | V    |
|             | Supply voltage for output buffers, 1.5-V operation  | (4)                | 1.4          | 1.6          | V    |
| $V_I$       | Input voltage                                       | (3), (6)           | –0.5         | 4.1          | V    |
| $V_O$       | Output voltage                                      |                    | 0            | $V_{CCIO}$   | V    |
| $T_J$       | Operating junction temperature                      | For commercial use | 0            | 85           | °C   |
|             |                                                     | For industrial use | –40          | 100          | °C   |