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HC55120, HC55121, HC55130, HC55140, HC55142, HC55143, HC55150

June 1, 2006 FN4659.13

Low Power UniSLIC14 Family

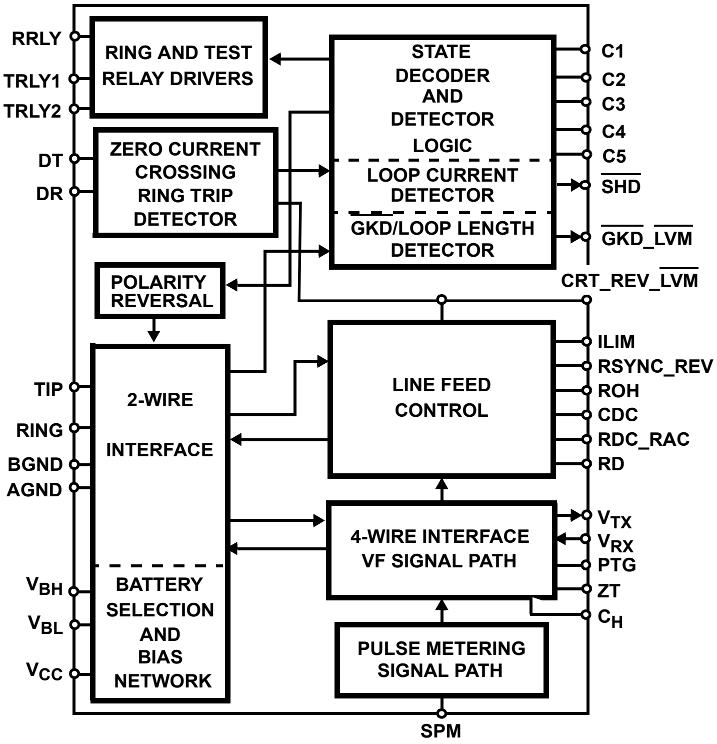
The UniSLIC14 is a family of Ultra Low Power SLICs. The feature set and common pinouts of the UniSLIC14 family positions it as a universal solution for: Plain Old Telephone Service (POTS), PBX, Central Office, Loop Carrier, Fiber in the Loop, ISDN-TA and NT1+, Pairgain and Wireless Local Loop.

The UniSLIC14 family achieves its ultra low power operation through: Its automatic single and dual battery selection (based on line length) and battery tracking anti clipping to ensure the maximum loop coverage on the lowest battery voltage. This architecture is ideal for power critical applications such as ISDN NT1+, Pairgain and Wireless local loop products.

The UniSLIC14 family has many user programmable features. This family of SLICs delivers a low noise, low component count solution for Central Office and Loop Carrier universal voice grade designs. The product family integrates advanced pulse metering, test and signaling capabilities, and zero crossing ring control.

The UniSLIC14 family is designed in the Intersil "Latch" free Bonded Wafer process. This process dielectrically isolates the active circuitry to eliminate any leakage paths as found in our competition's JI process. This makes the UniSLIC14 family compliant with "hot plug" requirements and operation in harsh outdoor environments.

Block Diagram



Features

- Ultra Low Active Power (OHT) < 60mW
- Single/Dual Battery Operation
- Automatic Silent Battery Selection
- Power Management/Shutdown
- Battery Tracking Anti Clipping
- Single 5V Supply with 3V Compatible Logic
- Zero Crossing Ring Control
  - Zero Voltage On/Zero Current Off
- Tip/Ring Disconnect
- Pulse Metering Capability
- 4 Wire Loopback
- Programmable Current Feed
- Programmable Resistive Feed
- Programmable Loop Detect Threshold
- Programmable On-Hook and Off-Hook Overheads
- Programmable Overhead for Pulse Metering
- Programmable Polarity Reversal Time
- Selectable Transmit Gain 0dB/-6dB
- 2 Wire Impedance Set by Single Network
- Loop and Ground Key Detectors
- On-Hook Transmission
- Common Pinout
- Pb-Free Plus Anneal Available (RoHS Compliant)

- HC55121
  - Polarity Reversal
- HC55130
  - -63dB Longitudinal Balance
- HC55140
  - Polarity Reversal
  - Ground Start
  - Line Voltage Measurement
  - 2 Wire Loopback
  - -63dB Longitudinal Balance
- HC55142
  - Polarity Reversal
  - Ground Start
  - Line Voltage Measurement
  - 2.2V_{RMS} Pulse Metering
  - 2 Wire Loopback
- HC55150
  - Polarity Reversal
  - Line Voltage Measurement
  - 2.2V_{RMS} Pulse Metering
  - 2 Wire Loopback

Related Literature

- AN9871, User's Guide for UniSLIC14 Eval Board
- AN9903, UniSLIC14 and TI TCM38C17

Ordering Information

PART NUMBER*	MAX LOOP CURRENT (mA)	POLARITY REVERSAL	GND START	GND KEY	LINE VOLTAGE MEASUREMENT †	PULSE METERING	2 TEST RELAY DRIVERS	2 WIRE LOOP-BACK †	LONGITUDINAL BALANCE	TEMP RANGE (°C)	PKG. DWG. #
HC55120CB	30			•					53dB	0 to 70	M28.3 SOIC
HC55120CBZ Pb-free (Note)	30			•					53dB	0 to 70	M28.3 SOIC
HC55120CM	30			•					53dB	0 to 70	N28.45 PLCC
HC55120CMZ Pb-free (Note)	30			•					53dB	0 to 70	N28.45 PLCC
HC55121IB	30	•		•		•		•	53dB	-40 to 85	M28.3 SOIC
HC55121IBZ Pb-free (Note)	30	•		•		•		•	53dB	-40 to 85	M28.3 SOIC
HC55121IM	30	•		•		•		•	53dB	-40 to 85	N28.45 PLCC
HC55121IMZ Pb-free (Note)	30	•		•		•		•	53dB	-40 to 85	N28.45 PLCC
HC55130IB	45								63dB	-40 to 85	M28.3 SOIC
HC55130IB96 (Tape and Reel)	45								63dB	-40 to 85	M28.3 SOIC
HC55130IBZ Pb-free (Note)	45								63dB	-40 to 85	M28.3 SOIC
HC55130IBZ96 (Tape and Reel) Pb-free (Note)	45								63dB	-40 to 85	M28.3 SOIC
HC55130IM	45								63dB	-40 to 85	N28.45 PLCC
HC55130IMZ Pb-free (Note)	45								63dB	-40 to 85	N28.45 PLCC
HC55140IB	45	•	•	•	•			•	63dB	-40 to 85	M28.3 SOIC
HC55140IBZ Pb-free (Note)	45	•	•	•	•			•	63dB	-40 to 85	M28.3 SOIC
HC55140IM	45	•	•	•	•			•	63dB	-40 to 85	N28.45 PLCC
HC55140IMZ Pb-free (Note)	45	•	•	•	•			•	63dB	-40 to 85	N28.45 PLCC
HC55142IB	45	•	•	•	•	•		•	63dB	-40 to 85	M28.3 SOIC
HC55142IBZ Pb-free (Note)	45	•	•	•	•	•		•	63dB	-40 to 85	M28.3 SOIC
HC55142IM	45	•	•	•	•	•		•	63dB	-40 to 85	N28.45 PLCC
HC55142IM96 (Tape and Reel)	45	•	•	•	•	•		•	63dB	-40 to 85	N28.45 PLCC
HC55142IMZ Pb-free (Note)	45	•	•	•	•	•		•	63dB	-40 to 85	N28.45 PLCC
HC55142IMZ96 (Tape and Reel) Pb-free (Note)	45	•	•	•	•	•		•	63dB	-40 to 85	N28.45 PLCC

Ordering Information (Continued)

PART NUMBER*	MAX LOOP CURRENT (mA)	POLARITY REVERSAL	GND START	GND KEY	LINE VOLTAGE MEASUREMENT †	PULSE METERING	2 TEST RELAY DRIVERS	2 WIRE LOOP-BACK †	LONGITUDINAL BALANCE	TEMP RANGE (°C)	PKG. DWG. #
HC55143IM	45	•	•	•	•	•	•	•	63dB	-40 to 85	N32.45x55 PLCC
HC55143IMZ Pb-free (Note)	45	•	•	•	•	•	•	•	63dB	-40 to 85	N32.45x55 PLCC
HC55150CB	45	•			•	•		•	55dB	0 to 70	M28.3 SOIC
HC55150CBZ Pb-free (Note)	45	•			•	•		•	55dB	0 to 70	M28.3 SOIC
HC55150CM	45	•			•	•		•	55dB	0 to 70	N28.45 PLCC
HC55150CMZ Pb-free (Note)	45	•			•	•		•	55dB	0 to 70	N28.45 PLCC
HC5514XEVAL1	Evaluation board										

† Available by placing SLIC in Test mode.

*Part marking is the same as the part number on all parts.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Device Operating Modes

C3	C2	C1	DESCRIPTION	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
0	0	0	Open Circuit 4-Wire Loopback	•	•	•	•	•	•
0	0	1	Ringing	•	•	•	•	•	•
0	1	0	Forward Active	•	•	•	•	•	•
0	1	1	Test Forward Active 2 Wire Loopback and Line Voltage Measurement		•		•	•	•
1	0	0	Tip Open Ground Start				•	•	
1	0	1	Reserved	•	•	•	•	•	•
1	1	0	Reverse Active		•		•	•	•
1	1	1	Test Reverse Active Line Voltage Measurement				•	•	•

Absolute Maximum Ratings $T_A = 25°C$

Temperature, Humidity	
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	-40°C to 110°C
Operating Junction Temperature Range	-40°C to 150°C
Power Supply ($-40°C \le T_A \le 85°C$)	
Supply Voltage V_{CC} to GND	-0.4V to 7V
Supply Voltage V_{BL} to GND	$-V_{BH}$ to 0.4V
Supply Voltage V_{BH} to GND, Continuous	-75V to 0.4V
Supply Voltage V_{BH} to GND, 10ms	-80V to 0.4V
Relay Driver	
Ring Relay Supply Voltage	0V to 14V
Ring Relay Current	50mA
Digital Inputs, Outputs (C1, C2, C3, C4, C5, $\overline{\text{SHD}}$, $\overline{\text{GKD\_LVM}}$)	
Input Voltage	-0.4V to V_{CC}
Output Voltage ($\overline{\text{SHD}}$, $\overline{\text{GKD\_LVM}}$ Not Active)	-0.4V to V_{CC}
Output Current ($\overline{\text{SHD}}$, $\overline{\text{GKD\_LVM}}$)	5mA
ESD Rating	500V
Gate Count	543 Transistors, 51 Diodes
Tipx and Ringx Terminals ($-40°C \le T_A \le 85°C$)	
Tipx or Ringx Current	-100mA to 100mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}
28 Lead PLCC Package	52°C/W
28 Lead SOIC Package	45°C/W
32 Lead PLCC Package	66.2°C/W
Continuous Power Dissipation at 85°C	
28 Lead PLCC Package	1.5W
28 Lead SOIC Package	2.0W
32 Lead PLCC Package	1.4W
Lead Temperature (Soldering 10s)	300°C
(PLCC, SOIC - Lead Tips Only)	Derate above 70°C

Tip and Ring Terminals

Tipx or Ringx, Current, Pulse < 10ms, T_{REP} > 10s	2A
Tipx or Ringx, Current, Pulse < 1ms, T_{REP} > 10s	5A
Tipx or Ringx, Current, Pulse < 10μs, T_{REP} > 10s	15A
Tipx or Ringx, Current, Pulse < 1μs, T_{REP} > 10s	20A
Tipx or Ringx, Pulse < 250ns, T_{REP} > 10s	20A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Typical Operating Conditions

These represent the conditions under which the device was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient Temperature	HC55120, HC55150/1	0	-	70	°C
	HC55121, HC55130/1, HC55140/1, HC55142/3	-40	-	85	°C
V_{BH} with Respect to GND		-58	-	-8	V
V_{BL} with Respect to GND		V_{BH}	-	0	V
V_{CC} with Respect to GND		4.75	-	5.25	V

Electrical Specifications

T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = -24V, PTG = Open, R_{P1} = R_{P2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 50kΩ, RDC_RAC = 20kΩ, R_{OH} = 40kΩ, C_H = 0.1µF, C_{DC} = 4.7µF, $C_{RT/REV}$ = 0.47µF, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) Symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
2-WIRE PORT											
Overload Level, Off Hook Forward and Reverse	1% THD, I_{DCMET} ≥ 18mA (Note 2, Figure 1)	3.2	-	-	V_{PEAK}	Forward Only	•	Forward Only	•	•	•
Overload Level, On Hook Forward and Reverse	1% THD, IDCMET ≤ 5mA (Note 3, Figure 1)	1.3	-	-	V_{PEAK}	Forward Only	•	Forward Only	•	•	•
Input Impedance (Into Tip and Ring)		-	Z_T/200	-	Ω	•	•	•	•	•	•
Longitudinal Impedance (Tip, Ring) Forward and Reverse	0 < f < 100Hz (Note 4, Figure 2)	-	0	-	Ω/Wire	Forward Only	•	Forward Only	•	•	•
LONGITUDINAL CURRENT LIMIT (TIP, RING)											
On-Hook, Off-Hook (Active), R_L = 736Ω Forward and Reverse	No False Detections, (Loop Current), LB > 45dB (Notes 5, 6, Figures 3A, 3B)	28	-	-	mA_{RMS}/Wire	Forward Only	•	Forward Only	•	•	•

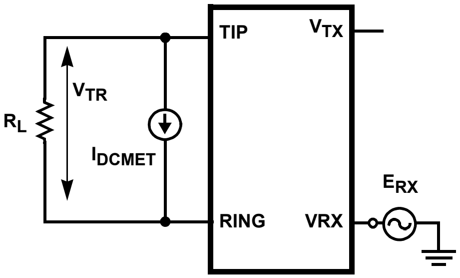


FIGURE 1. OVERLOAD LEVEL (OFF HOOK, ON HOOK)

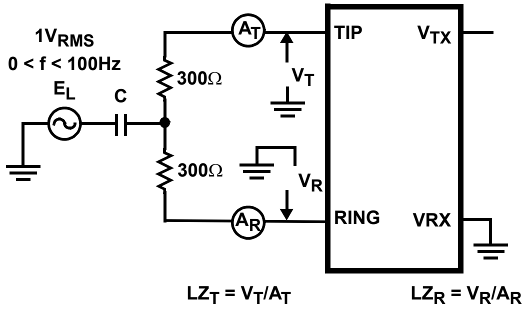


FIGURE 2. LONGITUDINAL IMPEDANCE

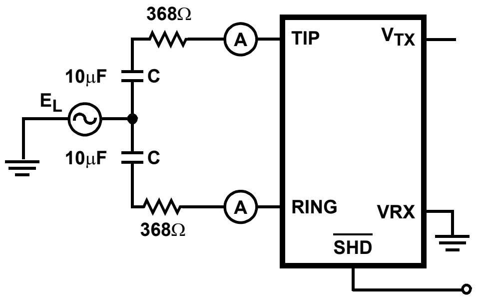


FIGURE 3A. LONGITUDINAL CURRENT LIMIT ON-HOOK (ACTIVE)

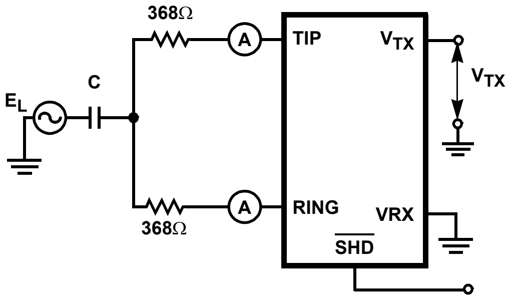


FIGURE 3B. LONGITUDINAL CURRENT LIMIT OFF-HOOK (ACTIVE)

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = -24V, PTG = Open, R_{P1} = R_{P2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 50kΩ, RDC_RAC = 20kΩ, R_{OH} = 40kΩ, C_H = 0.1µF, C_{DC} = 4.7µF, $C_{RT/REV}$ = 0.47µF, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) Symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
OFF-HOOK LONGITUDINAL BALANCE											
						MIN	**MIN**	**MIN**	**MIN**	**MIN**	**MIN**
Longitudinal to Metallic (Note 7) Forward and Reverse	IEEE 455 - 1985, R_{LR}, R_{LT} = 368Ω Normal Polarity:					Forward Only		Forward Only			
	0.2kHz < f < 1.0kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	55
	1.0kHz < f < 3.4kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	55
	0.2kHz < f < 1.0kHz, -40°C to 85°C	-	-	-	dB	NA	53	63	63	63	NA
	1.0kHz < f < 3.4kHz, -40°C to 85°C	-	-	-	dB	NA	53	58	58	58	NA
	Reverse Polarity 0.2kHz < f < 3.4kHz, (Figure 4)	-	-	-	dB	NA	53	NA	58	58	55
						MIN	**MIN**	**MIN**	**MIN**	**MIN**	**MIN**
Longitudinal to Metallic (Note 7) Forward and Reverse	R_{LR}, R_{LT} = 300Ω, Normal Polarity:					Forward Only		Forward Only			
	0.2kHz < f < 1.0kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	55
	1.0kHz < f < 3.4kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	55
	0.2kHz < f < 1.0kHz, -40°C to 85°C	-	-	-	dB	NA	53	63	63	63	NA
	1.0kHz < f < 3.4kHz, -40°C to 85°C	-	-	-	dB	NA	53	58	58	58	NA
	Reverse Polarity 0.2kHz < f < 3.4kHz, (Figure 4)	-	-	-	dB	NA	53	NA	58	58	55
						MIN	**MIN**	**MIN**	**MIN**	**MIN**	**MIN**
Longitudinal to 4-Wire (Note 9) (Forward and Reverse)	Normal Polarity:					Forward Only		Forward Only			
	0.2kHz < f < 1.0kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	61
	1.0kHz < f < 3.4kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	61
	0.2kHz < f < 1.0kHz, -40°C to 85°C	-	-	-	dB	NA	53	63	63	63	NA
	1.0kHz < f < 3.4kHz, -40°C to 85°C	-	-	-	dB	NA	53	58	58	58	NA
	Reverse Polarity 0.2kHz < f < 3.4kHz, (Figure 4)	-	-		dB	NA	53	NA	58	58	61
Metallic to Longitudinal (Note 10) Forward and Reverse	FCC Part 68, Para 68.310 (Note 8) 0.2kHz < f < 3.4kHz, (Figure 5)	40	50	-	dB	Forward Only	•	Forward Only	•	•	•
4-Wire to Longitudinal (Note 11) Forward and Reverse	0.2kHz < f < 3.4kHz, (Figure 5)	40	-	-	dB	Forward Only	•	Forward Only	•	•	•

Electrical Specifications

T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = -24V, PTG = Open, R_{P1} = R_{P2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 50kΩ, RDC_RAC = 20kΩ, R_{OH} = 40kΩ, C_H = 0.1μF, C_{DC} = 4.7μF, $C_{RT/REV}$ = 0.47μF, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) Symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

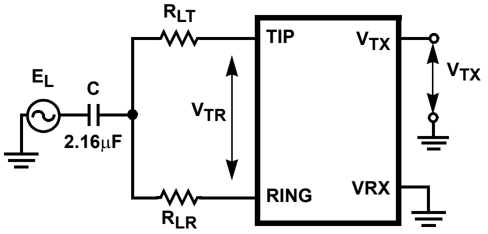


FIGURE 4. LONGITUDINAL TO METALLIC AND LONGITUDINAL TO 4-WIRE BALANCE

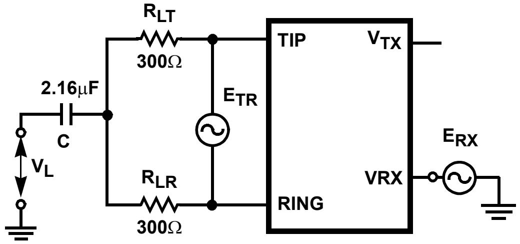


FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
2-Wire Return Loss Forward and Reverse	0.2kHz to 1.0kHz (Note 12, Figure 6)	30	35	-	dB	Forward Only	•	Forward Only	•	•	•
	1.0kHz to 3kHz (Note 12, Figure 6)	23	25	-	dB						
	3kHz to 3.4kHz (Note 12, Figure 6)	21	23	-	dB						
TIP IDLE VOLTAGE (User Programmable)											
TIPX Idle Voltage Forward and Reverse	Active, I_L < 5mA	-2.6	-2.2	-1.8	V	Forward Only	•	Forward Only	•	•	•
RING IDLE VOLTAGE (User Programmable)											
RINGX Idle Voltage Forward and Reverse	Active, I_L < 5mA	-46.4	-45.3	-44.2	V	Forward Only	•	Forward Only	•	•	•
	Tip open, I_L < 5mA	-46.4	-45.3	-44.2	V						
V_{TR} Forward and Reverse	Active, I_L < 5mA	41	43.1	45	V	Forward Only	•	Forward Only	•	•	•
$V_{TR(ROH)}$ Pulse Metering Forward and Reverse	Active, I_L ≥ 8.5mA, R_{OH} = 50kΩ	36	38.1	-	V	NA	•	NA	NA	•	•

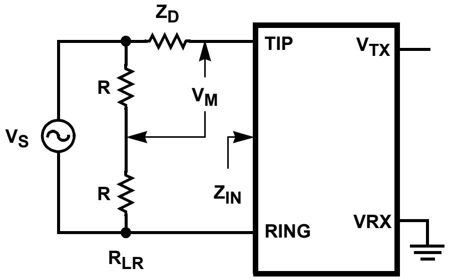


FIGURE 6. TWO-WIRE RETURN LOSS

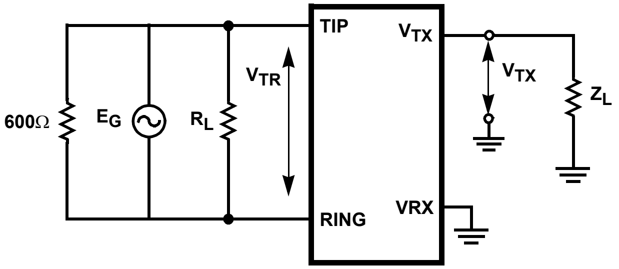


FIGURE 7. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT), OUTPUT OFFSET VOLTAGE AND HARMONIC DISTORTION

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = -24V, PTG = Open, R_{P1} = R_{P2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 50kΩ, RDC_RAC = 20kΩ, R_{OH} = 40kΩ, C_H = 0.1µF, C_{DC} = 4.7µF, $C_{RT/REV}$ = 0.47µF, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) Symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
4-WIRE TRANSMIT PORT (V_{TX})											
Overload Level, Off Hook (I_L≥ 18mA) Forward and Reverse	(Z_L > 20kΩ, IL 1% THD) (Note 13, Figure 7) T_A = 0°C to 85°C	3.2	-	-	V_{PEAK}	Forward Only	•	Forward Only	•	•	•
	T_A = -40°C to 0°C	3.0	-	-	V_{PEAK}						
Overload Level, On Hook (I_L ≤ 5mA) Forward and Reverse	(Z_L > 20kΩ, 1% THD) (Note 14, Figure 7)	1.3	-	-	V_{PEAK}	Forward Only	•	Forward Only	•	•	•
V_{TX} Output Offset Voltage Forward and Reverse	E_G = 0, Z_L = ∞, (Note 15, Figure 7)	-200	-	200	mV	Forward Only	•	Forward Only	•	•	•
Output Impedance (Guaranteed by Design)	0.2kHz < f < 03.4kHz	-	0.1	1	Ω	•	•	•	•	•	•
4-WIRE RECEIVE PORT (VRX)											
VRX Input Impedance (Guaranteed by Design)	0.2kHz < f < 3.4kHz	-	500	600	kΩ	•	•	•	•	•	•
FREQUENCY RESPONSE (OFF-HOOK)											
2-Wire to 4-Wire Forward and Reverse	Relative to 0dBm at 1.0kHz, E_{RX} = 0V 0.3kHz < f < 3.4kHz	-0.15	-	0.15	dB	Forward Only	•	Forward Only	•	•	•
	f = 8.0kHz (Note 16, Figure 8)	-	0.24	0.5	dB						
	f = 12kHz (Note 16, Figure 8)	-	0.58	1.0	dB						
	f = 16kHz (Note 16, Figure 8)	-	1.0	1.5	dB						
4-Wire to 2-Wire Forward and Reverse	Relative to 0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz	-0.15	-	0.15	dB	Forward Only	•	Forward Only	•	•	•
	f = 8kHz (Note 17, Figure 8)	-0.5	0.24	-	dB						
	f = 12kHz (Note 17, Figure 8)	-1.0	0.58	-	dB						
	f = 16kHz (Note 17, Figure 8)	-1.5	1.0	-	dB						
4-Wire to 4-Wire Forward and Reverse	Relative to 0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 18, Figure 8)	-0.15	-	0.15	dB	Forward Only	•	Forward Only	•	•	•
	8kHz, 12kHz, 16kHz (Note 18, Figure 8)	-0.5	0	0.5	dB						

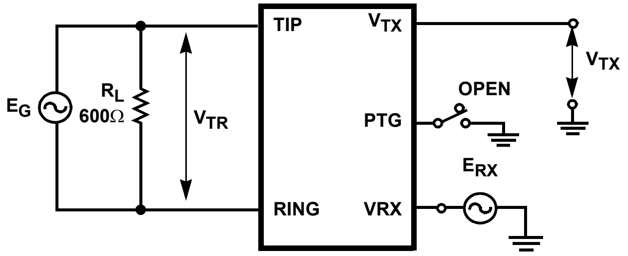


FIGURE 8. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

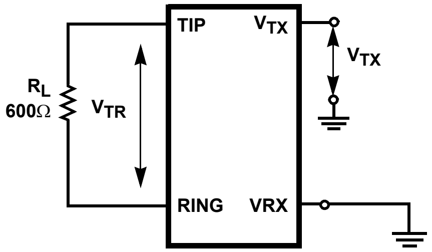


FIGURE 9. IDLE CHANNEL NOISE

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = -24V, PTG = Open, R_{P1} = R_{P2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 50kΩ, RDC_RAC = 20kΩ, R_{OH} = 40kΩ, C_H = 0.1µF, C_{DC} = 4.7µF, $C_{RT/REV}$ = 0.47µF, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) Symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
INSERTION LOSS											
2-Wire to 4-Wire Forward and Reverse	0dBm, 1kHz PTG = Open (Note 19, Figure 8)	-0.2	-	0.2	dB	Forward Only	•	Forward Only	•	•	•
	PTG = GND (Note 20, Figure 8)	-6.22	-6.02	-5.82	dB						
4-Wire to 2-Wire Forward and Reverse	0dBm, 1kHz (Note 21, Figure 8)	-0.2	-	0.2	dB	Forward Only	•	Forward Only	•	•	•
GAIN TRACKING (Ref = -10dBm, at 1.0kHz)											
2-Wire to 4-Wire Forward and Reverse	-40dBm to +3dBm (Note 22, Figure 8)	-0.1	-	0.1	dB	Forward Only	•	Forward Only	•	•	•
	-55dBm to -40dBm (Note 22, Figure 8)	-0.2	-	0.2	dB						
4-Wire to 2-Wire Forward and Reverse	-40dBm to +3dBm (Note 23, Figure 8)	-0.1	-	0.1	dB	Forward Only	•	Forward Only	•	•	•
	-55dBm to -40dBm (Note 23, Figure 8)	-0.2	-	0.2	dB						
NOISE											
Idle Channel Noise at 2-Wire	C-Message Weighting	-	10.5	13	dBrnC	Forward Only	•	Forward Only	•	•	•
Forward and Reverse	Psophometric Weighting (Note 24, Note 30, Figure 9)	-	-79.5	-77	dBmp						
Idle Channel Noise at 4-Wire	C-Message Weighting	-	10.5	13	dBrnC	Forward Only	•	Forward Only	•	•	•
Forward and Reverse	Psophometrical Weighting (Note 25, Note 30, Figure 9)	-	-79.5	-77	dBmp						
HARMONIC DISTORTION											
2-Wire to 4-Wire Forward and Reverse	0dBm, 0.3kHz to 3.4kHz (Note 26, Figure 7)	-	-67	-50	dB	Forward Only	•	Forward Only	•	•	•
4-Wire to 2-Wire Forward and Reverse	0dBm, 0.3kHz to 3.4kHz (Note 27, Figure 8)	-	-67	-50	dB	Forward Only	•	Forward Only	•	•	•

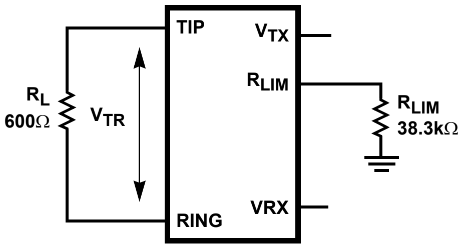


FIGURE 10. CONSTANT LOOP CURRENT TOLERANCE

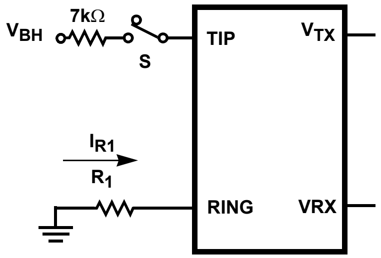


FIGURE 11. TIPX VOLTAGE

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = -24V, PTG = Open, R_{P1} = R_{P2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 50kΩ, RDC_RAC = 20kΩ, R_{OH} = 40kΩ, C_H = 0.1µF, C_{DC} = 4.7µF, $C_{RT/REV}$ = 0.47µF, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) Symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
BATTERY FEED CHARACTERISTICS											
Constant Loop Current Tolerance I_L = 26.5mA, R_{LIM} = 38.3kΩ Forward and Reverse	18mA ≤ IL ≤ 45mA, (Note 27, Figure 10)	$0.92I_L$	I_L	$1.08I_L$	mA	Forward Only	•	Forward Only	•	•	•
Tip Open State TIPX Leakage Current	S = Closed (Figure 11)	-	-	-200	µA	•	•	•	•	•	•
Tip Open State RINGX Current	R_1 = 0Ω, V_{BH} = -48V, R_{LIM} = 38.3kΩ R_1 = 2.5kΩ, V_{BH} = -48V (Figure 11)	22.6 15.5	26.8 17.1	31 18.2	mA mA	•	•	•	•	•	•
Tip Open State RINGX Voltage	5mA < I_{R1} < 26mA (Figure 11)	-	42.8	-	V	•	•	•	•	•	•
Tip Voltage (Ground Start)	Active State, (S Open) R_1 = 150Ω (Figure 11)	-5.3	-4.8	-4.3	V	NA	NA	NA	•	•	NA
Tip Voltage (Ground Start)	Active State, (S Closed) Tip Lead to -48V Through 7kΩ, Ring Lead to Ground Through 150Ω (Figure 11)	-5.3	-4.8	-4.3	V	NA	NA	NA	•	•	NA
Open Circuit State Loop Current	(Active) R_L = 0Ω	-20	0	20	µA	•	•	•	•	•	•
LOOP CURRENT DETECTOR											
Programmable Threshold Forward and Reverse	I_{LTh} = (500/ R_D) ≥ 5mA, I_{LTh} = 8.5mA R_D = 58.8kΩ	$0.9I_{LTh}$	I_{LTh}	$1.1I_{LTh}$	mA	Forward Only	•	Forward Only	•	•	•
GROUND KEY DETECTOR											
Ground Key Detector Threshold Tip/Ring Current Difference	Tip Open Active (Note 29, R1 = 2.5kΩ, Figure 12)	5 12.5	8 20	11 27.5	mA mA	•	•	NA	•	•	NA
LINE VOLTAGE MEASUREMENT											
Pulse Width ($\overline{GKD}$_$\overline{LVM}$)	Pulse Width = (20)($C_{REV...}$/I_{LIM})	0.32	0.36	0.4	ms/V	NA	NA	NA	•	•	•
RING TRIP DETECTOR (DT, DR)											
Ring Trip Comparator Current	Source Res = 2MΩ	-	2	-	µA	•	•	•	•	•	•
Input Common-Mode Range	Source Res = 2MΩ	-	-	±200	V	•	•	•	•	•	•

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = -24V, PTG = Open, $R_{P1} = R_{P2}$ = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 50kΩ, RDC_RAC = 20kΩ, R_{OH} = 40kΩ, C_H = 0.1µF, C_{DC} = 4.7µF, $C_{RT/REV}$ = 0.47µF, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) Symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
RING RELAY DRIVER											
V_{SAT} at 30mA	I_{OL} = 30mA	-	0.2	0.5	V	•	•	•	•	•	•
V_{SAT} at 40mA	I_{OL} = 40mA	-	0.52	0.8	V	•	•	•	•	•	•
Off State Leakage Current	V_{OH} = 13.2V	-	0.1	10	µA	•	•	•	•	•	•
TEST RELAY DRIVER (TRLY1, TRLY2)											
V_{SAT} at 30mA	I_{OL} = 30mA	-	0.3	0.5	V	NA	NA	NA/•	NA/•	NA/•	NA/•
V_{SAT} at 40mA	I_{OL} = 40mA	-	0.65	1.3	V	NA	NA	NA/•	NA/•	NA/•	NA/•
Off State Leakage Current	V_{OH} = 13.2V	-	-	10	µA	NA	NA	NA/•	NA/•	NA/•	NA/•

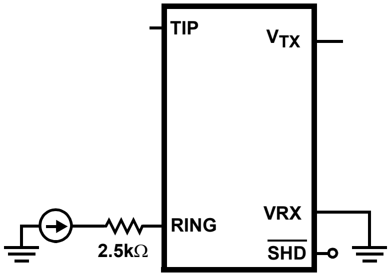


FIGURE 12. GROUND KEY DETECT

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
DIGITAL INPUTS (C1, C2, C3, C4, C5)											
Input Low Voltage, V_{IL}		0	-	0.8	V	•	•	•	•	•	•
Input High Voltage, V_{IH}		2.0	-	V_{CC}	V	•	•	•	•	•	•
Input Low Current, I_{IL}	V_{IL} = 0.4V	-	-	-10	µA	•	•	•	•	•	•
Input High Current, I_{IH}	V_{IH} = 2.5V	-	25	50	µA	•	•	•	•	•	•
DETECTOR OUTPUTS ($\overline{SHD}$, $\overline{GKD\_LVM}$)											
$\overline{SHD}$ Output Low Voltage, V_{OL} Forward, Reverse	I_{OL} = 1mA	-	-	0.5	V	Forward Only	•	Forward Only	•	•	•
$\overline{SHD}$ Output High Voltage, V_{OH} Forward, Reverse	I_{OH} = 100µA	2.7	-	-	V	Forward Only	•	Forward Only	•	•	•
$\overline{GKD\_LVM}$ Output Low Voltage, V_{OL} Forward and Tip Open	I_{OL} = 1mA R_1 = 2.5kΩ (Figure 11)	-	-	0.5	V	$\overline{GKD}$	$\overline{GKD}$	NA	$\overline{GKD\_LVM}$	$\overline{GKD\_LVM}$	$\overline{LVM}$
$\overline{GKD\_LVM}$ Output High Voltage, V_{OH} Forward and Tip Open	I_{OH} = 100µA	2.7	-	-	V	$\overline{GKD}$	$\overline{GKD}$	NA	$\overline{GKD\_LVM}$	$\overline{GKD\_LVM}$	$\overline{LVM}$
Internal Pull-Up Resistor		-	15	-	kΩ	•	•	•	•	•	•

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = -24V, PTG = Open, R_{P1} = R_{P2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 50kΩ, RDC_RAC = 20kΩ, R_{OH} = 40kΩ, C_H = 0.1µF, C_{DC} = 4.7µF, $C_{RT/REV}$ = 0.47µF, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) Symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
POWER DISSIPATION (V_{BH} = -48V, V_{BL} = -24V)											
Open Circuit State	C1, C2, C3 = 0, 0, 0	-	25	-	mW	Forward Only	•	Forward Only	•	•	•
On-Hook, Active	C1, C2, C3 = 0, 1, 0 C1, C2, C3 = 1, 1, 0						•		•	•	•
Forward and Reverse	I_L = 0mA, Longitudinal Current = 0mA	-	52	-	mW	Forward Only	•	Forward Only	•	•	•
POWER SUPPLY CURRENTS (V_{BH} = -48V, V_{BL} = -24V)											
V_{CC} Current, I_{CC}	Open Circuit State	-	2.25	3.0	mA	Forward Only	•	Forward Only	•	•	•
V_{BH} Current, I_{BH}		-	0.3	0.45	mA	Forward Only	•	Forward Only	•	•	•
V_{BL} Current, I_{BL}		-	0.022	0.035	mA	Forward Only	•	Forward Only	•	•	•
V_{CC} Current, I_{CC} Forward and Reverse	Active State I_L = 0mA, Longitudinal Current = 0mA	-	2.7	3.6	mA	Forward Only	•	Forward Only	•	•	•
V_{BH} Current, I_{BH} Forward and Reverse		-	0.8	1.06	mA	Forward Only	•	Forward Only	•	•	•
V_{BL} Current, I_{BL} Forward and Reverse		-	-	0.01	mA	Forward Only	•	Forward Only	•	•	•
POWER SUPPLY REJECTION RATIOS											
V_{CC} to 2 or 4 Wire Port Forward and Reverse	Active State R_L = 600Ω 50Hz < f < 3400Hz, V_{IN} =100mV	-	40	-	dB	Forward Only	•	Forward Only	•	•	•
V_{BH} to 2 or 4 Wire Port Forward and Reverse		-	40	-	dB	Forward Only	•	Forward Only	•	•	•
V_{BL} to 2 or 4 Wire Port Forward and Reverse		-	40	-	dB	Forward Only	•	Forward Only	•	•	•
TEMPERATURE GUARD											
Junction Threshold Temperature		-	175	-	°C	•	•	•	•	•	•

Notes

2. **Overload Level (Two-Wire Port, Off Hook)** - The overload level is specified at the 2-wire port (V_{TR}) with the signal source at the 4-wire receive port (E_{RX}). $R_L = 600\Omega$, $I_{DCMET} \geq 18mA$. Increase the amplitude of E_{RX} until 1% THD is measured at V_{TR}. Reference Figure 1.
3. **Overload Level (Two-Wire Port, On Hook)** - The overload level is specified at the 2-wire port (V_{TR}) with the signal source at the 4-wire receive port (E_{RX}). $R_L = \infty$, $I_{DCMET} = 0mA$. Increase the amplitude of E_{RX} until 1% THD is measured at V_{TR}. Reference Figure 1.
4. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground. L_{ZT}, L_{ZR}, V_T, V_R, A_R and A_T are defined in Figure 2.
   (TIP) $L_{ZT} = V_T/A_T$
   (RING) $L_{ZR} = V_R/A_R$
   where: $E_L = 1V_{RMS}$ (0Hz to 100Hz)
5. **Longitudinal Current Limit (On-Hook Active)** - On-Hook longitudinal current limit is determined by increasing the (60Hz) amplitude of E_L (Figure 3A) until the 2-wire longitudinal current is greater than $28mA_{RMS}$/Wire. Under this condition, $\overline{SHD}$ pin remains low (no false detection) and the 2-wire to 4-wire longitudinal balance is verified to be greater than 45dB ($LB_{2-4} = 20\log VTX/E_L$).
6. **Longitudinal Current Limit (Off-Hook Active)** - Off-Hook longitudinal current limit is determined by increasing the (60Hz) amplitude of E_L (Figure 3B) until the 2-wire longitudinal current is greater than $28mA_{RMS}$/Wire. Under this condition, $\overline{SHD}$ pin remains high (no false detection) and the 2-wire to 4-wire longitudinal balance is verified to be greater than 45dB ($LB_{2-4} = 20\log VTX/E_L$).
7. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation:

   $BLME = 20 \log (E_L/V_{TR})$, where: E_L and V_{TR} are defined in Figure 4.
8. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in this spec.
9. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation:

   $BLFE = 20 \log (E_L/V_{TX})$, E_L and V_{TX} are defined in Figure 4.
10. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation:

    $BMLE = 20 \log (E_{TR}/V_L)$, $E_{RX} = 0$

    where: E_{TR}, V_L and E_{RX} are defined in Figure 5.
11. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation:

    $BFLE = 20 \log (E_{RX}/V_L)$, E_{TR} = source is removed.

    where: E_{RX}, V_L and E_{TR} are defined in Figure 5.
12. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation:
    $r = -20 \log (2V_M/V_S)$ where: Z_D = The desired impedance; e.g., the characteristic impedance of the line, nominally 600Ω. (Reference Figure 6).
13. **Overload Level (4-Wire Port Off-Hook)** - The overload level is specified at the 4-wire transmit port (V_{TX}) with the signal source (E_G) at the 2-wire port, $Z_L = 20k\Omega$, $R_L = 600\Omega$ (Reference Figure 7). Increase the amplitude of E_G until 1% THD is measured at V_{TX}. Note the PTG pin is open, and the gain from the 2-wire port to the 4-wire port is equal to 1.
14. **Overload Level (4-Wire Port On-Hook)** - The overload level is specified at the 4-wire transmit port (V_{TX}) with the signal source (E_G) at the 2-wire port, $Z_L = 20k\Omega$, $R_L = \infty$ (Reference Figure 7). Increase the amplitude of E_G until 1% THD is measured at V_{TX}. Note the PTG pin is open, and the gain from the 2-wire port to the 4-wire port is equal to 1.
15. **Output Offset Voltage** - The output offset voltage is specified with the following conditions: $E_G = 0$, $R_L = 600\Omega$, $Z_L = \infty$ and is measured at V_{TX}. E_G, R_L, V_{TX} and Z_L are defined in Figure 7.
16. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to E_G = 0dBm at 1.0kHz, E_{RX} = 0V (VRX input floating), $R_L = 600\Omega$. The frequency response is computed using the following equation:

    $F_{2-4} = 20 \log (V_{TX}/V_{TR})$, vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX}, V_{TR}, R_L and E_G are defined in Figure 8.
17. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G source removed from circuit, $R_L = 600\Omega$. The frequency response is computed using the following equation:

    $F_{4-2} = 20 \log (V_{TR}/E_{RX})$, vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TR}, R_L and E_{RX} are defined in Figure 8.
18. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G source removed from circuit, $R_L = 600\Omega$. The frequency response is computed using the following equation:

    $F_{4-4} = 20 \log (V_{TX}/E_{RX})$, vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX}, R_L and E_{RX} are defined in Figure 8.
19. **Two-Wire to Four-Wire Insertion Loss (PTG = Open)** - The 2-wire to 4-wire insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, $E_{RX} = 0$ (VRX input floating), $R_L = 600\Omega$ and is computed using the following equation:

    $L_{2-4} = 20 \log (V_{TX}/V_{TR})$

    where: V_{TX}, V_{TR}, R_L and E_G are defined in Figure 8. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for $R_{F1} = R_{F2} = 0$).
20. **Two-Wire to Four-Wire Insertion Loss (PTG = AGND)** - The 2-wire to 4-wire insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, $E_{RX} = 0$ (VRX input floating), $R_L = 600\Omega$ and is computed using the following equation:

    $L_{2-4} = 20 \log (V_{TX}/V_{TR})$

    where: V_{TX}, V_{TR}, R_L and E_G are defined in Figure 8. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for $R_{F1} = R_{F2} = 0$).
21. **Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire insertion loss is measured based upon E_{RX} = 0dBm, 1.0kHz input signal, E_G source removed from circuit, $R_L = 600\Omega$ and is computed using the following equation:

    $L_{4-2} = 20 \log (V_{TR}/E_{RX})$

    where: V_{TR}, R_L and E_{RX} are defined in Figure 8.
22. **Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for E_G = -10dBm, 1.0kHz signal, $E_{RX} = 0$ (VRX output floating), $R_L = 600\Omega$ and is computed using the following equation.

    $G_{2-4} = 20 \bullet \log (V_{TX}/V_{TR})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TX}, R_L and V_{TR} are defined in Figure 8.

23. **Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for E_{RX} = -10dBm, 1.0kHz signal, E_G source removed from circuit, R_L = 600Ω and is computed using the following equation:

    $G_{4-2} = 20 \bullet \log (V_{TR}/E_{RX})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TR}, R_L and E_{RX} are defined in Figure 8. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.

24. **Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at V_{TR} is specified with the 2-wire port terminated in 600Ω (R_L) and with the 4-wire receive port (VTX) floating (Reference Figure 9).

25. **Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at V_{TX} is specified with the 2-wire port terminated in 600Ω (R_L). The noise specification is with respect to a 600Ω impedance level at V_{TX}. The 4-wire receive port (VTX) floating (Reference Figure 9).

26. **Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured within the voice band with the following conditions. E_G = 0dBm at 1kHz, R_L = 600Ω. Measurement taken at V_{TX}. (Reference Figure 7).

27. **Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured within the voice band with the following conditions. E_{RX} = 0dBm0. Vary frequency between 300Hz and 3.4kHz, R_L = 600Ω. Measurement taken at V_{TR}. (Reference Figure 8).

28. **Constant Loop Current** - The constant loop current is calculated using the following equation:

    $I_L = 1000/R_{LIM} = V_{TR}/600$ (Reference Figure 10).

29. **Ground Key Detector** - (TRIGGER) Ground the Ring pin through a 2.5kΩ resistor and verify that $\overline{GKD}$ goes low.

    (RESET) Disconnect the Ring pin and verify that $\overline{GKD}$ goes high.

    (Hysteresis) Compare difference between trigger and reset.

30. **Electrical Test** - Not tested in production at -40°C.

Circuit Operation and Design Information

The UniSLIC14 family of SLICs are voltage feed current sense **S**ubscriber **L**ine **I**nterface **C**ircuits (SLIC). For short loop applications, the voltage between the tip and ring terminals varies to maintain a constant loop current. For long loop applications, the voltage between the tip and ring terminals are relatively constant and the loop current varies in proportion to the load.

The tip and ring voltages for various loop resistances are shown in Figure 13. The tip voltage remains relatively constant as the ring voltage moves to limit the loop current for short loops.

The loop current for various loop resistances are shown in Figure 14. For short loops, the loop current is limited to the programmed current limit, set by RILIM. For long loop applications, the loop current varies in accordance with Ohms law for the given tip to ring voltage and the loop resistance.

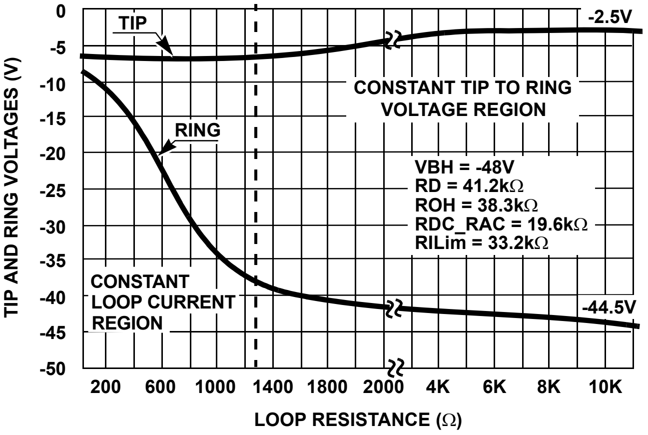


FIGURE 13. TIP AND RING VOLTAGES vs LOOP RESISTANCE

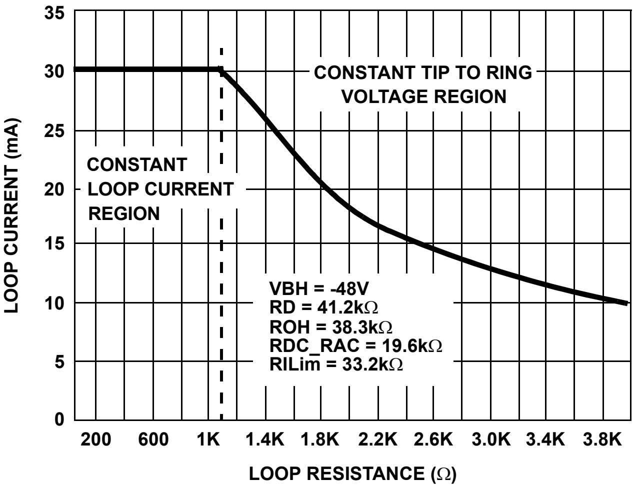
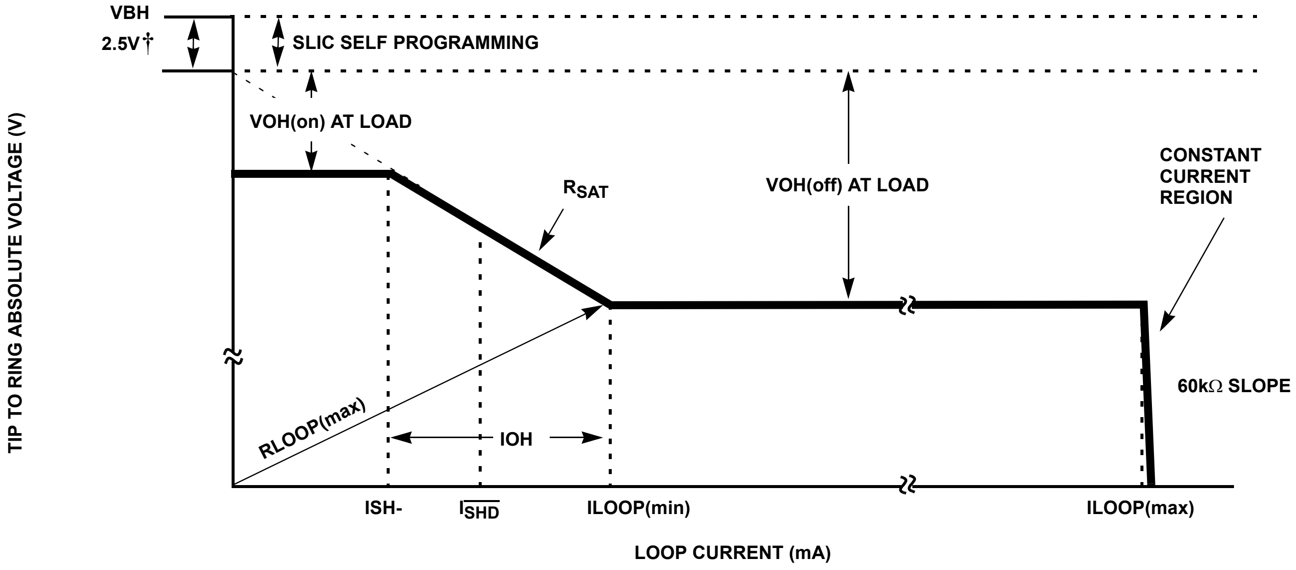


FIGURE 14. LOOP CURRENT vs LOOP RESISTANCE

The following discussion separates the SLIC's operation into its DC and AC paths, then follows up with additional circuit and design information.

DC Feed Curve

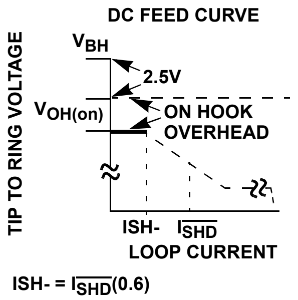
The DC feed curve for the UniSLIC14 family is user programmable. The user defines the on hook and off hook overhead voltages (including the overhead voltage for off hook pulse metering if applicable), the maximum and minimum loop current limits, the switch hook detect threshold and the battery voltage. From these requirements, the DC feed curve is customized for optimum operation in any given application. An Excel spread sheet to calculate the external components can be downloaded off our web site www.intersil.com/telecom/unislic14.xls.



† Internal overhead voltage automatically generated by the SLIC.

FIGURE 15. UniSLIC14 DC FEED CURVE

On Hook Overhead Voltage



The on hook overhead voltage at the load (V_{OH}(on) at Load) is independent of the V_{BH} battery voltage. Once set, the on hook voltage remains constant as the V_{BH} battery voltage changes. The on hook voltage also remains constant over temperature and line leakages up to 0.6 times the Switch Hook Detect threshold ($I_{\overline{SHD}}$). The maximum loop current for a constant on hook overhead voltage is defined as ISH-.

The on hook overhead voltage, required for a given signal level at the load, must take into account the AC voltage drop across the 2 external protection resistors (R_P) and the 2 internal sense resistors (R_S) as shown in Figure 16. The AC on hook overload voltage is calculated using Equation 1.

$$V_{OH(on)\ at\ Load} = V_{sp(on)} \times \left(1 + \frac{2R_P + 2R_S}{Z_L}\right) + 1.5V \qquad \text{(EQ.}$$

where

$V_{OH(on)\ at\ Load}$ = On hook overhead voltage at load

$V_{sp(on)}$ = Required on hook transmission for speech

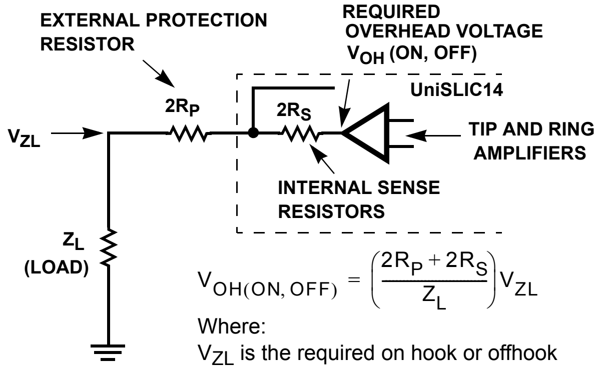
R_P = Protection Resistors (Typically 30Ω)

R_S = Internal Sense Resistors (40Ω)

Z_L = AC load impedance for (600Ω)

1.5V = Additional on hook overhead voltage requirement

To account for any process and temperature variations in the performance of the SLIC, 1.5V is added to the overhead voltage requirement for the on hook case in Equation 1 and 2.0V for the off hook case in Equation 3. Note the 2.5V overhead is automatically generated in the SLIC and is not part of the external overhead programming.

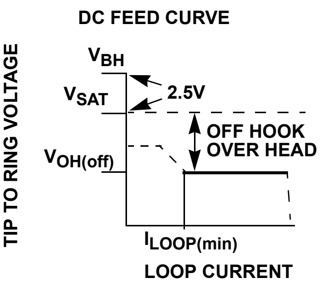


$$V_{OH(ON,\,OFF)} = \left(\frac{2R_P + 2R_S}{Z_L}\right) V_{ZL}$$

Where:
V_{ZL} is the required on hook or offhook transmission delivered to the load.

FIGURE 16. OVERHEAD VOLTAGE OF THE TIP AND RING AMPLIFIERS

Off Hook Overhead Voltage



The off hook overhead voltage V_{OH}(off) at Load is also independent of the V_{BH} battery voltage and remains constant over temperature. The required off hook overhead voltage is the sum of the AC and DC voltage drops across the internal sense resistors (R_S), the protection resistors (R_P), the required (peak) off hook voltage for speech ($V_{sp(off)}$) and the required (peak) off hook voltage for the pulse metering ($V_{pm(off)}$), if applicable.

The off hook overhead voltage is defined in Equation 2 and calculated using Equation 3.

$$V_{OH(off)\ at\ Load} = V_{OH(Rsense)} + V_{sp(off)} + V_{pm(off)} \quad \text{(EQ. 2)}$$

where:

$V_{OH(off)\ at\ Load}$ = Off hook overhead voltage at load

$V_{OH}(R_{sense})$ = Required overhead for the DC voltage drop across sense resistors ($2R_S$ x $Iloop_{(max)}$)

$V_{sp(off)}$ = Required (peak) off hook AC voltage for speech

$V_{pm(off)}$ = Required (peak) off hook AC voltage for pulse metering

$$V_{OH(off)\ at\ Load} = 80 \times I_{LOOP(max)} + V_{sp(off)} \times \left(1 + \frac{2R_P + 2R_S}{Z_L}\right)$$
$$+ V_{pm(off)} \times \left(1 + \frac{2R_P + 2R_S}{Z_{pm}}\right) + 2.0V \quad \text{(EQ. 3)}$$

where:

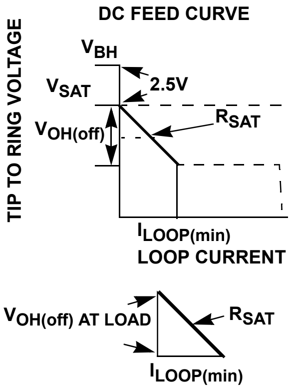
$80 = 2R_s + 2R_{INT}$ (reference Figure 17)

Z_{pm} = Pulse metering load impedance (typically 200Ω).

2.0V = Additional off hook overhead voltage requirement

R_{SAT} Resistance Calculation

The R_{SAT} resistance of the DC feed curve is used to determine the value of the RDC_RAC resistor (Equation 6). The value of this resistor has an effect on both the on hook and off hook overheads. In most applications the off hook condition will dominate the overhead requirements. Therefore, we'll start by calculating the R_{SAT} value for the off hook conditions and then verify that the on hook conditions are also satisfied.

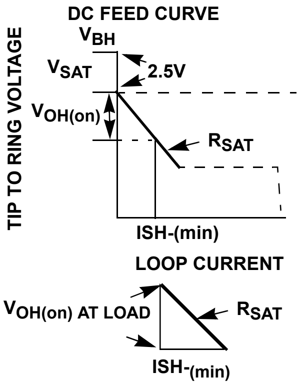


When considering the Off hook condition, R_{SAT} is equal to $V_{OH(off)\ at\ Load}$ divided by $Iloop_{(min)}$ (Equation 4).

For the given system requirements (recommended application circuit in back of data sheet): Iloop (min) = 20mA, Iloop (max) = 30mA, $V_{sp(off)} = 3.2V_{PEAK}$, $V_{spm(off)} = 0V_{PEAK}$, $V_{OH(off)\ at\ Load} = 8.34V$ the value of $R_{SAT(off)}$ is equal to 417Ω as calculated in Equation 4.

$$R_{SAT(off)} = \frac{V_{OH(off)\ at\ Load}}{I_{LOOP(min)}} = \frac{8.34V}{20mA} = 417\Omega \quad \text{(EQ. 4)}$$

Before using this R_{SAT} value, to calculate the RDC_RAC resistor, we need to verify that the on hook requirements will also be met.



The on hook overhead voltage calculated with the off hook R_{SAT} ($R_{SAT(off)}$), is given in Equation 5 and equals 3.0V. The on hook overhead calculated with Equation 1 equals 2.85V for the given system requirements (recommended application circuit in back of data sheet): Switch Hook Detect threshold = 12mA, ISH- = (0.6)12mA = 7.2mA, $V_{sp(on)} = 0.775V_{RMS}$

$$R_{SAT(on)} = \frac{2.85V}{7.2mA} = 395\Omega$$

Thus, the on hook overhead requirements of 2.85V will be met if we use the $R_{SAT(off)}$ value.

$$V_{OH(on)} = (ISH\text{-})(R_{SAT(off)}) \quad \text{(EQ. 5)}$$

$$V_{OH(on)} = 7.2mA \times 417\Omega$$

$$V_{OH(on)} = 3.0V$$

If the on hook overhead requirement is not met, then we need to use the $R_{SAT(on)}$ value to determine the RDC_RAC resistor value. The external saturation guard resistor RDC_RAC is equal to 50 times R_{SAT}.

In the example above R_{SAT} would equal 417Ω and RDC_RAC would then equal to 20.85kΩ (closest standard value is 21kΩ).

$$RDC\_RAC = 50 \times R_{SAT} \quad \text{(EQ. 6)}$$

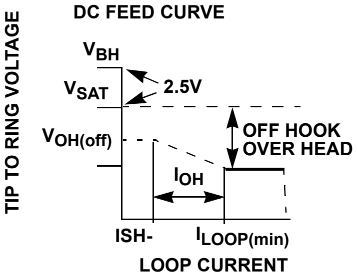
The Switch Hook Detect threshold current is set by resistor R_D and is calculated using Equation 7. For the above example R_D is calculated to be 41.6kΩ (500/12mA). The next closest standard value is 41.2kΩ.

$$R_D = \frac{500}{I_{SHD}} \qquad \text{(EQ. 7)}$$

The true value of ISH-, for the selected value of R_D is given by Equation 8:

$$ISH- = \frac{500}{R_D}(0.6) \qquad \text{(EQ. 8)}$$

For the example above, ISH- equals 7.28mA (500 x 0.6/ 41.2K). Verify that the value of ISH- is above the suspected line leakage of the application. The UniSLIC family will provide a constant on hook voltage level for leakage currents up to this value of line leakage.



The R_{OH} resistor, which is used to set the offhook overhead voltage, is calculated using Equations 9 and 10.

I_{OH} is defined as the difference between the $I_{LOOP(min)}$ and ISH-. Substituting Equation 8 for ISH- into Equation 9 and solving for R_{OH} defines R_{OH} in terms of $I_{LOOP(min)}$ and R_D.

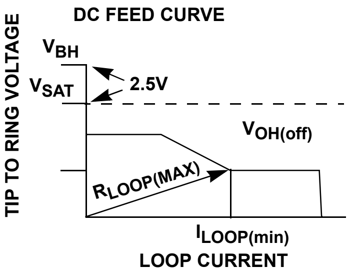
$$R_{OH} = \frac{500}{I_{OH}} = \frac{500}{I_{LOOP(min)} - ISH-} \qquad \text{(EQ. 9)}$$

Equation 10 can be used to determine the actual ISH- value resulting from the R_D resistor selected. The value of R_D should be the next standard value that is lower than that calculated. This will insure meeting the $I_{LOOP(min)}$ requirement. ROH for the above example equals 39.1kΩ.

$$R_{OH} = \frac{R_D 500}{R_D I_{LOOP(min)} - 500(.6)} \qquad \text{(EQ. 10)}$$

The current limit is set by a single resistor and is calculated using Equation 11.

$$R_{LIM} = \frac{1000}{I_{LOOP(max)}} \qquad \text{(EQ. 11)}$$



The maximum loop resistance is calculated using Equation 12. The resistance of the protection resistors ($2R_P$) is subtracted out to obtain the maximum loop length to meet the required off hook overhead voltage. If $R_{LOOP(MAX)}$ meets the loop length requirements you are done. If the loop length needs to be longer, then consider adjusting one of the following: 1) the $\overline{SHD}$ threshold, 2) minimum loop current requirement or 3) the on and off hook signal levels.

$$R_{LOOP(max)} = \frac{V_{BH} - [V_{SAT} + 2V + V_{OH(off)}]}{I_{LOOP(min)}} - 2R_P \qquad \text{(EQ. 12)}$$

SLIC in the Active Mode

Figure 17 shows a simplified AC transmission model. Circuit analysis yields the following design equations:

$$V_A = I_M \times 2R_S \times \frac{1}{80k} \times 200(Z_{TR} - 2R_P) \times 5 \qquad \text{(EQ. 13)}$$

$$V_A = \frac{I_M}{2}(Z_{TR} - 2R_P) \qquad \text{(EQ. 14)}$$

Node Equation

$$\frac{V_{RX}}{500k} - \frac{V_A}{500k} = I_X \qquad \text{(EQ. 15)}$$

Substitute Equation 14 into Equation 15

$$I_X = \frac{V_{RX}}{500k} - \frac{I_M(Z_{TR} - 2R_P)}{1000k} \qquad \text{(EQ. 16)}$$

Loop Equation

$$I_X 500k - V_{TX}' + I_X 500k = 0 \qquad \text{(EQ. 17)}$$

Substitute Equation 16 into Equation 17

$$V_{TX}' = 2V_{RX} - I_M(Z_{TR} - 2R_P) \qquad \text{(EQ. 18)}$$

Loop Equation

$$V_{TR} - I_M 2R_P + V_{TX}' = 0 \qquad \text{(EQ. 19)}$$

Substitute Equation 18 into Equation 19

$$V_{TR} = I_M Z_{TR} - 2V_{RX} \qquad \text{(EQ. 20)}$$

Substituting $-V_{TR}/Z_L$ into Equation 20 for I_M and rearranging to solve for V_{TR} results in Equation 21

$$V_{TR}\left(1 + \frac{Z_{TR}}{Z_L}\right) = -2V_{RX} \qquad \text{(EQ. 21)}$$

where:

V_{RX} = The input voltage at the VRX pin.

V_A = An internal node voltage that is a function of the loop current detector and the impedance matching networks.

I_X = Internal current in the SLIC that is the difference between the input receive current and the feedback current.

I_M = The AC metallic current.

R_P = A protection resistor (typical 30Ω).

Z_T = An external resistor/network for matching the line impedance.

V_{TX}' = The tip to ring voltage at the output pins of the SLIC.

V_{TR} = The tip to ring voltage including the voltage across the protection resistors.

Z_L = The line impedance.

Z_{TR} = The input impedance of the SLIC including the protection resistors.

(AC) 4-Wire to 2-Wire Gain

The 4-wire to 2-wire gain is equal to V_{TR}/V_{RX}.

From Equation 21 and the relationship $Z_T = 200(Z_{TR}-2R_P)$.

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = -2\frac{Z_L}{Z_L + Z_{TR}} = -2\frac{Z_L}{Z_L + \left(\frac{Z_T}{200} + 2R_P\right)} \qquad \text{(EQ. 22)}$$

Notice that the phase of the 4-wire to 2-wire signal is 180°out of phase with the input signal.

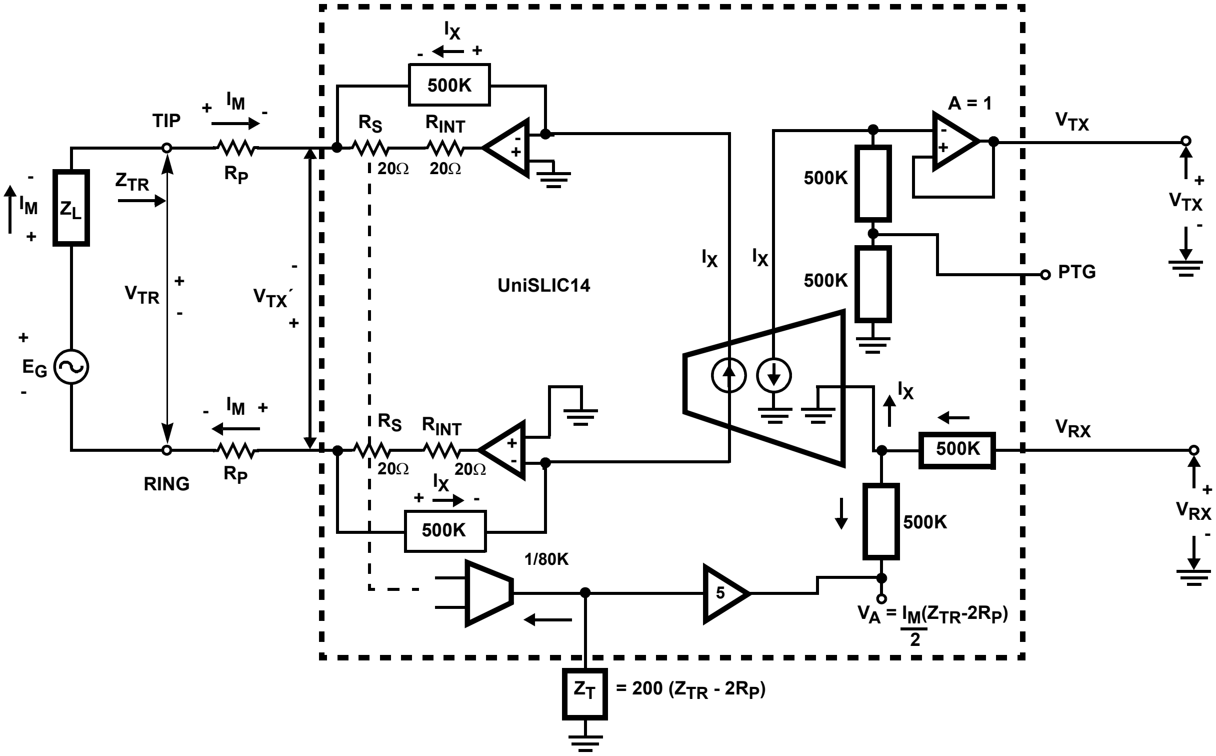


FIGURE 17. SIMPLIFIED AC TRANSMISSION CIRCUIT

(AC) 2-Wire to 4-Wire Gain

The 2-wire to 4-wire gain is equal to V_{TX}/E_G with V_{RX} = 0

Loop Equation

$$-E_G + Z_L I_M + 2R_P I_M - V_{TX}' = 0 \qquad \text{(EQ. 23)}$$

From Equation 18 with V_{RX} = 0

$$V_{TX}' = -I_M(Z_{TR} - 2R_P) \qquad \text{(EQ. 24)}$$

Substituting Equation 24 into Equation 23 and simplifying.

$$E_G = I_M(Z_L + Z_{TR}) \qquad \text{(EQ. 25)}$$

By design, VTX = -VTX´, therefore

$$G_{2-4} = \frac{V_{TX}}{E_G} = \frac{I_M(Z_{TR} - 2R_P)}{I_M(Z_L + Z_{TR})} = \frac{(Z_{TR} - 2R_P)}{(Z_L + Z_{TR})} \qquad \text{(EQ. 26)}$$

A more useful form of the equation is rewritten in terms of V_{TX}/V_{TR}. A voltage divider equation is written to convert from E_G to V_{TR} as shown in Equation 27.

$$V_{TR} = \left(\frac{Z_{TR}}{Z_{TR} + Z_L}\right)E_G \qquad \text{(EQ. 27)}$$

Rearranging Equation 27 in terms of E_G, and substituting into Equation 26 results in an equation for 2-wire to 4-wire gain, that's a function of the synthesized input impedance of the SLIC (Z_{TR}) and the protection resistors (R_P).

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_{TR} - 2R_P}{Z_{TR}} \qquad \text{(EQ. 28)}$$

Notice that the phase of the 2-wire to 4-wire signal is in phase with the input signal.

(AC) 4-Wire to 4-Wire Gain

The 4-wire to 4-wire gain is equal to V_{TX}/V_{RX}, E_G = 0.

From Equation 18.

$$V_{TX}' = -V_{TX} = -2V_{RX} + I_M(Z_{TR} - 2R_P) \qquad \text{(EQ. 29)}$$

Substituting $-V_{TR}/Z_L$ into Equation 29 for I_M results in Equation 30.

$$V_{TX} = -2V_{RX} - \frac{V_{TR}(Z_{TR} - 2R_P)}{Z_L} \qquad \text{(EQ. 30)}$$

Substituting Equation 21 for V_{TR} in Equation 30 and simplifying results in Equation 31.

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = -2\left(\frac{Z_L + 2R_P}{Z_L + Z_{TR}}\right) \quad \text{(EQ. 31)}$$

(AC) 2-Wire Impedance

The AC 2-wire impedance (Z_{TR}) is the impedance looking into the SLIC, including the fuse resistors. The formula to calculate the proper Z_T for matching the 2-wire impedance is shown in Equation 32.

$$Z_T = 200 \bullet (Z_{TR} - 2R_P) \quad \text{(EQ. 32)}$$

Equation 32 can now be used to match the SLIC's impedance to any known line impedance (Z_{TR}).

EXAMPLE:

Calculate Z_T to make $Z_{TR} = 600\Omega$ in series with 2.16µF. $R_P = 30\Omega$.

$$Z_T = 200\left(600 + \frac{1}{j\omega 2.16X10^{-6}} - (2)(30)\right) \quad \text{(EQ. 33)}$$

$Z_T = 108k\Omega$ in series with 0.0108µF.

Note: Some impedance models, with a series capacitor, will cause the op-amp feedback to behave as an open circuit DC. A resistor with a value of about 10 times the reactance of the Z_T capacitor (2.16µF/200 = 10.8nF) at the low frequency of interest (200Hz for example) can be placed in parallel with the capacitor in order to solve the problem (736kΩ for a 10.8nF capacitor).

Calculating Tip and Ring Voltages

The **on hook** tip to ground voltage is calculated using Equation 34. The minus 1.0 volt results from the SLIC self programming. ISH- is the maximum loop current for a constant on hook overhead voltage (ISH- = $I_{\overline{SHD}}(0.6)$) and the value of $R_{SAT(off)}$ is calculated in Equation 4.

On hook Tip Voltage

$$V_{TIP(onhook)} = -1.0V + -(ISH\text{-})\left(\frac{R_{SAToff}}{2}\right) \quad \text{(EQ. 34)}$$

The **off hook** tip to ground voltage is calculated using Equation 35. $I_{LOOP(min)}$ is the minimum loop current allowed by the design and the value of $R_{SAT(off)}$ is calculated in Equation 4.

Off hook Tip Voltage

$$V_{TIP(offhook)} = -1V - (I_{LOOP(min)})\frac{R_{SAT(off)}}{2} - I_{LOOP(MAX)} \times R_P \quad \text{(EQ. 35)}$$

The **on hook** ring to ground voltage is calculated using Equation 36. The 1.5 volt results from the SLIC self programming. ISH- is the maximum loop current for a constant on hook overhead voltage (ISH- = $I_{\overline{SHD}}(0.6)$) and the value of $R_{SAT(off)}$ is calculated in Equation 4.

On hook Ring Voltage

$$V_{RING(onhook)} = V_{BH} + 1.5V + (ISH\text{-})\left(\frac{R_{SAT(off)}}{2}\right) \quad \text{(EQ. 36)}$$

The calculation of the ring voltage with respect to ground in the off hook condition is dependent upon whether the SLIC is in current limit or not.

The **off hook** ring to ground voltage (in current limit) is calculated using Equation 37. I_{LIM} is the programmed loop current limit and R_L is the load resistance across tip and ring. The minus 0.2V is a correction factor for the 60kΩ slope in Figure 15.

Off hook Ring Voltage in Current Limit

$$V_{RING(CL)} = V_{TIP(offhook)} - I_{LOOP(MAX)}R_L - 0.2V \quad \text{(EQ. 37)}$$

The **off hook** ring to ground voltage (not in current limit) is calculated using Equation 38. The 1.5V results from the SLIC self programming. $I_{LOOP(min)}$ is the minimum loop current allowed by the design and the value of $R_{SAT(off)}$ is calculated in Equation 4.

Off hook Ring Voltage not in Current Limit

$$V_{RING(NCL)} = V_{BH} + 1.5V + (I_{LOOP(min)})\left(\frac{R_{SAT(off)}}{2}\right) - I_{LOOP(MIN)} \times R_P \quad \text{(EQ. 38)}$$

Layout Considerations

Systems with Dual Supplies (V_{BH} and V_{BL})

If the V_{BL} supply is ***not*** derived from the V_{BH} supply, it is recommended that an additional diode be placed in series with the V_{BH} supply. The orientation of this diode is anode on pin 8 of the device and cathode to the external supply. This external diode will inhibit large currents and potential damage to the SLIC, in the event the V_{BH} supply is shorted to GND. If V_{BL} is derived from V_{BH} then this diode is not required. Suggested (not required) supply sequence V_{BH} - V_{BL}- V_{CC}.

Floating the PTG Pin

The PTG pin is a high impedance pin (500kΩ) that is used to program the 2-wire to 4-wire gain to either 0dB or -6dB.

If 0dB is required, it is necessary to float the PTG pin. The PC board interconnect should be as short as possible to minimize stray capacitance on this pin. Stray capacitance on this pin forms a low pass filter and will cause the 2-wire to 4-wire gain to roll off at the higher frequencies.

If a 2-wire to 4-wire gain of -6dB is required, the PTG pin should be grounded as close to the device as possible.

SPM Pin

For optimum performance, the PC board interconnect the SPM pin should be as short as possible. If pulses metering is not being used, then this pin should be grounded as close to the device pin as possible.

RLIM Pin

The current limiting resistor R_{LIM} needs to be as close to the RLIM pin as possible.

Layout of the 2-Wire Impedance Matching Resistor Z_T

Proper connection to the ZT pin is to have the external Z_T network as close to the device pin as possible.

The ZT pin is a high impedance pin that is used to set the proper feedback for matching the impedance of the 2-wire side. This will eliminate circuit board capacitance on this pin to maintain the 2-wire return loss across frequency.

TABLE 1. DETECTOR STATES

STATE	C3	C2	C1	SLIC OPERATING STATE	ACTIVE DETECTOR	OUTPUT	
						SHD	$\overline{\text{GKD}}$_ LVM
0	0	0	0	Open Circuit State	4 wire loopback test capability	HIGH	HIGH
1	0	0	1	Ringing State (Previous State cannot be Reverse Active State)	Ring Trip Detector	↓	HIGH
2	0	1	0	Forward Active State	Loop Current Detector	↓	
					Ground Key Detector		↓
3	0	1	1	Test Active State Requires previous state to be in the Forward Active state to determine the On hook or Off hook status of the line.	**On Hook** Loopback Detector	LOW	
					Ground Key Detector		HIGH
					Off Hook Loop Current Detector	LOW	
					Line Voltage Detector		⎍⎍
4	1	0	0	Tip Open - Ground Start State	Ground Key Detector	↓	↓
5	1	0	1	Reserved	Reserved	N/A	N/A
6	1	1	0	Reverse Active State	Loop Current Detector	↓	
					Ground Key Detector		↓
7	1	1	1	Test Reversal Active State Requires previous state to be in the Reverse Active state to determine the On hook or Off hook status of the line.	**On Hook** Loop Current Detector	↓	HIGH
					Off Hook Loop Current Detector	LOW	
					Line Voltage Detector		⎍⎍
8	X	X	X	Thermal Shutdown		LOW	LOW

Digital Logic Inputs

Table 1 is the logic truth table for the 3V to 5V logic input pins. A combination of the control pins C3, C2 and C1 select 1 of the possible 6 operating states. The 8th state listed is Thermal Shutdown. Thermal Shutdown protection is invoked if a fault condition on the tip or ring causes the junction temperature of the die to exceed 175°C. A description of each operating state and the control logic follows:

Open Circuit State (C3 = 0, C2 = 0, C1 = 0)

In this state, the tip and ring outputs are in a high impedance condition (>1MΩ). No supervisory functions are available and $\overline{\text{SHD}}$ and $\overline{\text{GKD}}$ outputs are at a TTL high level.

4-wire loopback testing can be performed in this state. With the PTG pin floating, the signal on the V_{TX} output is 180^o out of phase and approximately 2 times the V_{RX} input signal. If the PTG pin is grounded, then the amplitude will be approximately the same as its input and 180^o out of phase.

Ringing State (C3 = 0, C2 = 0, C1 = 1)

In this state, the output of the ring relay driver pin (RRLY) goes low (energizing the ring relay to connect the ringing signal to the phone) if either of the following two conditions are satisfied:

(1) The RSYNC_REV pin is grounded through a resistor - This connection enables the RRLY pin to go low the instant the ringing state is invoked, without any regard for the ringing voltage ($90V_{RMS}$ -$120V_{RMS}$) across the relay contacts. The resistor (34.8kΩ to 70kΩ) is required to limit the current into the RSYNC_REV pin.

(2) A ring sync pulse is applied to the RSYNC_REV pin - This connection enables the RRLY pin to go low at the command of a ring sync pulse. A ring sync pulse should go low at zero **voltage** crossing of the ring signal. This pulse should have a rise and fall time <400µs and a minimum pulse width of 2ms.

Zero ring **current** detection is performed automatically inside the SLIC. This feature de-energizes the ring relay slightly before zero current occurs to partially compensate for the delay in the opening of the relay.

The $\overline{\text{SHD}}$ output will go low when the subscriber goes off hook. Once $\overline{\text{SHD}}$ is activated, an internal latch will prohibit the re-ringing of the line until the ringing code is removed and then reapplied.

The state prior to ringing the phone, can not be the Reverse Active State. In the reverse active state the polarity of the voltage on the CRT_REV_$\overline{\text{LVM}}$ capacitor, will make it appear as if the subscriber is off hook. This subsequently will activate an internal latch prohibiting the ringing of the line.

The $\overline{\text{GKD}}$_LVM output is disabled (TTL high level) during the ringing state. Reference the Section titled “Ringing the Phone” for more information.

Forward Active State (C3 = 0, C2 = 1, C1 = 0)

In this state, the SLIC is fully functional. The tip voltage is more positive than the ring voltage. The tip and ring output voltages are an unbalanced DC feed, reference Figure 13. Both $\overline{\text{SHD}}$ and $\overline{\text{GKD}}$ supervisory functions are active. Reference the section titled “DC Feed Curve” for more information.

Test Active State (C3 = 0, C2 = 1, C1 = 1)

Proper operation of the Test Active State requires the previous state be the Forward Active state to determine the on hook or off hook status of the line. In this state, the SLIC can perform two different tests.

If the subscriber is **on hook** when the state is entered, a loopback test is performed by switching an internal 600Ω resistor between tip and ring. The current flows through the internal 600Ω is unidirectional via blocking diodes. (Cannot be used in reverse.) When the loopback current flows, the $\overline{\text{SHD}}$ output will go low and remain there until the state is exited. This is intended to be a short test since the ability to detect subscriber off hook is lost during loopback testing. Reference the section titled “Loopback Tests” for more information.

If the subscriber is **off hook** when the state is entered, a Line Voltage Measurement test is performed. The output of the $\overline{\text{GKD}}$_$\overline{\text{LVM}}$ pin is a pulse train. The pulse width of the active low portion of the signal is proportional to the voltage across the tip and ring pins. If the loop length is such that the SLIC is operating in constant current, the tip to ring voltage can be used to determine the length of the line under test. The longer the line, the larger the tip to ring voltage and the wider the pulse. This relationship can determine the length of the line for setting gains in the system. Reference the section titled “Operation of Line Voltage Measurement” for more information.

Tip Open State (C3 = 1, C2 = 0, C1 = 0)

In this state, the tip output is in a high impedance state (>250kΩ) and the ring output is capable of full operation, i.e. has full longitudinal current capability. The Tip Open/Ground Start state is used to interface to a PBX incoming 2-wire trunk line. When a ground is applied through a resistor to the ring lead, this current is detected and presented as a TTL logic low on the $\overline{\text{SHD}}$ and $\overline{\text{GKD}}$_$\overline{\text{LVM}}$ output pins.

Reserved (C3 = 1, C2 = 0, C1 = 1)

This state is undefined and reserved for future use.

Reverse Active State (C3 = 1, C2 = 1, C1 = 0)

In this state, the SLIC is fully functional. The ring voltage is more positive than the tip voltage. The tip and ring output voltages are an unbalanced DC feed, reference Figure 13. The polarity reversal time is determined by the RC time constant of the RSYNC_REV resistor and the CRT_REV_$\overline{\text{LVM}}$ capacitor. Capacitor CRT_REV_$\overline{\text{LVM}}$ performs three different functions: Ring trip filtering, polarity reversal time and line voltage measurement. It is recommended that programming of the reversal time be accomplished by changing the value of RSYNC_REV resistor (see Figure 18). The value of RSYNC_REV resistor is limited between 34.8K (10ms) and 73.2k (21ms). Equation 39 gives the formula for programming the reversal time.

$$\mathrm{RSYNC-REV} = 3.47\mathrm{k}\Omega \times \mathrm{ReversalTime(ms)} \qquad \text{(EQ. 39)}$$

Both $\overline{\text{SHD}}$ and $\overline{\text{GKD}}$ supervisory functions are active. Reference the section titled “Polarity Reversal” for more information.

Test Reversal Active State (C3 = 1, C2 = 1, C1 = 1)

Proper operation of the Test Reversal Active State requires the previous state be the Reverse Active state to determine the on hook or off hook status of the line.

If the subscriber is **on hook** when the state is entered, the SLIC’s tip and ring voltages are the same as the Reverse Active state. The $\overline{\text{SHD}}$ output will go low when the subscriber goes off hook and the $\overline{\text{GKD}}$_LVM output is disabled (TTL level high). (Note: operation is the same as the Reverse Active state with the GKD_LVM output disabled.)

If the subscriber is **off hook** when the state is entered, a Line Voltage Measurement test is performed.

The output of the $\overline{\text{GKD}}$_$\overline{\text{LVM}}$ pin is a pulse train. The pulse width of the active low portion of the signal is proportional to the voltage across the tip and ring pins. If the loop length is such that the SLIC is operating in constant current mode, the tip to ring voltage can be used to determine the length of the line under test. The longer the line, the larger the tip to ring voltage and the wider the pulse. This relationship can determine the length of the line for setting gains in the system. Reference the section titled “Operation of Line Voltage Measurement” for more information.

Thermal Shutdown

The UniSLIC14's thermal shutdown protection is invoked if a fault condition causes the junction temperature of the die to exceed about 175°C. Once the thermal limit is exceeded, both detector outputs go low ($\overline{\text{SHD}}$ and $\overline{\text{GKD}}$_$\overline{\text{LVM}}$) and one of two things can happen.

For marginal faults where loop current is flowing during the time of the over-temperature condition, foldback loop current limiting reduces the loop current by reducing the tip to ring voltage. An equilibrium condition will exist that maintains the junction temperature at about 175°C until the fault condition is removed.

For short circuit faults (tip or ring to ground, or to a supply, etc.) that result in an over-temperature condition, the foldback current limiting will try to maintain an equilibrium at about 175°C. If the junction temperature keeps rising, the device will thermally shutdown and disconnect tip and ring until the junction temperature falls to approximately 150°C.

Supervisory Functions

Switch Hook Detect Threshold

The Switch Hook Detect Threshold is programmed with a single external resistor (R_D). The output of the $\overline{\text{SHD}}$ pin goes low when an off hook condition is detected.

Ground Key Detect Threshold

The Ground Key Detect Threshold is set internally and is not user programmable.

Ringing the Phone

The UniSLIC14 family handles all the popular ringing formats with high or low side ring trip detection. High side detection is possible because of the high common mode range on the ring signal detect input pins (DT, DR). To minimize power drain from the ring generator, when the phone is not being rung, the sense resistors are typically 2MΩ. This reduces the current draw from the ring generator to just a few microamps.

When the subscriber goes off hook during ringing, the UniSLIC14 family automatically releases the ring relay and DC feed is applied to the loop. The UniSLIC14 family has very low power dissipation in the on hook active mode. This enables the SLIC (during the ring cadence) to be powered up in the active state, avoiding unnecessary powering up and down of the SLIC. The control logic is designed to facilitate easy implementation of the ring cadence, requiring only one bit change to go from active to ringing and back again.

DT, DR AND RRLY INPUTS

Ring trip detection will occur when the DR pin goes more positive than DT by approximately 4V.

The ring relay driver pin, RRLY, has an internal clamp between it's output and ground. This eliminates the need to place an external snubber diode across the ring relay.

Reducing Impulse Noise During Ringing

With an increase in digital data lines being installed next to analog lines, the threat from impulse noise on analog lines is increasing. Impulse noise can cause large blocks of high speed data to be lost, defeating most error correcting techniques. The UniSLIC14 family has the capability to reduce impulse noise by closing the ring relay at zero voltage and opening the ring relay at zero current.

CLOSING THE RING RELAY AT ZERO VOLTAGE

Closing the ring relay at zero voltage is accomplished by providing a ring sync pulse to the RSYNC_REV pin. The ring sync pulse is synchronized to go low at the zero voltage crossing of the ring signal. The resistor R1 in Figure 18 limits the current into the RSYNC_REV pin. If a particular polarity reversal time is required, then make R1 equal to the calculated value in Equation 39. If a specific polarity reversal time is not desired, R1 equal to 50kΩ is suggested.

The RSYNC_REV pin is designed to allow the ring sync pulse to be present at all times. There is no need to gate the ring sync pulse on and off. The logic control for the RSYNC_REV pin **cannot** be an open collector. It must be high (push-pull logic output stage / pull up resistor to VCC), low or being clocked by the ring sync pulse. When the RSYNC_REV pin is high the ring relay pin is disabled. When the RSYNC_REV pin is low the ring relay pin is activated the instant the logic code for ringing is applied.

OPENING THE RING RELAY AT ZERO CURRENT

The ring relay is automatically opened at zero current by the SLIC. The SLIC logic requires zero ringing current in the loop and either a valid switch hook detect ($\overline{\text{SHD}}$) or a change in the operating mode (cadence of the ringing signal) to release the ring relay.

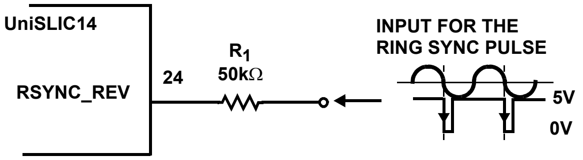


FIGURE 18. REDUCING IMPULSE NOISE USING THE RSYNC_REV PIN AND SETTING THE POLARITY REVERSAL TIME

If the subscriber goes off hook during ringing, the $\overline{\text{SHD}}$ output will go low. An internal latch will sense $\overline{\text{SHD}}$ is low and disable the ring relay at zero ringing current. This prevents the ring signal from being reapplied to the line. To ring the line again, the SLIC must toggle between logic states. (Note: The previous state can not be the Reverse Active State. In the reverse state, the voltage on the CRT_REV_$\overline{\text{LVM}}$

capacitor will activate an internal latch prohibiting the ringing of the line.

Figure 19 shows the sequence of events from ringing the phone to ring trip. The ring relay turns on when both the ringing code and ring sync pulse are present (A). $\overline{\text{SHD}}$ is high at this point. When the subscriber goes off hook the $\overline{\text{SHD}}$ pin goes low and stays low until the ringing control code is removed (B). This prevents the $\overline{\text{SHD}}$ output from pulsing after ring trip occurs. At the next zero current crossing of the ring signal, ring trip occurs and the ring relay releases the line to allow loop current to flow in the loop (C).

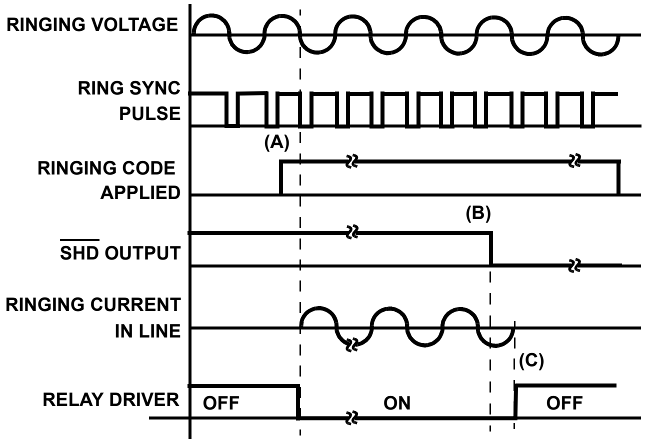


FIGURE 19. RINGING SEQUENCE

Operation of Line Voltage Measurement

A few of the SLICs in the UniSLIC14 family feature Line Voltage Measurement (LVM) capability. This feature provides a pulse on the $\overline{\text{GKD}}\_\overline{\text{LVM}}$ output pin that is proportional to the loop voltage. Knowing the loop voltage and thus the loop length, other basic cable characteristics such as attenuation and capacitance can be inferred. Decisions can be made about gain switching in the CODEC to overcome line losses and verification of the 2-wire circuit integrity.

The LVM function can only be activated in the off hook condition in either the forward or reverse operating states. The LVM uses the ring signal supplied to the SLIC as a timebase generator. The loop resistance is determined by monitoring the pulse width of the output signal on the $\overline{\text{GKD}}\_\overline{\text{LVM}}$ pin. The output signal on the $\overline{\text{GKD}}\_\overline{\text{LVM}}$ pin is a square wave for which the average duration of the low state is proportional to the average voltage between the tip and ring terminals. The loop resistance is determined by the tip to ring voltage and the constant loop current. Reference Figure 20.

Although the logic state changes to the Test Active State when performing this test, the SLIC is still powered up in the active state (forward or reverse) and the subscriber is unaware the measurement is being taken.

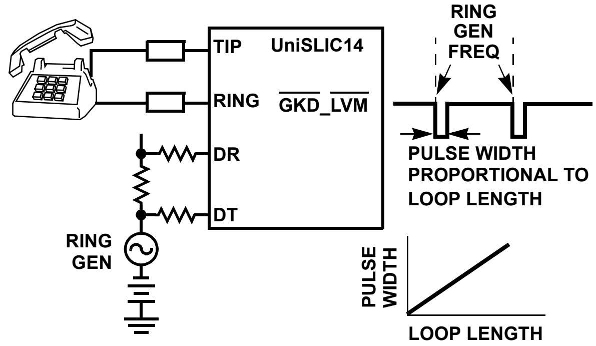


FIGURE 20. OPERATION OF THE LINE VOLTAGE MEASUREMENT CIRCUIT

Polarity Reversal

Most of the SLICs in the UniSLIC14 family feature full polarity reversal. Full polarity reversal means that the SLIC can: transmit, determine the status of the line (on hook and off hook) and provide "silent" polarity reversal. The value of RSYNC_REV resistor is limited between 34.8k (10ms) and 73.2k (21ms). Reference Equation 39 to program the polarity reversal time.

Transhybrid Balance

If a low cost CODEC is chosen that does not have a transmit op-amp, the UniSLIC14 family of SLICs can solve this problem without the need for an additional op-amp. The solution is to use the **P**rogrammable **T**ransmit **G**ain pin (PTG) as an input for the receive signal (V_{RX}). In theory, when the PTG pin is connected to a divider network (R1 and R2 Figure 21) and the value of R1 and R2 is much less than the internal 500kΩ resistors, two things happen. First the transmit gain from V_{RX} to V_{TX} is reduced by half. This is the result of shorting out the bottom 500kΩ resistor with the much smaller external resistor. And second, the input signal from V_{RX} is also decreased by the voltage divider R1 and R2. Transhybrid balance occurs when these two, equal but opposite in phase, signals are cancelled at the input to the output buffer. The calculation of the value of R2, once R1 is selected, is effected by the line feed resistors. EQ. 40 can be used to calculate the value of R2. Where : Z_L= Line Impedance, Z_{TR} = input impedance of SLIC including the protection resistor, and RP = protection resitors (typical 30Ω).

$$R_2 = \frac{R_1 \| 500K}{1.02}\left(\frac{Z_L + Z_{TR}}{Z_L + 2ZR_P}\right) - \frac{R_1 \| 500K}{1.02} \qquad \text{(EQ. 40)}$$

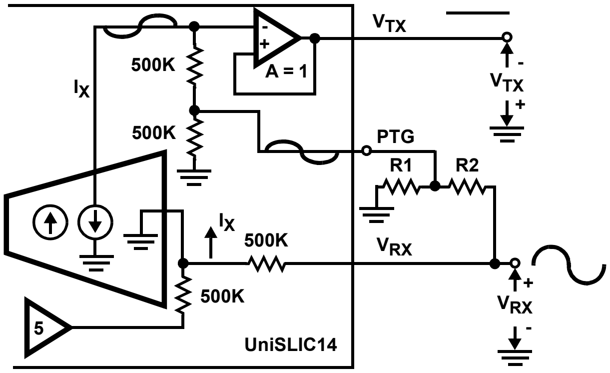


FIGURE 21. TRANSHYBRID BALANCE USING THE PTG PIN

Loopback Tests

4-Wire Loopback Test

This feature can be very useful in the testing of line cards during the manufacturing process and in field use. The test is unobtrusive, allowing it to be used in live systems. Reference Figure 22.

Most systems do not provide 4-wire loopback test capability because of costly relays needed to switch in external loads. All the SLICs in the UniSLIC14 family can easily provide this function when configured in the Open Circuit logic state. With the PTG pin floating, the signal on the V_{TX} output is 180° out of phase and approximately 2 times the V_{RX} input signal. If the PTG pin is grounded, then the amplitude will be approximately the same as the input signal and 180° out of phase.

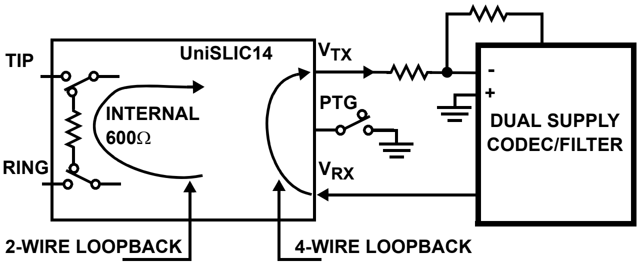


FIGURE 22. 4-WIRE AND 2-WIRE LOOPBACK TESTS

2-Wire Loopback Test

Most of the SLICs in the UniSLIC14 family feature 2-Wire loopback testing. This loopback function is only activated when the subscriber is **on hook** and the logic command to the SLIC is in the Test Active State. (Note: if the subscriber is **off hook** and in the Test Active State, the function performed is the Line Voltage Measurement.)

During the 2-wire loopback test, a 2kΩ internal resistor is switched across the tip and ring terminals of the SLIC. This allows the $\overline{SHD}$ function and the 4-wire to 4-wire AC transmission, right up to the subscriber loop, to be tested. Together with the 4-wire loopback test in the Open Circuit logic state, this 2-wire loopback test allows the complete network (including SLIC) to be tested up to the subscriber loop.

Pulse Metering

The HC55121, HC55142, HC35143, and HC55150 are designed to support pulse metering. They offer solutions to the following pulse metering design issues:

1) Providing adequate signal gain and current drive to the subscriber metering equipment to overcome the attenuation of this (12kHz, 16kHz) out of band signal.

2) Attenuating the pulse metering transhybrid signal without severely attenuating the voice band signal to avoid clipping in the CODEC/Filter.

3) Tailoring the overload levels in the SLIC to avoid clipping of the combined voiceband and pulse metering signal.

4) Having the provision of silent polarity reversal as a backup in the case where the loop attenuates the out of band signal too much for it to be detected by the subscriber's metering equipment.

Adequate Signal Gain

Adequate signal gain and current drive to the subscriber's metering equipment is made easier by the network shown in Figure 23. The pulse metering signal is supplied to a dedicated high impedance input pin called SPM. The circuit in Figure 23 shows the connection of a network that sets the 2-wire impedance (Z_{TR}), at the pulse metering frequencies, to be approximately 200Ω. If the line impedance (Z_L) is equal to 200Ω at the pulse metering frequencies, then the 4-Wire to 2-wire gain (V_{TR}/SPM) is equal 4. Thereby lowering the input signal requirements of the pulse metering signal.

Note: The automatic pulse metering 2-wire impedance matching is independent of the programmed 2-wire impedance matching at voiceband frequencies.

Calculation of the pulse metering gain is achieved by replacing $V_{RX}/500k$ in Equation 15 with SPM/125k and following the same process through to Equation 21. The UniSLIC14 sets the 2-wire input impedance of the SLIC (Z_{TR}), including the protection resistors, equal to 200Ω. The results are shown in Equation 41.

$$A_{4-2} = \frac{V_{TR}}{SPM} = -8\frac{Z_L}{Z_L + Z_{TR}} = -8\frac{200}{200 + 200} = -4 \qquad \text{(EQ. 41)}$$

Avoiding Clipping in the CODEC/Filter

The amplitude of the returning pulse metering signal is often very large and could easily over drive the input to the CODEC/Filter. By using the same method discussed in section "Transhybrid Balance", most if not all of the pulse metering signal can be canceled out before it reaches the input to the CODEC/Filter. This connection is shown in Figure 23.

Overload Levels and Silent Polarity Reversal

The pulse metering signal and voice are simultaneously transmitted, and therefore require additional overhead to prevent distortion of the signal. Reference section “Off hook Overhead Voltage” to account for the additional pulse metering signal requirements.

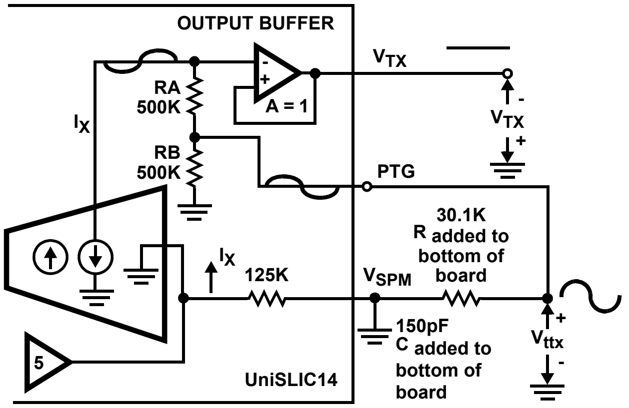


FIGURE 23. PULSE METERING WITH TRANSHYBRID BALANCE

Most of the SLICs in the UniSLIC14 family feature full polarity reversal. Full polarity reversal means that the SLIC can transmit, determine the status of the line (on hook and off hook) and provide “silent” polarity reversal. Reference Equation 39 to program the polarity reversal time.

Interface to Dual and Single Supply CODECs

Great care has been taken to minimize the number of external components required with the UniSLIC14 family while still providing the maximum flexibility. Figures 24A, 24B) shows the connection of the UniSLIC14 to both a dual supply CODEC/Filter and a single supply DSP CODEC/Filter.

To eliminate the DC blocking capacitors between the SLIC and the CODEC/Filter when using a dual supply CODEC/Filter, both the receive and transmit leads of the SLIC are referenced to ground. This leads to a very simple SLIC to CODEC/Filter interface, as shown in Figure 24A.

When using a single supply DSP CODEC/Filter the output and input of the CODEC/Filter are no longer referenced to ground. To achieve maximum voltage swing with a single supply, both the output and input of the CODEC/Filter are referenced to its own $V_{CC}/2$ reference. Thus, DC blocking capacitors are once again required. By using the PTG pin of the UniSLIC14 and the externally supplied $V_{CC}/2$ reference of the CODEC/Filter, one of the DC blocking capacitors can be eliminated (Figure 24B).

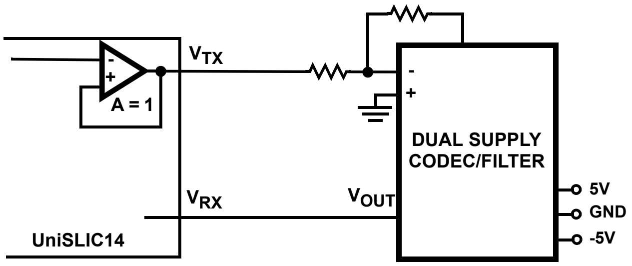


FIGURE 24A.

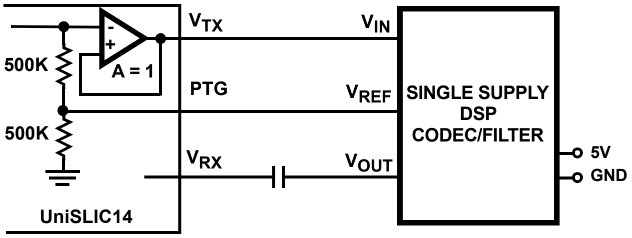


FIGURE 24B.

FIGURE 24. INTERFACE TO DUAL AND SINGLE SUPPLY CODECs

Power Management

The UniSLIC14 family provides two distinct power management capabilities:

Power Sharing and Battery Selection

Power Sharing

Power sharing is a method of redistributing the power away from the SLIC in short loop applications. The total system power is the same, but the die temperature of the SLIC is much lower. Power sharing becomes important if the application has a single battery supply (-48V on hook requirements for faxes and modems) and the possibility of high loop currents (reference Figure 25). This technique would prevent the SLIC from getting too hot and thermally shutting down on short loops.

The power dissipation in the SLIC is the sum of the smaller quiescent supply power and the much larger power that results from the loop current. The power that results from the loop current is the loop current times the voltage across the SLIC. The power sharing resistor (R_{PS}) reduces the voltage across the SLIC, and thereby the on-chip power dissipation. The voltage across the SLIC is reduced by the voltage drop across R_{PS}. This occurs because R_{PS} is in series with the loop current and the negative supply.

A mathematical verification follows: