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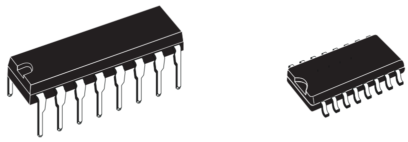
HCF4099B

8 BIT ADDRESSABLE LATCH

- SERIAL DATA INPUT - ACTIVE PARALLEL OUTPUT
- STORAGE REGISTER CAPABILITY - MASTER CLEAR
- CAN FUNCTION AS DEMULTIPLEXER
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP **SOP**

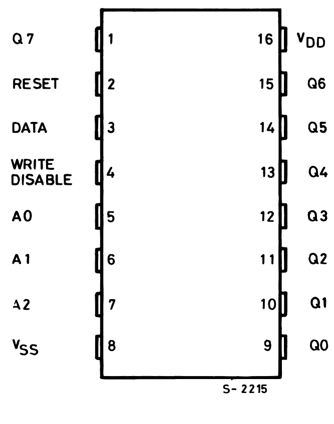
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4099BEY	
SOP	HCF4099BM1	HCF4099M013TR

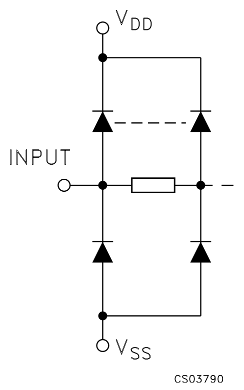
DESCRIPTION

HCF4099B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
HCF4099B, an 8-bit addressable latch, is a serial-input, parallel output storage register that can perform a variety of functions. Data is input to a particular bit in the latch when that bit is addressed (by means of input A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs. A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer ; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

PIN CONNECTION



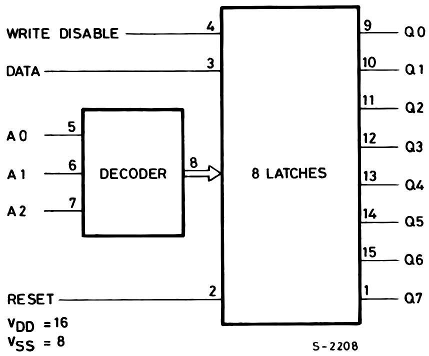
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
5, 6, 7	A0 to A2	Address Inputs
9, 10, 11, 12, 13, 14, 15, 1	Q0 to Q7	Latch Outputs
3	DATA	Data Inputs
2	RESET	Reset Input
4	WRITE DISABLE	Write Disable Input
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



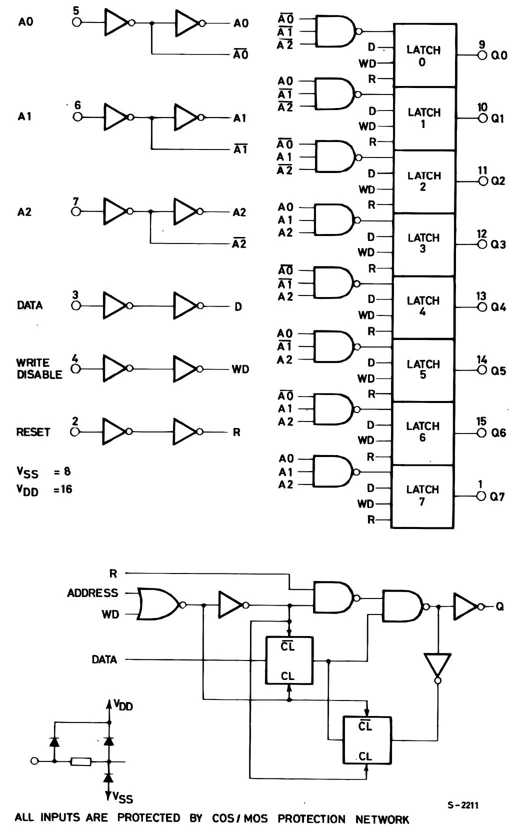
TRUTH TABLE

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

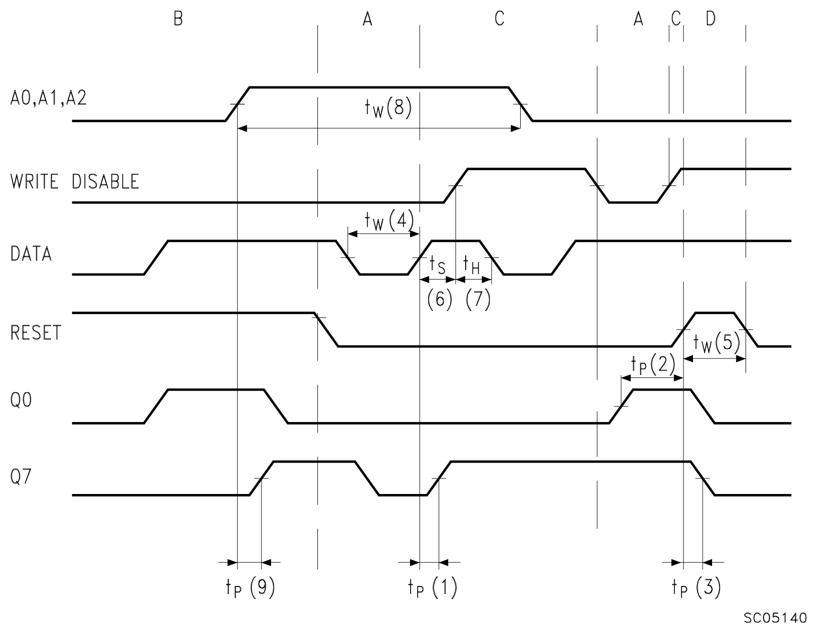
INPUTS		OUTPUTS OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
WRITE DISABLE	RESET			
L	L	D	Qi0	ADDRESSABLE LATCH
L	H	Qi0	Qi0	MEMORY
H	L	D	L	DEMULTIPLEXER
H	H	L	L	CLEAR ALL BITS TO "0"

D: The level at the data input ; Q_{i0} The level before the indicated steady state input conditions were established, (i=0, 1,...7)

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	µA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/18.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		0.5/4.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			1.5/18.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5		5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6		5	-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4		5	0.44	1		0.36		0.36		mA
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	any input		18		$\pm10^{-5}$	±0.1		±1		±1	µA
C_I	Input Capacitance		any input				5	7.5					pF

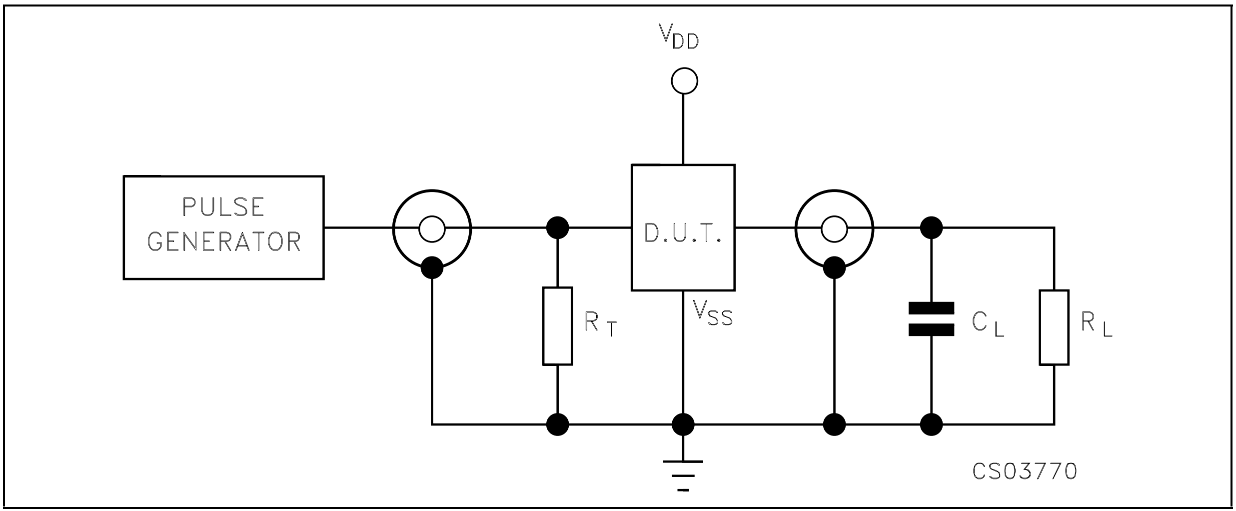
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)	See Timing Chart	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (Data to Output)	5	(1)		200	400	ns
		10			75	150	
		15			50	100	
t_{PLH} t_{PHL}	Propagation Delay Time (Write Disable to Output)	5	(2)		200	400	ns
		10			80	160	
		15			60	120	
t_{PLH} t_{PHL}	Propagation Delay Time (Address to Output)	5	(9)		225	450	ns
		10			100	200	
		15			75	150	
t_{PHL}	Propagation Delay Time (Reset to Output)	5	(3)		175	350	ns
		10			80	160	
		15			65	130	
t_{THL} t_{TLH}	Transition Time (any output)	5			100	200	ns
		10			50	100	
		15			40	80	
t_W	Pulse WIdth (Data)	5	(4)	200	100		ns
		10		100	50		
		15		80	40		
t_W	Pulse WIdth (Address)	5	(8)	400	200		ns
		10		200	100		
		15		125	65		
t_W	Pulse WIdth (Reset)	5	(5)	150	75		ns
		10		75	40		
		15		50	25		
t_{setup}	Setup Time (Data to Write Disable)	5	(6)	100	50		ns
		10		50	25		
		15		35	20		
t_{hold}	Hold Time (Data to Write Disable)	5	(7)	150	75		ns
		10		75	40		
		15		50	25		

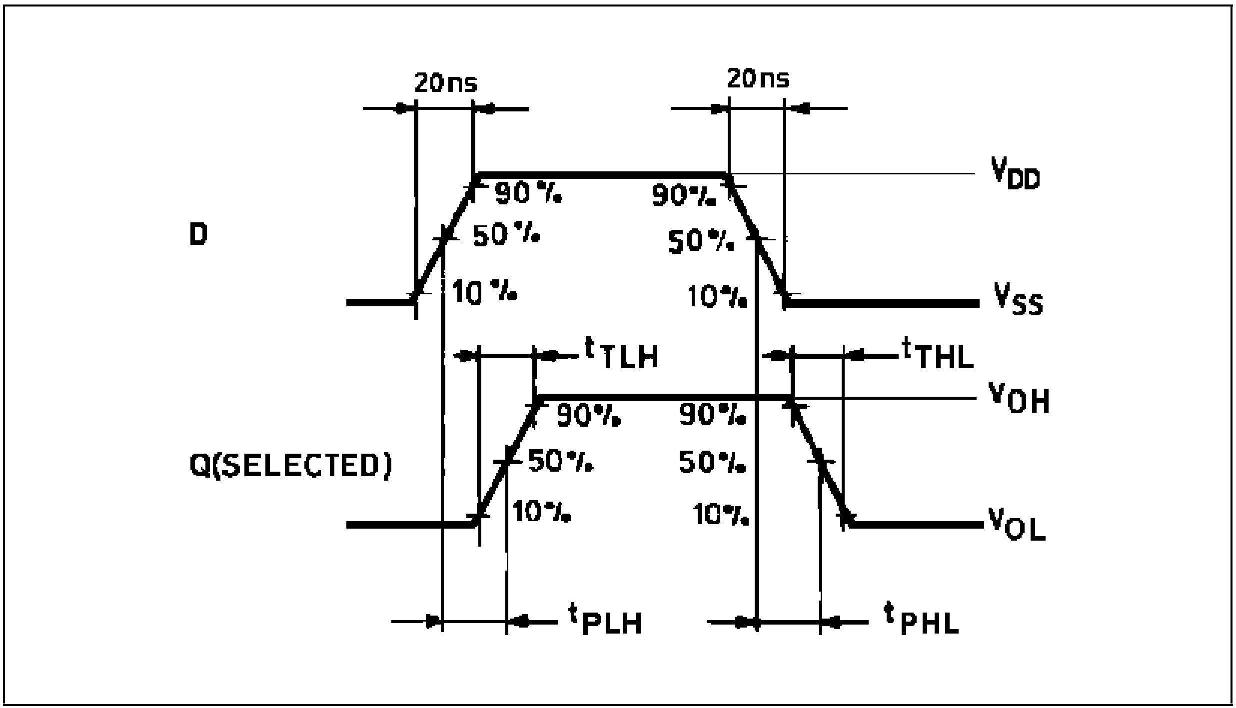
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TEST CIRCUIT

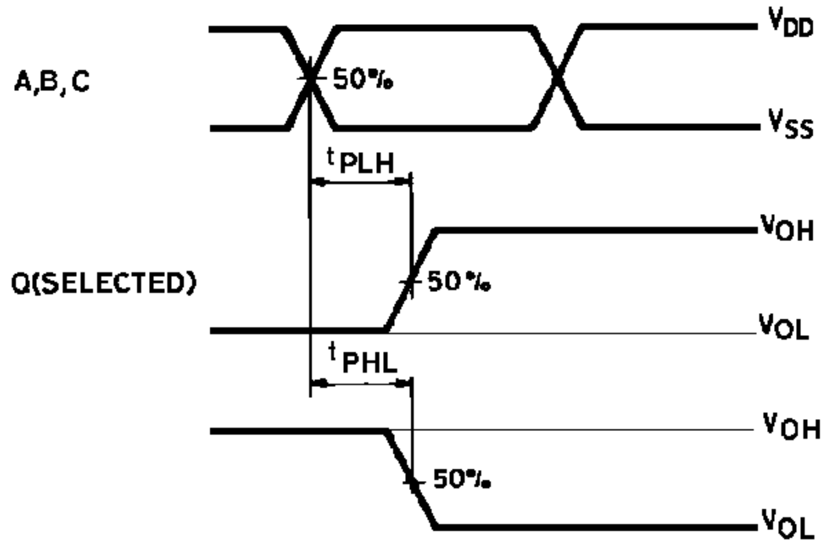


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

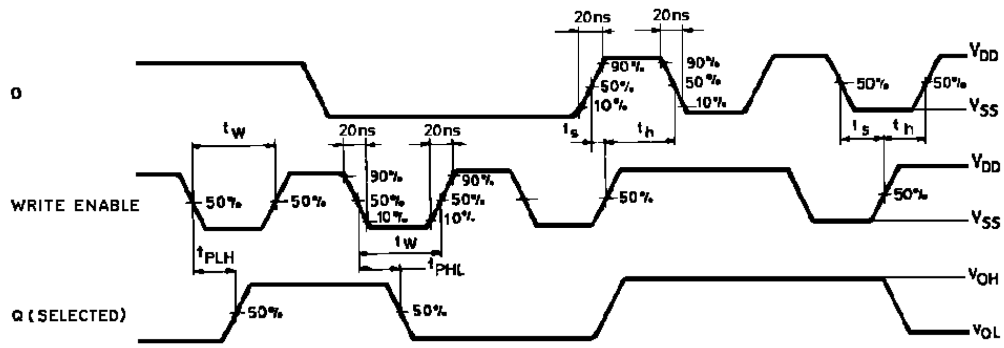
WAVEFORM 1 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



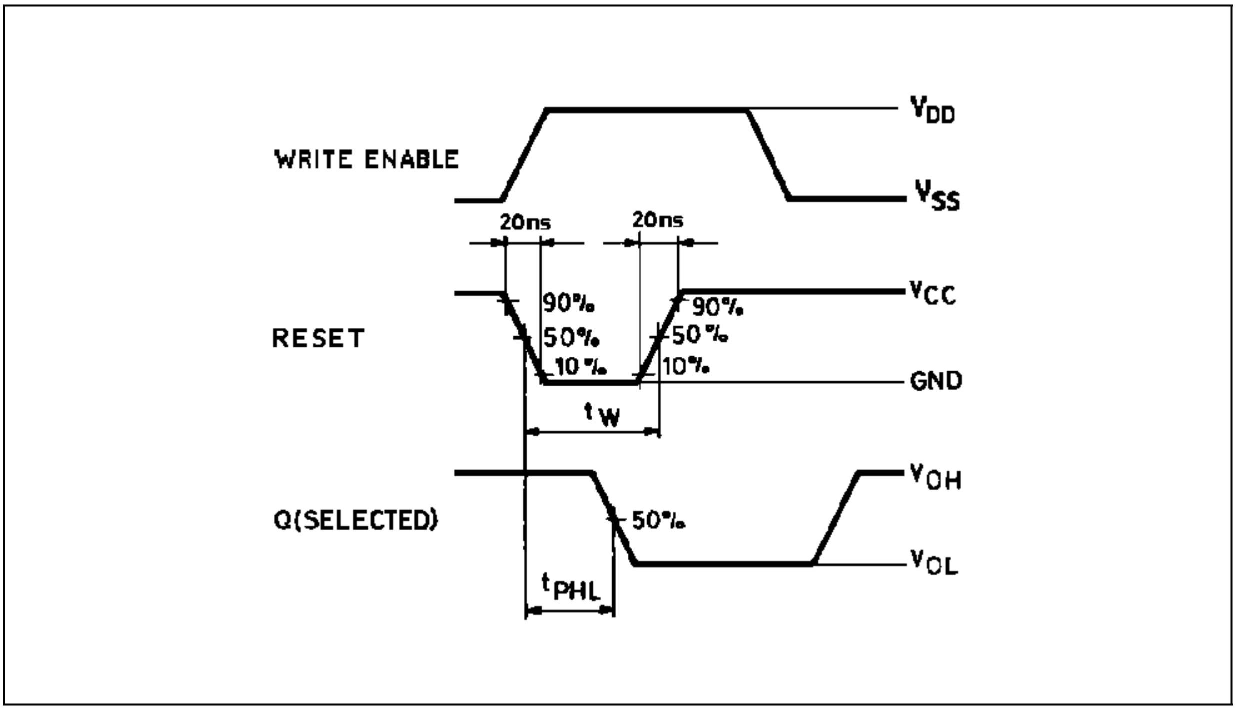
WAVEFORM 2 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



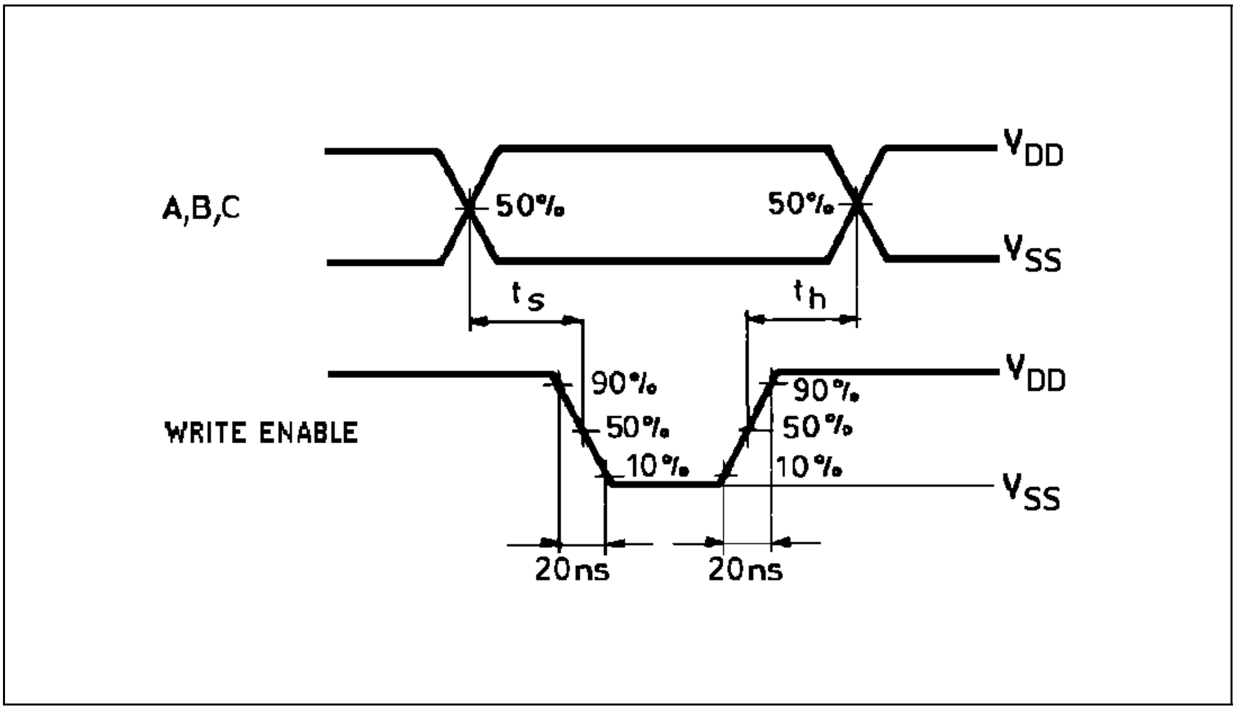
WAVEFORM 3 : MINIMUM PULSE WIDTH, SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



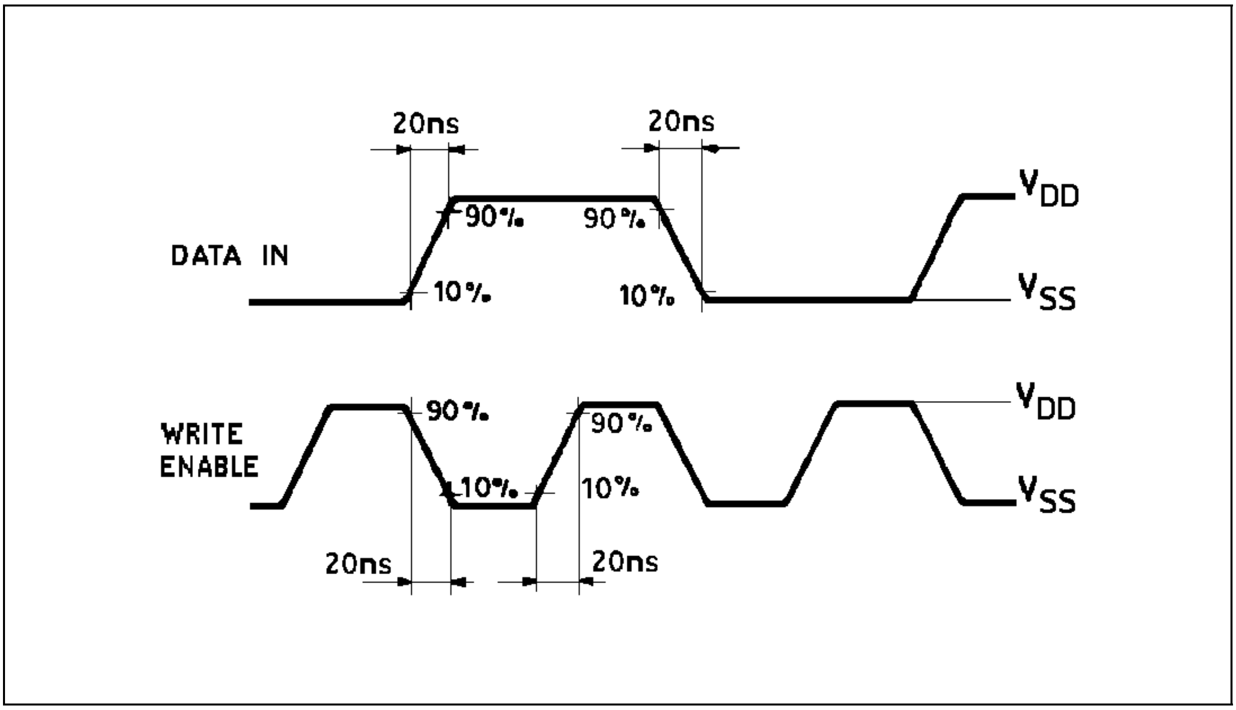
WAVEFORM 4 : MINIMUM PULSE WIDTH (f=1MHz; 50% duty cycle)



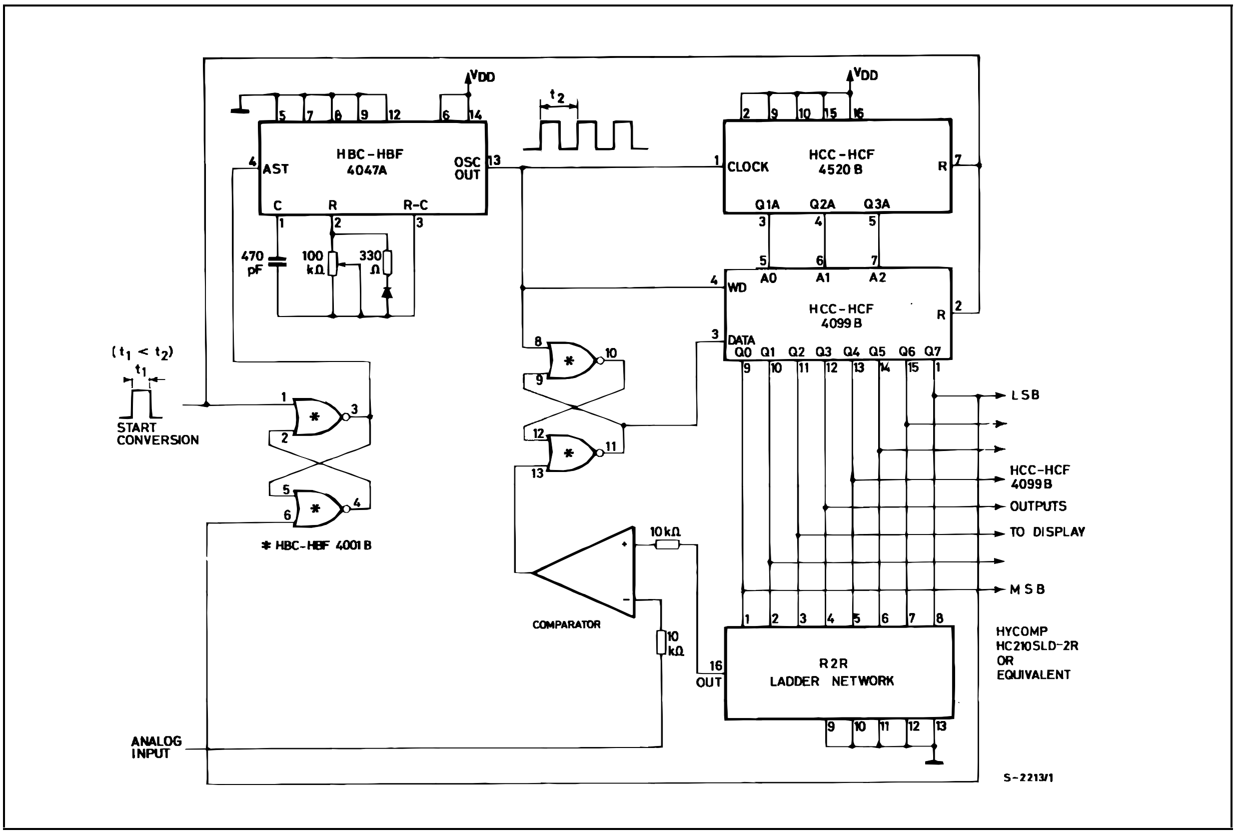
WAVEFORM 5 : SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



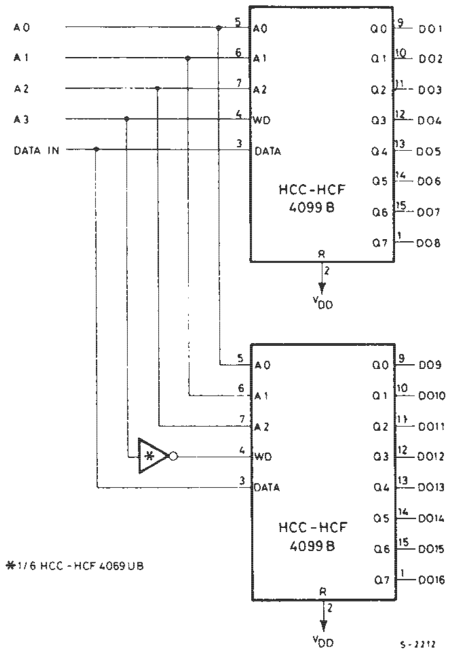
WAVEFORM 6 : INPUT WAVEFORMS (f=1MHz; 50% duty cycle)



TIPICAL APPLICATIONS

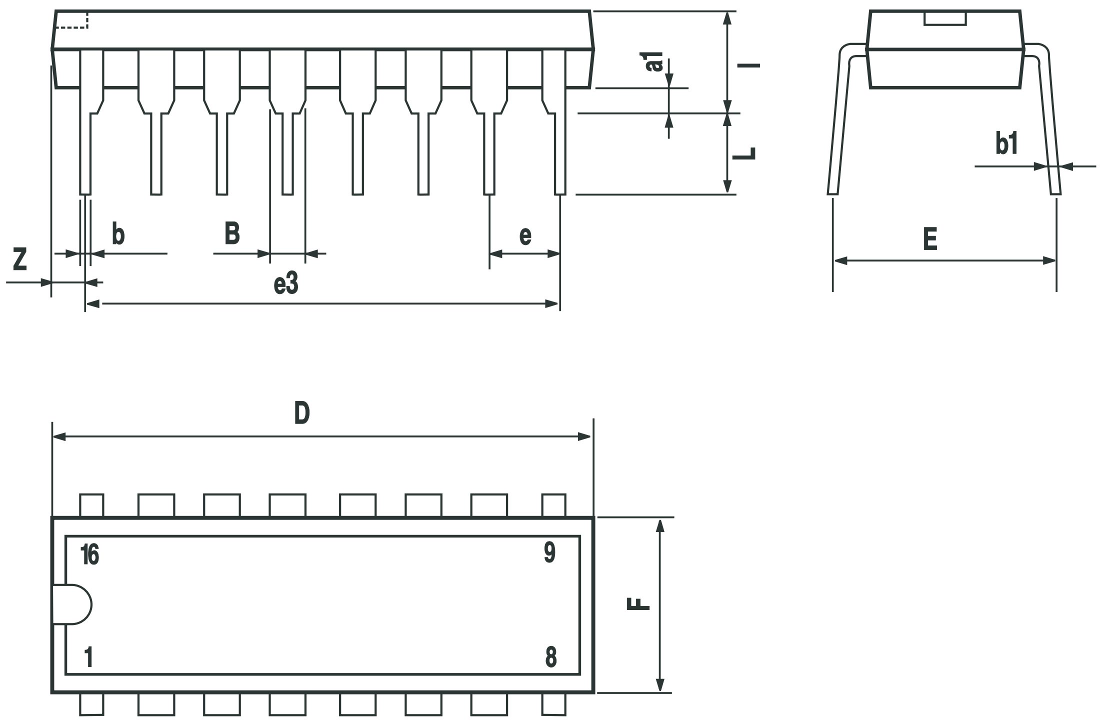


TIPICAL APPLICATIONS



Plastic DIP-16 (0.25) MECHANICAL DATA

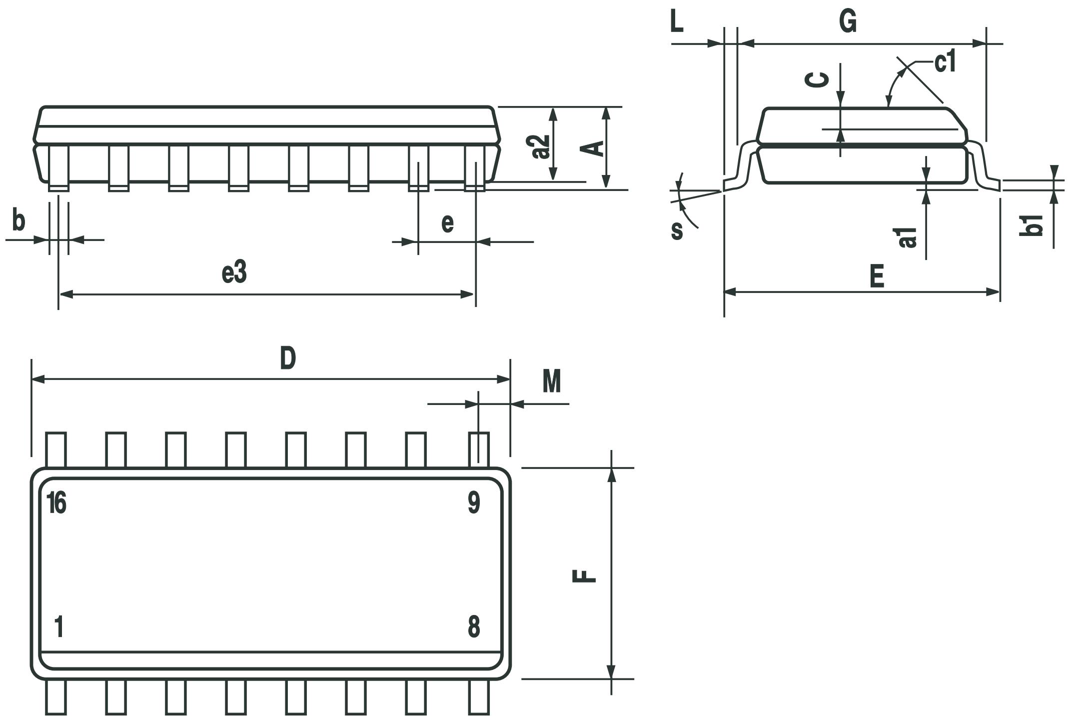
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

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